# S75WS-N Based MCPs

Stacked Multi-Chip Product (MCP) 256 Megabit (I6M x I6-bit) CMOS I.8 Volt-only Simultaneous Read/Write, Burst-mode Flash Memory with I28 Mb (8M x I6-Bit) RAM Type 4 and 5I2 Mb (32M x I6-bit) Data Flash or I Gb ORNAND Flash



Data Sheet

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# S75WS-N Based MCPs

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## Data Sheet

### PRELIMINARY

# **General Description**

The S75WS-N Series is a product line of stacked Multi-Chip Product (MCP) packages and consists of the following items:

- One or more S29WS-N code Flash
- RAM Type 4
- One or more S29WS-N data Flash, or one or more S30MS-P ORNAND Flash

The products covered by this document are listed in the table below:

Device			RAM ensity	NOR Data Flash Density	ORNAND Data Flash Density	
	256 Mb	128 Mb	256 Mb	512 Mb	1024 Mb	
S75WS256NDF	•			•		
S75WS256NEG						

# **Distinctive Characteristics**

## **MCP Features**

- Power supply voltage of 1.7 V to 1.95 V
- High Performance
  - 54 MHz, 66 Mhz, 80 MHz
- Packages
  - 9 x 12 mm 84 ball FBGA
  - 11 x 13 mm 115 ball FBGA
- Operating Temperature
  - Wireless, -25°C to +85°C



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# I Product Selector Guide

	Madal	1	MCP Configur		Code	RAM	Data Flash	Flash	pSRAM	DYB	pSRAM	Package
Device	Model Numbers	Code Flash	RAM (Mb)	Data Storage Flash	Density (Mb)	Density (Mb)	Density (Mb)	Speed (MHz)	Speed (MHz)	Power-Up State (See Note)	(RAM Type 4) Supplier	84 ball FBGA (mm)
	LK							54	54	0	- 4	9x12
	NK									1		
S75WS256NDF	LJ	WS256N 128	100	2xWS256N	256	128	512		66	0		
575W5250NDF	NJ		128					66		1		
	LH							80	80	0		
	NH									1		

**Note:** 0 (Protected), 1 (Unprotected [Default State])

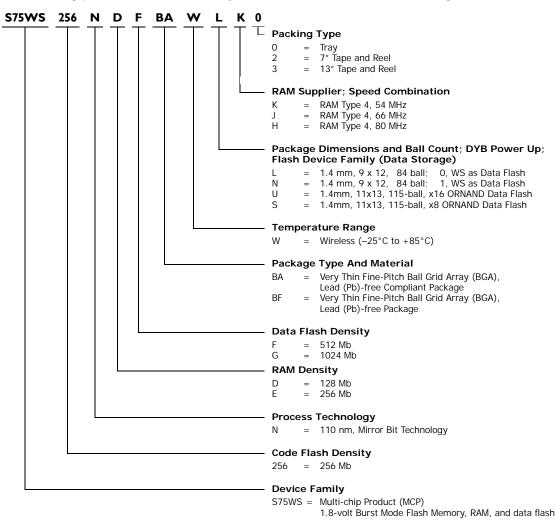
# I.I NOR Flash + pSRAM + ORNAND Flash MCPs

Device	Model Numbers	NOR Flash Density	ORNAND Flash Density	p <b>SRAM</b> Density	MCP Speed	Supplier	ORNAND Bus Width	Package
	UK				54 MHz	1.8 V pSRAM Type 4	x16	- 11 x 13 x 1.4 mm
	UJ	512 Mb			66 MHz			
	UH		1024 Mb	256 Mb	80 MHz			
S75WS256NEG	SK				54 MHz		x8	
	SJ				66 MHz			
	SH				80 MHz			



# 2 Ordering Information

The ordering part number is formed by a valid combination of the following:





Valid Combination								
S75WS256N	D	F	BA, BF	W	L, N	К, Н		

### Table 2.2 ORNAND Configurations and Valid Combinations

Valid Combination									
S75WS256N	E	G	BA, BF	W	U, S	K, J, H			

#### Package Marking Note:

The BGA package marking omits the leading S75 and packing type designator from the ordering part number.

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.



# **3** Input/Output Descriptions

Table 3.1 identifies the input and output package connections provided on the device.

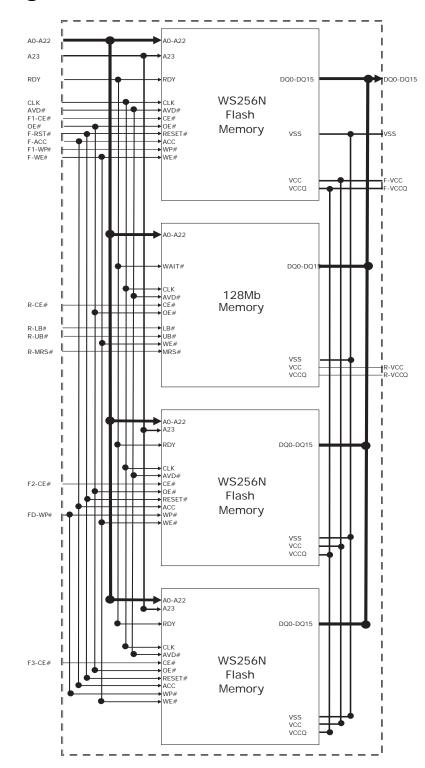
Symbol	Description							
A <sub>max</sub> – A0	Address Inputs							
DQ15 - DQ0	Data Inputs/Outputs							
OE#	Output Enable input	(Common)						
WE#	Write Enable input							
V <sub>SS</sub>	Ground							
NC	No Connect; not connected internally.	·						
RDY	Ready output. Indicates the status of the Burst read.	(Flash)						
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at $V_{\rm IL}$ or $V_{\rm IH}$ while in asynchronous mode.	(Common)						
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs.	(Flash)						
F-RST#	Hardware reset input.							
F-WP#	Hardware write protect input. At $V_{1L}$ , disables program and erase functions in the four outermost sectors. Should be at $V_{1H}$ for all other conditions.							
F-ACC	Accelerated input. At V <sub>HH</sub> , accelerates programming; automatically places device in unlock bypass mode. At V <sub>IL</sub> , disables all program and erase functions. Should be at V <sub>IH</sub> for all other conditions.							
R-CE#	Chip-enable input for pSRAM							
F1-CE#	Chip-enable input for Code Flash.							
F2-CE#	Chip-enable input for Data Flash 1.	Asynchronous relative to CLK for Burst Mode.						
F2-CE#	Chip-enable input for Data Flash 2.							
R-MRS#	Control Register Enable.	(pSRAM – RAM Type 4 only)						
F-V <sub>CC</sub>	Flash 1.8 Volt-only single power supply.	•						
R-V <sub>CC</sub>	pSRAM Power Supply.							
R-UB#	Upper Byte Control.	(nSPAM)						
R-LB#	Lower Byte Control .	– (pSRAM)						

Table 3.2 identifies the ORNAND input and output connections provided on the device.

Symbol	Description				
N-PRE	ORNAND Power-On Read Enable. Tie to V <sub>SS</sub> on customer board if not used.				
N-ALE	ORNAND Address Latch Enable				
N-CLE	ORNAND Command Latch Enable				
N-CE#	ORNAND Chip-enable				
N-WP#	ORNAND Write-protect				
N-WE#	ORNAND Write-enable				
N-RE#	ORNAND Read-enable				
N-RY/BY#	ORNAND Ready-Busy-this is shared with NOR RDY				
N-I/O0-N-I/O15	ORNAND I/O signals (I/O0-I/O7 for x8 bus width)				
N-V <sub>CC</sub>	ORNAND Power supply				



# 4 MCP Block Diagram



### Notes:

- 1. MRS is only present in RAM Type 4.
- 2. CE#f1, CE#f2, and CE#f3 are the chip enable pins for the first, second and third Flash devices, respectively.

Figure 4.1 MCP Block Diagram I



\_ \_ \_ \_ \_ \_ \_ \_ \_ A0-A22 A0-A22 A23 A23 DQ0-DQ15 DQ0-DQ15 RDY RDY WS256N CLK AVD# CLK AVD# Flash CE#
 OE#
 RESET# F-CE# F-CE# -OE# ₩ F-RST# F-ACC F1-WP# ₩ Memory V<sub>SS</sub> V<sub>SS</sub> ACC WP# WE# WE#  $V_{\rm CC}$ F-V<sub>CC</sub> V<sub>CCQ</sub> A0-A22 WAIT# DQ0-DQ15 → CLK → AVD# → CE# → OF <sup>++</sup> 128 Mb R1-CE# RAM OE# Memory R-LB# LB# R-UB# ► UB#
► WE#
► MRS# L R-MRS# V<sub>ss</sub> V<sub>cc</sub> R-V<sub>CC</sub> V<sub>CCQ</sub>  $\|$  $\|$ A0-A22  $\|$ WAIT# DQ0-DQ15 CLK 128 Mb AVD# CE# OE# R2-CE# RAM Memory LB# UB# WE# MRS# V<sub>SS</sub> V<sub>CC</sub> V<sub>CCQ</sub> 1/00-1/015 I/00-I/015 N-RY/BY# RB# MS01GP N-CLE CLE CE# ALE x16 ORNAND N-CE# N-ALE Memory V<sub>SS</sub> N-VSS N-RE# N-WP# RE# WP# PRE . WE# II  $V_{CC}$ N-V<sub>CC</sub> 

x16 MS01GP-based MCP





# 5 Connection Diagrams/Physical Dimensions

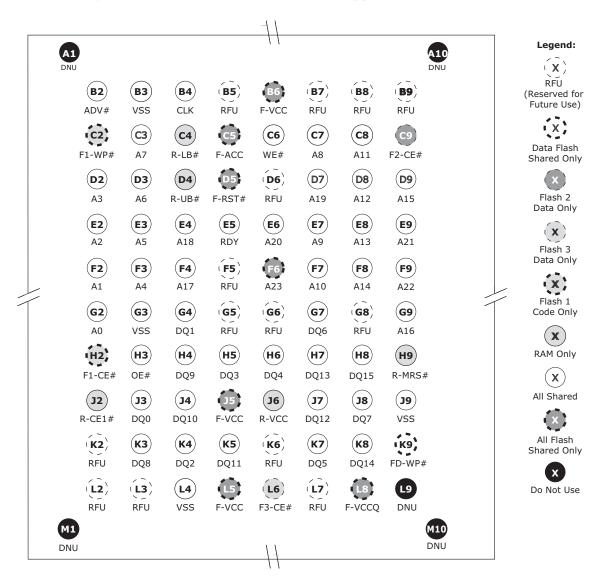
This section contains the I/O designations and package specifications for the S75WS.

## 5.1 Special Handling Instructions for FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

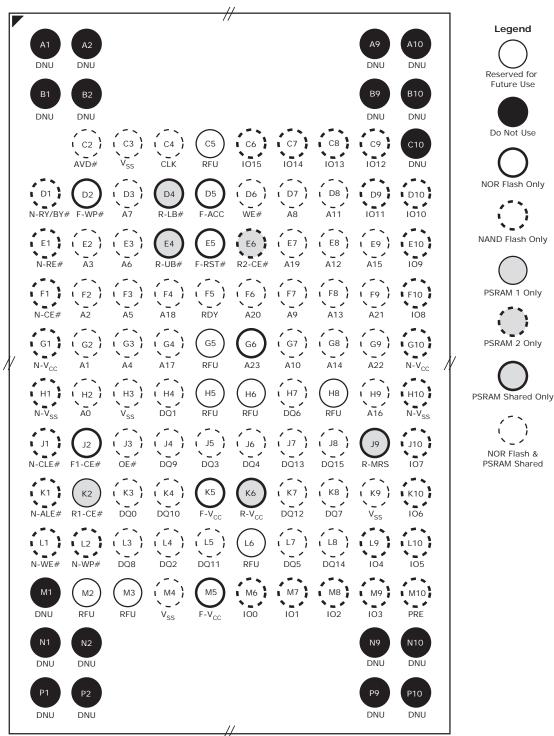
Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

## 5.2 Connection Diagram – NOR Flash & I.8 V RAM Type 4 Based Pinout, 9 x I2 mm





## 5.3 Connection Diagram – ORNAND-Based Pinout, II x I3 mm



Note: Bus 1: NOR Flash + pSRAM, Bus 2: ORNAND Flash



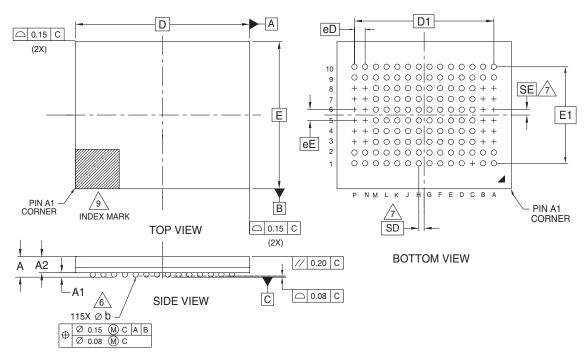
#### Physical Dimensions – FEA084 – Fine Pitch Ball Grid Array 9 x 12 mm 5.4

(2X)	C		D		$\begin{array}{c} \bullet \\ \bullet $				
PIN A CORNE	\1 <b>─</b> ∕			VIEW (2X)	$\begin{array}{c} B \\ + 0 \\ 7 \\ + 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\$				
A A2			<del></del>		D.20 C BOTTOM VIEW				
E	A1 84X	5 M C A	SIDE B		0.08 C				
PACKAGE		FEA 084							
JEDEC		N/A		-	<ol> <li>DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.</li> </ol>				
DxE	12.0	00 mm x 9.00	) mm	NOTE	2. ALL DIMENSIONS ARE IN MILLIMETERS.				
0.4.50		PACKAGE		-	3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.				
SYMBOL	MIN	NOM	MAX		4. e REPRESENTS THE SOLDER BALL GRID PITCH.				
A A1	0.10		1.40	PROFILE BALL HEIGHT	5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.				
A1 A2	1.11		1.26	BODY THICKNESS	SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE				
D		12.00 BSC.		BODY SIZE	"E" DIRECTION.				
E		9.00 BSC.		BODY SIZE	<ul> <li>n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.</li> </ul>				
D1		8.80 BSC.		MATRIX FOOTPRINT	6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL				
E1		7.20 BSC.		MATRIX FOOTPRINT	DIAMETER IN A PLANE PARALLEL TO DATUM C.				
MD		12		MATRIX SIZE D DIRECTION	SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A				
ME		10		MATRIX SIZE E DIRECTION	AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.				
n				BALL COUNT	WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE				
Øb	0.35	0.40	0.45	BALL DIAMETER	OUTER ROW SD OR SE = 0.000.				
eE		0.80 BSC.		BALL PITCH					
eD		0.80 BSC		BALL PITCH	OUTER ROW, SD OR SE = $\boxed{e/2}$ 8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED				
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT	BALLS.				
	B1,B E1,E H1,H10,	,A4,A5,A6,A7 10,C1,C10,D 10,F1,F10,G J1,J10,K1,K1 M4,M5,M6,M	1,D10 1,G10 10,L1,L10	DEPOPULATED SOLDER BALLS	9. N/A A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.				
					3423 \ 16-038.21				

3423 \ 16-038.21a



# 5.5 Physical Dimensions – FNDII5 – Fine Pitch Ball Grid Array II x I3 mm



DAGKAGE				
PACKAGE	FND 115			
JEDEC	N/A			
D x E	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A			1.40	PROFILE
A1	0.17			BALL HEIGHT
A2	0.98		1.15	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	10.40 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	115			BALL COUNT
Øb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A3-A8,B3-B8,C1,N3-N8,P3-P8			DEPOPULATED SOLDER BALLS

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- 2. ALL DIMENSIONS ARE IN MILLIMETERS.
- 3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- e REPRESENTS THE SOLDER BALL GRID PITCH.
   SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D"
- DIRECTION.
  - SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

- WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE =  $\left[\Theta/2\right]$
- 8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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# 6 MCP Revisions

## Revision A0 (February 17, 2005)

Initial Release

### Revision AI (September 8, 2005)

#### Global

Removed references to the S29RS-N data sheet

### Product Selector Guide

Updated table and added 80 MHz options

#### Ordering Information

Updated table with new options

#### MCP Configurations and Valid Combinations

Updated table to reflect new options

#### Input/Output Descriptions

Updated table and changed some pin names

#### MCP Block Diagram

Updated the illustration

#### **Connection Diagram**

Updated the pinout diagram

#### **Physical Dimensions**

Added the FEA084 package diagram

#### Look-Ahead Connection Diagram

Removed from data sheet

#### S29WS-N Flash Module

Updated to the latest revision

### Revision A2 (October 6, 2005)

#### Global

Added ORNAND Flash information

#### **Product Selector Guide**

Added ORNAND options

#### **Ordering Information**

Updated table with new options

#### MCP Block Diagram

Added the ORNAND illustration

#### **Connection Diagram**

Added the pinout diagram for the ORNAND device

#### **Physical Dimensions**

Added the FND115 package diagram



#### S29WS-N Flash Module

Removed from MCP. Available as a standalone document.

#### 1.8 V Type 4 pSRAM Module

Removed from MCP. Available as a standalone document.

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