

FEATURES

- 1.8 V AFETG core**
- Internal LDO regulator and charge pump circuitry**
- Compatibility with 3 V or 1.8 V systems**
- 24 programmable vertical clock outputs**
- Correlated double sampler (CDS) with -3 dB, 0 dB, +3 dB, and +6 dB gain**
- 6 dB to 42 dB, 10-bit variable gain amplifier (VGA)**
- 12-bit, 40 MHz ADC**
- Black level clamp with variable level control**
- Complete on-chip timing generator**
- Precision Timing* core with 400 ps resolution**
- On-chip 3 V horizontal and RG drivers**
- General-purpose outputs (GPOs) for shutter and system support**
- On-chip driver for external crystal**
- On-chip sync generator with external sync input**
- 105-lead CSP_BGA package, 8 mm × 8 mm, 0.65 mm pitch**

APPLICATIONS

Digital still cameras

GENERAL DESCRIPTION

The AD9992 is a highly integrated CCD signal processor for digital still camera applications. It includes a complete analog front end with A/D conversion combined with a full-function programmable timing generator. The timing generator is capable of supporting up to 24 vertical clock signals to control advanced CCDs. A *Precision Timing* core allows adjustment of high speed clocks with approximately 400 ps resolution at 40 MHz operation. The AD9992 also contains eight general-purpose input/outputs, which can be used for shutter and system functions.

The AD9992 is specified at pixel rates of up to 40 MHz. The analog front end includes black level clamping, CDS, VGA, and a 12-bit analog-to-digital converter (ADC). The timing generator provides all the necessary CCD clocks: RG, H-clocks, V-clocks, sensor gate pulses, substrate clock, and substrate bias control. Operation is programmed using a 3-wire serial interface.

The AD9992 is specified over an operating temperature range of -25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

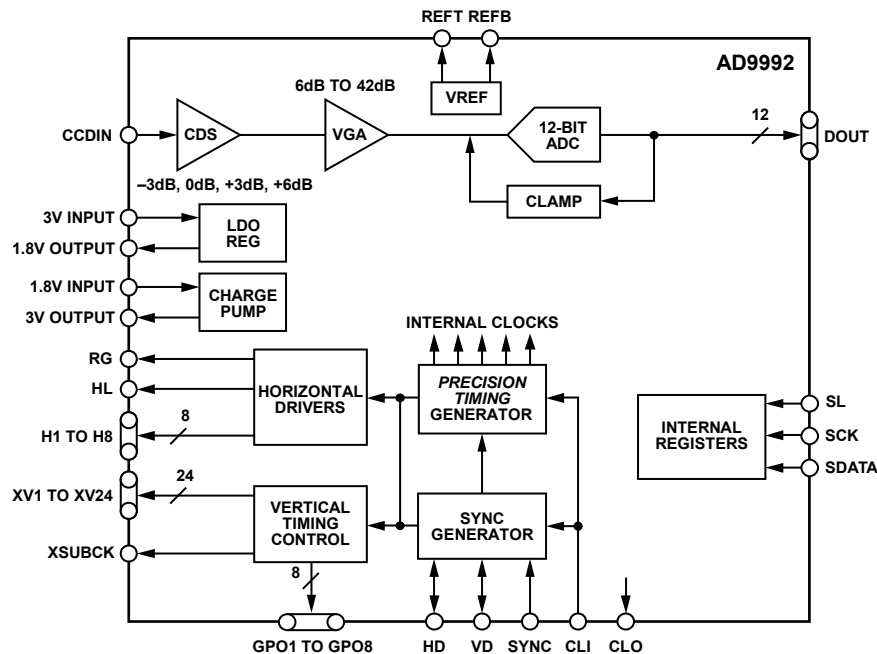


Figure 1.

Rev. 0

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REVISION HISTORY

1/06—Revision 0: Initial Version

SPECIFICATIONS

Table 1.

| Parameter | Min | Typ | Max | Unit |
|--|------|-----|------|------|
| TEMPERATURE RANGE | | | | |
| Operating | -25 | | +85 | °C |
| Storage | -65 | | +150 | °C |
| POWER SUPPLY VOLTAGE INPUTS | | | | |
| AVDD (AFE Analog Supply) | 1.6 | 1.8 | 2.0 | V |
| TCVDD (Timing Core Supply) | 1.6 | 1.8 | 2.0 | V |
| CLIVDD (CLI Input Supply) | 1.6 | 3.0 | 3.6 | V |
| RGVDD (RG, HL Driver) | 2.7 | 3.0 | 3.6 | V |
| HVDD (H1 to H8 Drivers) | 2.7 | 3.0 | 3.6 | V |
| DVDD (Digital Logic) | 1.6 | 1.8 | 2.0 | V |
| DRVDD (Parallel Data Output Drivers) | 1.6 | 3.0 | 3.6 | V |
| IOVDD (Digital I/O) | 1.6 | 3.0 | 3.6 | V |
| XVDD (Vertical Output Drivers) | 1.6 | 3.0 | 3.6 | V |
| CP1P8 (CP Supply Input) | 1.6 | 1.8 | 2.0 | V |
| LDOIN (LDO Supply Input) | 2.25 | 3.0 | 3.6 | V |
| POWER SUPPLY CURRENTS—40 MHz OPERATION | | | | |
| AVDD (1.8 V) | | 27 | | mA |
| TCVDD (1.8 V) | | 5 | | mA |
| CLIVDD (3 V) | | 1.5 | | mA |
| RGVDD (3.3 V, 20 pF RG Load, 20 pF HL Load) | | 10 | | mA |
| HVDD ¹ (3.3 V, 480 pF Total Load on H1 to H8) | | 59 | | mA |
| DVDD (1.8 V) | | 9.5 | | mA |
| DRVDD (3 V, 10 pF Load on Each DOUT Pin) | | 6 | | mA |
| IOVDD (3 V, Depends on Load and Output Frequency of Digital I/O) | | 2 | | mA |
| XVDD (3 V, Depends on Load and Output Frequency of XV Signals) | | 2 | | mA |
| POWER SUPPLY CURRENTS—STANDBY MODE OPERATION | | | | |
| Standby1 Mode | | 12 | | mA |
| Standby2 Mode | | 5 | | mA |
| Standby3 Mode | | 1.5 | | mA |
| MAXIMUM CLOCK RATE (CLI) | 40 | | | MHz |

¹ The total power dissipated by the HVDD (or RGVDD) supply can be approximated using the equation

$$\text{Total HVDD Power} = [C_L \times \text{HVDD} \times \text{Pixel Frequency}] \times \text{HVDD}$$

Reducing the capacitive load and/or reducing the HVDD supply reduces the power dissipation. C_L is the total capacitance seen by all H-outputs.

AD9992

DIGITAL SPECIFICATIONS

IOVDD = 1.6 V to 3.6 V, RGVDD = HVDD = 2.7 V to 3.6 V, $C_L = 20$ pF, T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|----------|----------------|-----|-----|---------|
| LOGIC INPUTS (IOVDD) | | | | | |
| High Level Input Voltage | V_{IH} | $V_{DD} - 0.6$ | | | V |
| Low Level Input Voltage | V_{IL} | | | 0.6 | V |
| High Level Input Current | I_{IH} | | 10 | | μ A |
| Low Level Input Current | I_{IL} | | 10 | | μ A |
| Input Capacitance | C_{IN} | | 10 | | pF |
| LOGIC OUTPUTS (IOVDD, XVDD) | | | | | |
| High Level Output Voltage @ $I_{OH} = 2$ mA | V_{OH} | $V_{DD} - 0.5$ | | | V |
| Low Level Output Voltage @ $I_{OL} = 2$ mA | V_{OL} | | | 0.5 | V |
| RG and H-DRIVER OUTPUTS (HVDD, RGVDD) | | | | | |
| High Level Output Voltage @ Maximum Current | V_{OH} | $V_{DD} - 0.5$ | | | V |
| Low Level Output Voltage @ Maximum Current | V_{OL} | | | 0.5 | V |
| Maximum Output Current (Programmable) | | 18 | | | mA |
| Maximum Load Capacitance (for Each Output) | | 60 | | | pF |

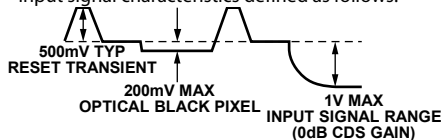
ANALOG SPECIFICATIONS

AVDD = 1.8 V, f_{CL1} = 40 MHz, typical timing specifications, T_{MIN} to T_{MAX} , unless otherwise noted.

Table 3.

| Parameter | Min | Typ | Max | Unit | Notes |
|---|------|------------|------|---------|---|
| CDS ¹ | | | | | |
| Allowable CCD Reset Transient | | 0.5 | 1.2 | V | |
| CDS Gain Accuracy | | | | | VGA gain = 6.3 dB (Code 15, default value) |
| –3.0 dB CDS Gain | –3.3 | –2.8 | –2.3 | dB | |
| 0 dB CDS Gain | –0.5 | 0 | +0.5 | dB | |
| +3 dB CDS Gain | 2.4 | 2.9 | 3.4 | dB | |
| +6 dB CDS Gain | 5.0 | 5.5 | 6.0 | dB | |
| Maximum Input Range Before Saturation | | | | | VGA gain = 6.3 dB (Code 15, default value) |
| –3 dB CDS Gain | | 1.4 | | V p-p | |
| 0 dB CDS Gain | | 1.0 | | V p-p | |
| +3 dB CDS Gain | | 0.7 | | V p-p | |
| +6 dB CDS Gain | | 0.5 | | V p-p | |
| Allowable OB Pixel Amplitude ¹ | | | | | |
| 0 dB CDS Gain (Default) | –100 | | +200 | mV | |
| +6 dB CDS Gain | –50 | | +100 | mV | |
| VARIABLE GAIN AMPLIFIER (VGA) | | | | | |
| Gain Control Resolution | | 1024 | | Steps | |
| Gain Monotonicity | | Guaranteed | | | |
| Gain Range | | | | | |
| Low Gain (VGA Code 15, Default) | | 6.3 | | dB | |
| Maximum Gain (VGA Code 1023) | | 42.4 | | dB | |
| BLACK LEVEL CLAMP | | | | | |
| Clamp Level Resolution | | 1024 | | Steps | |
| Clamp Level | | | | | Measured at ADC output |
| Minimum Clamp Level (Code 0) | | 0 | | LSB | |
| Maximum Clamp Level (Code 1023) | | 255 | | LSB | |
| ADC | | | | | |
| Resolution | 12 | | | Bits | |
| Differential Nonlinearity (DNL) | –1.0 | ±0.5 | +1.0 | LSB | |
| No Missing Codes | | Guaranteed | | | |
| Integral Nonlinearity (INL) | | 1 | 4 | LSB | |
| Full-Scale Input Voltage | | 2.0 | | V | |
| VOLTAGE REFERENCE | | | | | |
| Reference Top Voltage (REFT) | | 1.4 | | V | |
| Reference Bottom Voltage (REFB) | | 0.4 | | V | |
| SYSTEM PERFORMANCE | | | | | |
| Gain Accuracy | | | | | Includes entire signal chain 0 dB CDS gain |
| Low Gain (VGA Code 15) | 5.8 | 6.3 | 6.8 | dB | Gain = (0.0358 × Code) + 5.76 dB |
| Maximum Gain (VGA Code 1023) | 41.9 | 42.4 | 42.9 | dB | |
| Peak Nonlinearity, 1.0 V Input Signal | | 0.1 | 0.2 | % | 6 dB VGA gain, 0 dB CDS gain applied |
| Total Output Noise | | 0.5 | | LSB rms | AC-grounded input, 6 dB VGA gain applied |
| Power Supply Rejection (PSR) | | 50 | | dB | Measured with step change on supply |

¹ Input signal characteristics defined as follows:



06991-002

AD9992

TIMING SPECIFICATIONS

$C_L = 20$ pF, $AVDD = DVDD = TCVD = 1.8$ V, $DRVDD = 3.0$ V, $f_{CLI} = 40$ MHz, unless otherwise noted.

Table 4.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|---------------|------------|------|---------------------------------|---------------|
| MASTER CLOCK (See Figure 14) | | | | | |
| CLI Clock Period | t_{CONV} | 25 | | | ns |
| CLI High/Low Pulse Width | | 10 | 12.5 | 15 | ns |
| Delay from CLI Rising Edge to Internal Pixel Position 0 | t_{CLIDL} | | 6 | | ns |
| VD FALLING EDGE TO HD FALLING EDGE IN SLAVE MODE (See Figure 75) | t_{VDHD} | 0 | | VD period – $5 \times t_{CONV}$ | ns |
| AFE CLPOB PULSE WIDTH (See Figure 21 and Figure 31) ^{1,2} | | 2 | 20 | | Pixels |
| AFE SAMPLE LOCATION (See Figure 15 and Figure 18) ¹ | | | | | |
| SHP Sample Edge to SHD Sample Edge | t_{S1} | 11 | 12.5 | | ns |
| DATA OUTPUTS (See Figure 19 and Figure 20) | | | | | |
| Output Delay from DCLK Rising Edge | t_{OD} | | 1 | | ns |
| Inhibited Area for DOUTPHASE Edge Location | $t_{DOUTINH}$ | SHDLOC + 1 | | SHDLOC + 15 | Edge location |
| Pipeline Delay from SHP/SHD Sampling to DOUT | | | 16 | | Cycles |
| SERIAL INTERFACE (See Figure 82) | | | | | |
| Maximum SCK Frequency (Must Not Exceed CLI Frequency) | f_{SCLK} | 40 | | | MHz |
| SL to SCK Setup Time | t_{LS} | 10 | | | ns |
| SCK to SL Hold Time | t_{LH} | 10 | | | ns |
| SDATA Valid to SCK Rising Edge Setup | t_{DS} | 10 | | | ns |
| SCK Falling Edge to SDATA Valid Hold | t_{DH} | 10 | | | ns |

¹ Parameter is programmable.

² Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.

ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | With Respect To | Rating |
|-----------------------------|-----------------|-------------------------|
| AVDD | AVSS | -0.3 V to +2.0 V |
| TCVDD | TCVSS | -0.3 V to +2.0 V |
| HVDD | HVSS | -0.3 V to +3.9 V |
| RGVDD | RGVSS | -0.3 V to +3.9 V |
| DVDD | DVSS | -0.3 V to +2.0 V |
| DRVDD | DRVSS | -0.3 V to +3.9 V |
| IOVDD | DVSS | -0.3 V to +3.9 V |
| XVVDD | DVSS | -0.3 V to +3.9 V |
| CLIVDD | TCVSS | -0.3 V to +3.9 V |
| CP1P8 | CPVSS | -0.3 V to +2.0 V |
| RG Output | RGVSS | -0.3 V to RGVDD + 0.3 V |
| H1 to H8, HL Output | HVSS | -0.3 V to HVDD + 0.3 V |
| Digital Outputs | DVSS | -0.3 V to IOVDD + 0.3 V |
| Digital Inputs | DVSS | -0.3 V to IOVDD + 0.3 V |
| SCK, SL, SDATA | DVSS | -0.3 V to IOVDD + 0.3 V |
| REFT, REFB, CCDIN | AVSS | -0.3 V to AVDD + 0.3 V |
| Junction Temperature | | 150°C |
| Lead Temperature, 10 sec | | 350°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS

Thermal Resistance

CSP_BGA package: $\theta_{JA} = 40.3^{\circ}\text{C}/\text{W}$

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

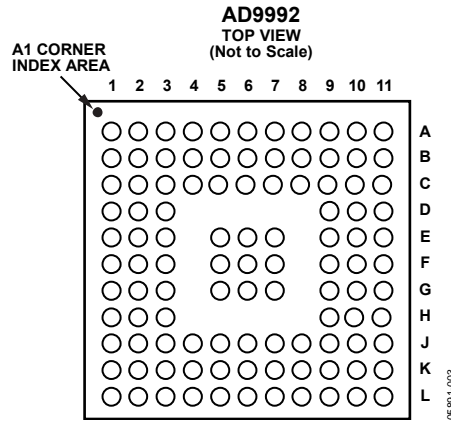


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

| Pin No. | Mnemonic | Type | Description | Pin No. | Mnemonic | Type | Description |
|---------|----------|------|--|---------|----------|------|-----------------------------|
| A1 | GPO8 | DIO | General-Purpose Output 8 | H2 | XV11 | DO | CCD Vertical Clock 11 |
| B2 | GPO7 | DIO | General-Purpose Output 7 | H1 | XV12 | DO | CCD Vertical Clock 12 |
| C2 | GPO6 | DIO | General-Purpose Output 6 | G6 | XV13 | DO | CCD Vertical Clock 13 |
| B1 | GPO5 | DIO | General-Purpose Output 5 | G7 | XV14 | DO | CCD Vertical Clock 14 |
| B4 | GPO4 | DIO | General-Purpose Output 4 | J2 | XV15 | DO | CCD Vertical Clock 15 |
| C1 | GPO3 | DIO | General-Purpose Output 3 | J1 | XV16 | DO | CCD Vertical Clock 16 |
| D2 | GPO2 | DIO | General-Purpose Output 2 | L1 | XV17 | DO | CCD Vertical Clock 17 |
| C3 | GPO1 | DIO | General-Purpose Output 1 | L2 | XV18 | DO | CCD Vertical Clock 18 |
| D3 | SYNC | DI | External System Sync Input | L3 | XV19 | DO | CCD Vertical Clock 19 |
| E2 | VD | DIO | Vertical Sync Pulse (input for slave mode, output for master mode) | K1 | XV20 | DO | CCD Vertical Clock 20 |
| D1 | HD | DIO | Horizontal Sync Pulse (input for slave mode, output for master mode) | K2 | XV21 | DO | CCD Vertical Clock 21 |
| E7 | RSTB | DI | External Reset Input (active low pulse to reset, internal pull-up resistor) | K3 | XV22 | DO | CCD Vertical Clock 22 |
| E6 | IOVDD | P | Digital I/O Supply: 1.8 V, 3.3 V (GPO, SUBCK, HD/VD, SL, SCK, SDATA, SYNC, RSTB) | J3 | XV23 | DO | CCD Vertical Clock 23 |
| E5 | IOVSS | P | Digital I/O Ground | H3 | XV24 | DO | CCD Vertical Clock 24 |
| E3 | XVVDD | P | XV Output Supply: 1.8 V, 3.3 V | L4 | DVDD | P | Digital Logic Supply: 1.8 V |
| E1 | XSUBCK | DO | CCD Substrate Clock | K4 | DVSS | P | Digital Logic Ground |
| F2 | XV1 | DO | CCD Vertical Clock 1 | K5 | NC | | Not Internally Connected |
| F3 | XV2 | DO | CCD Vertical Clock 2 | J5 | NC | | Not Internally Connected |
| F7 | XV3 | DO | CCD Vertical Clock 3 | L6 | D0 | DO | Data Output 0 (LSB) |
| G3 | XV4 | DO | CCD Vertical Clock 4 | K6 | D1 | DO | Data Output 1 |
| F5 | XV5 | DO | CCD Vertical Clock 5 | J6 | D2 | DO | Data Output 2 |
| F6 | XV6 | DO | CCD Vertical Clock 6 | L7 | D3 | DO | Data Output 3 |
| G2 | XV7 | DO | CCD Vertical Clock 7 | K7 | D4 | DO | Data Output 4 |
| F1 | XV8 | DO | CCD Vertical Clock 8 | J7 | D5 | DO | Data Output 5 |
| G1 | XV9 | DO | CCD Vertical Clock 9 | L8 | D6 | DO | Data Output 6 |
| G5 | XV10 | DO | CCD Vertical Clock 10 | K8 | D7 | DO | Data Output 7 |
| | | | | J8 | D8 | DO | Data Output 8 |
| | | | | L9 | D9 | DO | Data Output 9 |
| | | | | K9 | D10 | DO | Data Output 10 |
| | | | | J9 | D11 | DO | Data Output 11 (MSB) |
| | | | | L10 | DCLK | DO | Data Clock Output |
| | | | | K10 | DRVSS | P | Data Driver Ground |

| Pin No. | Mnemonic | Type | Description |
|---------|----------|------|-------------------------------------|
| L11 | DRVDD | P | Data Driver Supply: 1.8V, 3.3V |
| K11 | CP3P3 | P | Charge Pump 3.3 V Output |
| J10 | CPFCT | AO | Charge Pump Flying Capacitor Top |
| J11 | CPFCB | AO | Charge Pump Flying Capacitor Bottom |
| H10 | CPVSS | P | Charge Pump Ground |
| H11 | CP1P8 | P | Charge Pump 1.8 V Input |
| H9 | CPCLI | DI | Charge Pump Clock Input |
| G11 | LDO3P2EN | DI | LDO 3.2 V Output Enable |
| G9 | LDOVSS | P | LDO Ground |
| F10 | LDO1P8EN | DI | LDO 1.8 V Output Enable |
| F11 | SENSE | AI | LDO Output Sense Pin |
| E11 | LDOOUT | AO | LDO Output Voltage |
| E10 | LDOIN | P | LDO 3.3 V Input |
| F9 | H1 | DO | CCD Horizontal Clock 1 |
| E9 | H2 | DO | CCD Horizontal Clock 2 |
| D11 | HVSS1 | P | H-Driver Ground 1 |
| C11 | HVDD1 | P | H-Driver Supply 1: 3.3 V |
| D10 | H3 | DO | CCD Horizontal Clock 3 |
| C10 | H4 | DO | CCD Horizontal Clock 4 |
| D9 | H5 | DO | CCD Horizontal Clock 5 |
| C9 | H6 | DO | CCD Horizontal Clock 6 |
| B11 | HVSS2 | P | H-Driver Ground 2 |
| A11 | HVDD2 | P | H-Driver Supply 2: 3.3 V |
| B10 | H7 | DO | CCD Horizontal Clock 7 |

| Pin No. | Mnemonic | Type | Description |
|-----------------|----------|------|--|
| A10 | H8 | DO | CCD Horizontal Clock 8 |
| B9 | HL | DO | CCD Last Horizontal Clock |
| B8 | RGVSS | P | RG Driver Ground |
| A8 | RGVDD | P | RG Driver Supply: 3.3 V |
| C8 | RG | DO | CCD Reset Gate Clock |
| B7 | TCVSS | P | Analog Ground for Timing Core |
| A7 | TCVDD | P | Timing Core Supply: 1.8 V |
| C7 | CLIVDD | P | CLI Input Supply: 3.3V |
| C6 | CLO | DO | Clock Output for Crystal |
| C5 | CLI | DI | Reference Clock Input |
| B6 | AVDD | P | AFE Supply: 1.8 V |
| A6 | CCDIN | AI | CCD Signal Input |
| B5, A5 | AVSS | P | Analog Supply Ground |
| A4 | REFT | AO | Voltage Reference Top Bypass |
| A3 | REFB | AO | Voltage Reference Bottom Bypass |
| C4 | SL | DI | 3-Wire Serial Load Pulse (internal pull-up resistor) |
| A2 | SDATA | DI | 3-Wire Serial Data Input |
| B3 | SCK | DI | 3-Wire Serial Clock |
| A9, G10, J4, L5 | NC | | Not Internally Connected |

TERMINOLOGY

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes must be present over all operating conditions.

Peak Nonlinearity

Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9992 from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1 LSB and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.

Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage using the relationship

$$1 \text{ LSB} = (\text{ADC Full Scale} / 2^n \text{ Codes})$$

where n is the bit resolution of the ADC. For the AD9992, 1 LSB is 0.488 mV.

Power Supply Rejection (PSR)

The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

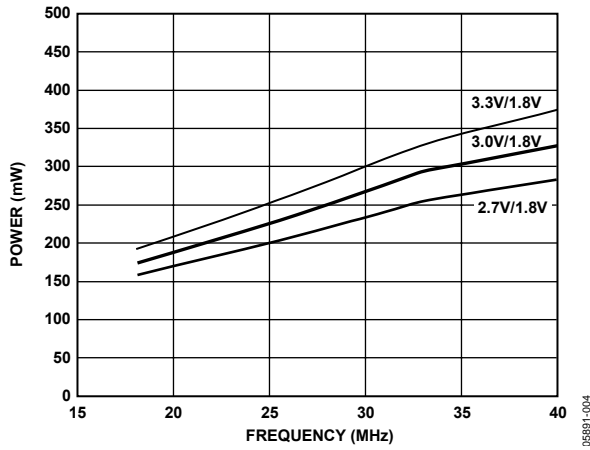


Figure 3. Power vs. Frequency
 (AVDD = TCVDD = DVDD = 1.8 V, All Other Supplies at 2.7 V, 3.0 V, or 3.3 V)

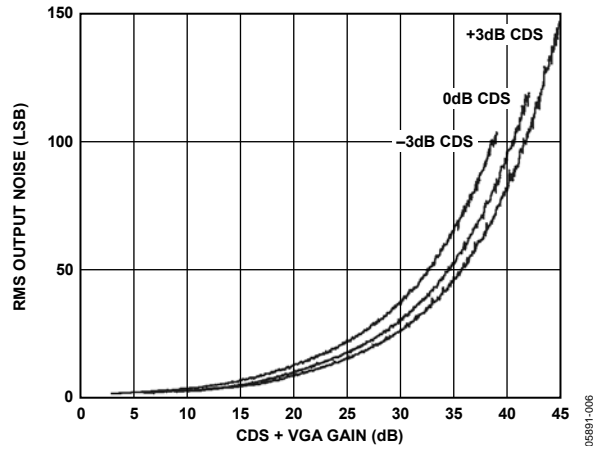


Figure 5. Output Noise vs. Total Gain (CDS + VGA)

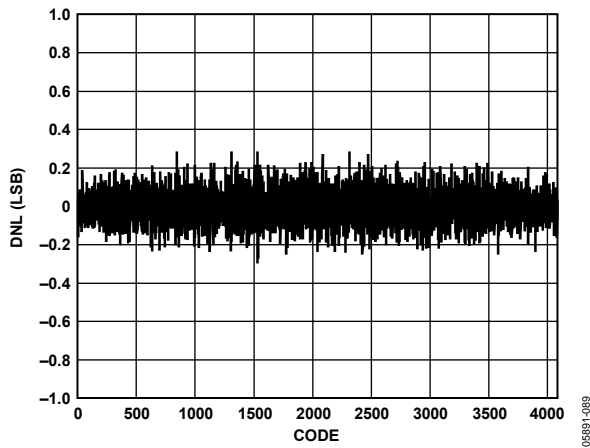


Figure 4. Typical Differential Nonlinearity (DNL) Performance

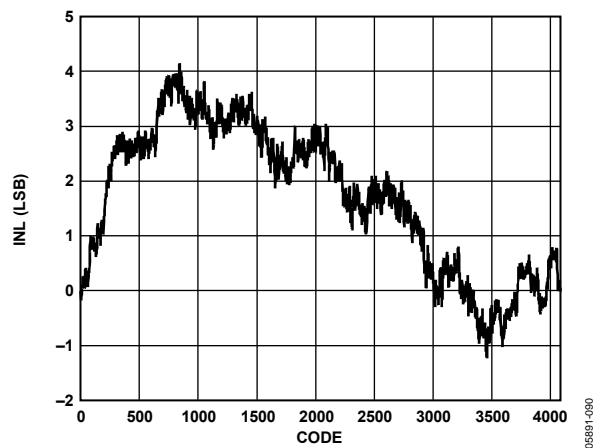


Figure 6. Typical Integral Nonlinearity (INL) Performance

EQUIVALENT CIRCUITS

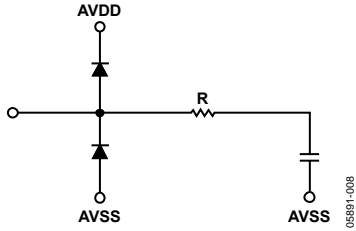


Figure 7. CCDIN

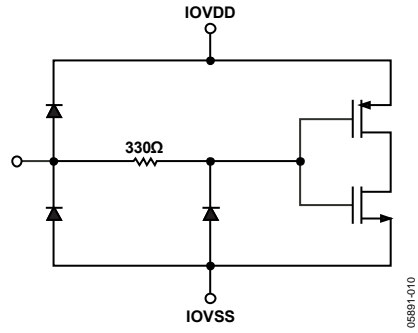


Figure 9. Digital Inputs

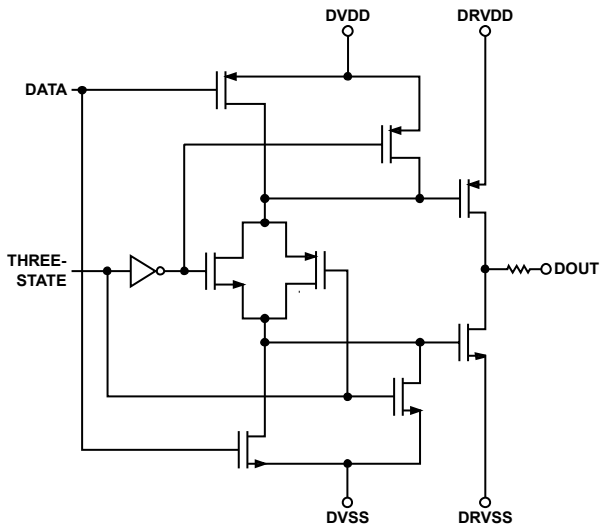


Figure 8. Digital Data Outputs

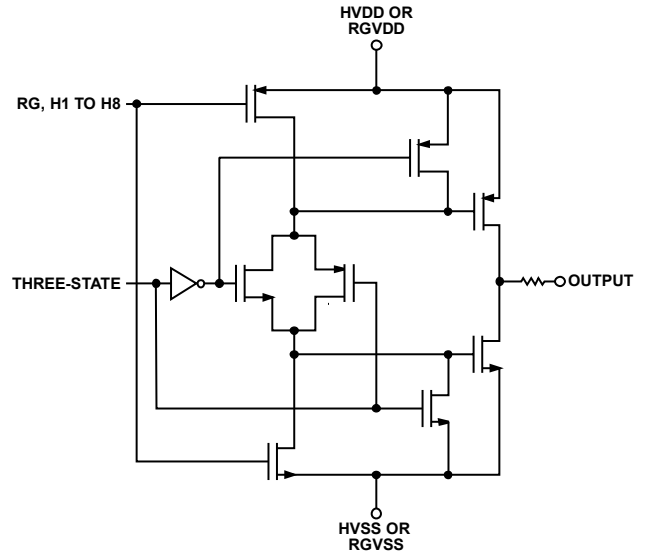


Figure 10. H1 to H8, HL, RG Drivers

SYSTEM OVERVIEW

Figure 11 shows the typical system block diagram for the AD9992 in master mode. The CCD output is processed by the AD9992's AFE circuitry, which consists of a CDS, VGA, black level clamp, and ADC. The digitized pixel information is sent to the digital image processor chip, which performs the postprocessing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9992 from the system microprocessor through the 3-wire serial interface. From the master clock, CLI, provided by the image processor or external crystal, the AD9992 generates the CCD's horizontal and vertical clocks and internal AFE clocks. External synchronization is provided by a sync pulse from the microprocessor, which resets the internal counters and resyncs the VD and HD outputs.

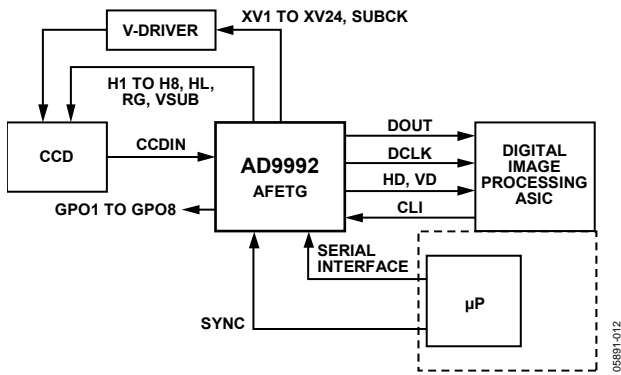


Figure 11. Typical System Block Diagram, Master Mode

Alternatively, the AD9992 can be operated in slave mode. In this mode, the VD and HD are provided externally from the image processor, and all AD9992 timing is synchronized with VD and HD.

The H-drivers for H1 to H8, HL, and RG are included in the AD9992, allowing these clocks to be directly connected to the CCD. An H-driver voltage of up to 3.3 V is supported. An external V-driver is required for the vertical transfer clocks, the sensor gate pulses, and the substrate clock.

The AD9992 includes programmable general-purpose outputs (GPO), which can trigger mechanical shutter and strobe (flash) circuitry.

Figure 12 and Figure 13 show the maximum horizontal and vertical counter dimensions for the AD9992. All internal horizontal and vertical clocking is controlled by these counters, which specify line and pixel locations. Maximum HD length is 8192 pixels per line, and maximum VD length is 8192 lines per field.

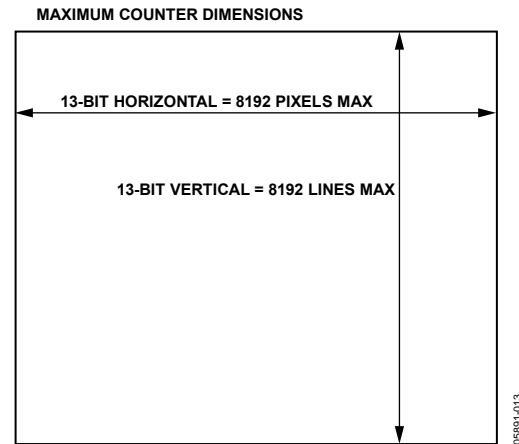


Figure 12. Vertical and Horizontal Counters

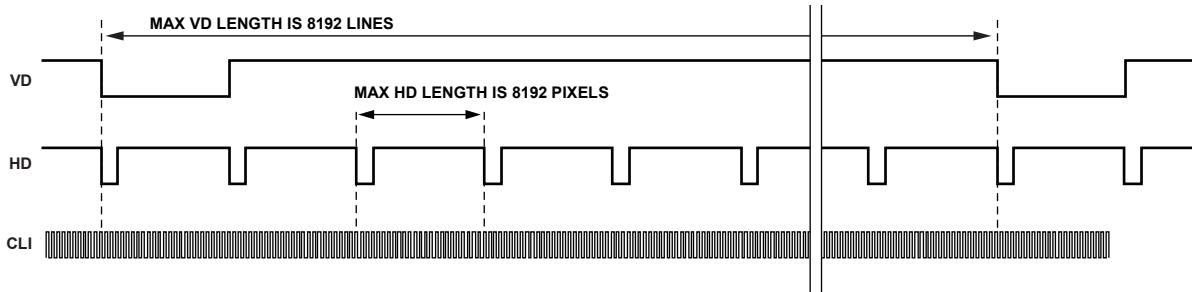


Figure 13. Maximum VD/HD Dimensions

HIGH SPEED PRECISION TIMING CORE

The AD9992 generates high speed timing signals using the flexible *Precision Timing* core. This core is the foundation for generating the timing used for both the CCD and the AFE; it includes the reset gate RG, horizontal drivers H1 to H8, HL, and SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

The high speed timing of the AD9992 operates the same way in either master or slave mode configuration. For more information on synchronization and pipeline delays, see the Power-Up Sequence for Master Mode section.

Timing Resolution

The *Precision Timing* core uses a 1× master clock input as a reference (CLI). This clock should be the same as the CCD pixel clock frequency. Figure 14 illustrates how the internal timing core divides the master clock period into 64 steps or edge positions. Using a 40 MHz CLI frequency, the edge resolution of the *Precision Timing* core is approximately 0.4 ns. If a 1× system clock is not available, it is possible to use a 2× reference

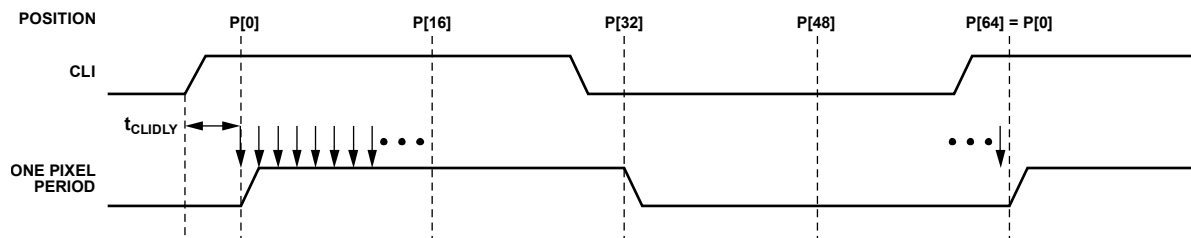
clock by programming the CLIDIVIDE register (AFE Register Address 0x0D). The AD9992 then internally divides the CLI frequency by 2.

The AD9992 includes a master clock output, CLO, which is the inverse of CLI. This output should be used as a crystal driver. A crystal can be placed between the CLI and CLO pins to generate the master clock for the AD9992.

High Speed Clock Programmability

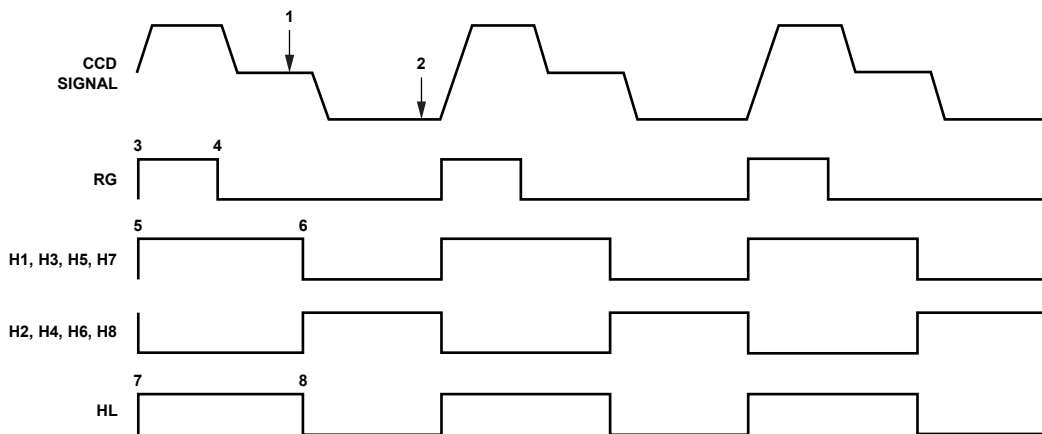
Figure 15 shows when the high speed clocks RG, H1 to H8, SHP, and SHD are generated. The RG pulse has programmable rising and falling edges and can be inverted using the polarity control. Horizontal Clock H1 has programmable rising and falling edges and polarity control. In HCLK Mode 1, H3, H5, and H7 are equal to H1 and H2, H4, H6, and H8 are always inverses of H1.

The edge location registers are each six bits wide, allowing the selection of all 64 edge locations. Figure 18 shows the default timing locations for all of the high speed clock signals.



- NOTES
1. THE PIXEL CLOCK PERIOD IS DIVIDED INTO 64 POSITIONS, PROVIDING FINE EDGE RESOLUTION FOR HIGH SPEED CLOCKS.
 2. THERE IS A FIXED DELAY FROM THE CLI INPUT TO THE INTERNAL PIXEL PERIOD POSITION (t_{CLIDLY}).

Figure 14. High Speed Clock Resolution from CLI, Master Clock Input



- PROGRAMMABLE CLOCK POSITIONS:
- 1SHP SAMPLE LOCATION.
 - 2SHD SAMPLE LOCATION.
 - 3RG RISING EDGE.
 - 4RG FALLING EDGE.
 - 5H1 RISING EDGE.
 - 6H1 FALLING EDGE.
 - 7HL RISING EDGE.
 - 8HL FALLING EDGE.

Figure 15. High Speed Clock Programmable Locations (HCLKMODE = 001)

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9992 features on-chip output drivers for the RG, HL, and H1 to H8 outputs. These drivers are powerful enough to drive the CCD inputs directly. The H-driver and RG current can be adjusted for optimum rise/fall time for a particular load by using the drive strength control registers (Addresses 0x35 and 0x36). The 3-bit drive setting for each output is adjustable in 4.3 mA increments: 0 = three-state; 1 = 4.3 mA; 2 = 8.6 mA; 3 = 12.9 mA; and 4, 5, 6, 7 = 17.2 mA.

As shown in Figure 15, when HCLK Mode 1 is used, the H2, H4, H6, and H8 outputs are inverses of the H1, H3, H5, and H7 outputs, respectively. Using the HCLKMODE register (Address 0x23, Bits [9:7]), it is possible to select a different configuration. Table 8 shows a comparison of the different programmable settings for each HCLK mode. Figure 16 and Figure 17 show the settings for HCLK Mode 2 and HCLK Mode 3, respectively.

Note that it is recommended that all H1 to H8 outputs on the AD9992 be used together for maximum flexibility in drive strength settings. A typical CCD with H1 and H2 inputs should only have the AD9992's H1, H3, H5, and H7 outputs connected together to drive the CCD's H1, and the H2, H4, H6, and H8 outputs connected together to drive the CCD's H2. Similarly, a CCD with H1, H2, H3, and H4 inputs should have

- H1 and H3 connected to the CCD's H1.
- H2 and H4 connected to the CCD's H2.
- H5 and H7 connected to the CCD's H3.
- H6 and H8 connected to the CCD's H4.

Table 7. Timing Core Register Parameters for H1, H2, HL, RG, SHP, SHD

| Parameter | Length | Range | Description |
|-------------------|--------|-----------------------|---|
| Polarity | 1b | High/low | Polarity control for H1, H2, HL, and RG (0 = inversion, 1 = no inversion) |
| Positive Edge | 6b | 0 to 63 edge location | Positive edge location for H1, H2, HL, and RG |
| Negative Edge | 6b | 0 to 63 edge location | Negative edge location for H1, H2, HL, and RG |
| Sampling Location | 6b | 0 to 63 edge location | Sampling location for internal SHP and SHD signals |
| Drive Strength | 3b | 0 to 4 current steps | Drive current for H1 to H8 , HL, and RG outputs (4.3 mA per step) |

Table 8. HCLK Modes, Selected by Address 0x23, Bits [9:7]

| HCLKMODE | Register Value | Description |
|-------------------|-------------------------|--|
| Mode 1 | 001 | H1 edges are programmable, with H3 = H5 = H7 = H1, H2 = H4 = H6 = H8 = inverse of H1 |
| Mode 2 | 010 | H1 edges are programmable, with H3 = H5 = H7 = H1 H2 edges are programmable, with H4 = H6 = H8 = H2 |
| Mode 3 | 100 | H1 edges are programmable, with H3 = H1 and H2 = H4 = inverse of H1 H5 edges are programmable, with H7 = H5 and H6 = H8 = inverse of H5 |
| Invalid Selection | 000, 011, 101, 110, 111 | Invalid register settings |

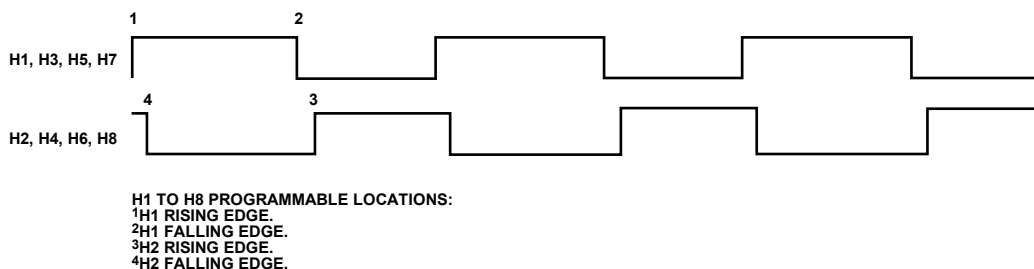
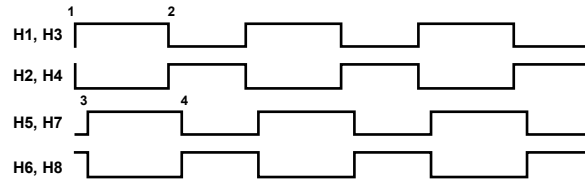


Figure 16. HCLK Mode 2 Operation

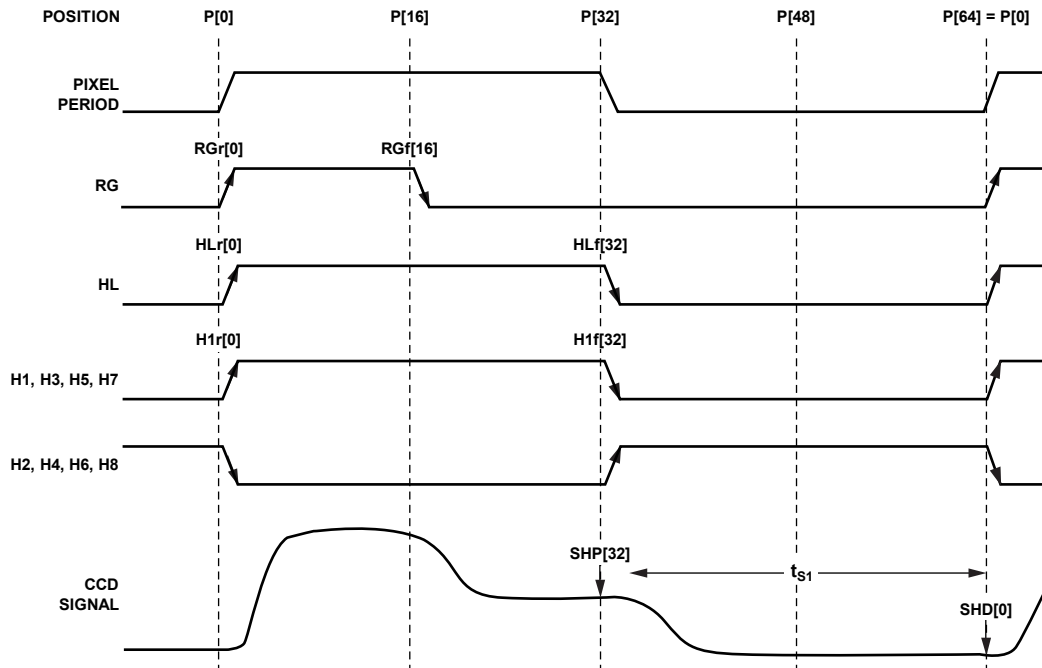
06891-017



H1 TO H8 PROGRAMMABLE EDGES:
 1 H1 RISING EDGE.
 2 H1 FALLING EDGE.
 3 H5 RISING EDGE.
 4 H5 FALLING EDGE.

05881-018

Figure 17. HCLK Mode 3 Operation



NOTES

1. ALL SIGNAL EDGES ARE FULLY PROGRAMMABLE TO ANY OF THE 64 POSITIONS WITHIN ONE PIXEL PERIOD. DEFAULT POSITIONS FOR EACH SIGNAL ARE SHOWN. HCLK MODE 1 IS SHOWN.
2. CONNECT H1, H3, H5, AND H7 TOGETHER AND H2, H4, H6, AND H8 TOGETHER FOR MAXIMUM DRIVE STRENGTH.

05881-019

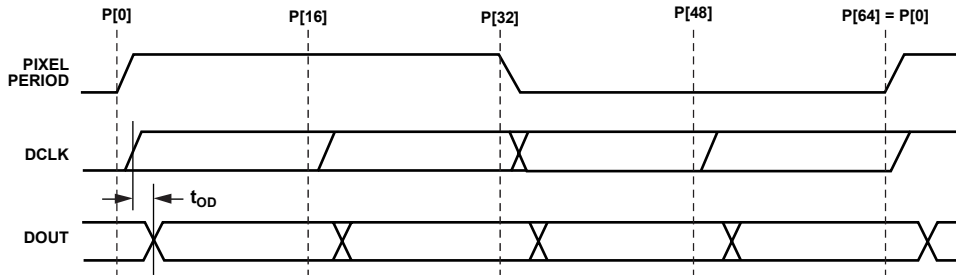
Figure 18. High Speed Timing Default Locations

Digital Data Outputs

The AD9992 data output and DCLK phase are programmable using the DOUTPHASE registers (Address 0x38, Bits [11:0]). DOUTPHASEP (Bits [5:0]) selects any edge location from 0 to 63, as shown in Figure 19. DOUTPHASEN (Bits [11:6]) does not actually program the phase of the data outputs but is used internally and should always be programmed to a value of DOUTPHASEP plus 32 edges. For example, if DOUTPHASEP is set to 0, DOUTPHASEN should be set to 32 (0x20).

Normally, the DOUT and DCLK signals track in phase, based on the contents of the DOUTPHASE registers. The DCLK output phase can also be held fixed with respect to the data outputs by changing the DCLKMODE register high (Address 0x38, Bit [12]). In this mode, the DCLK output remains at a fixed phase equal to a delayed version of CLI while the data output phase is still programmable.

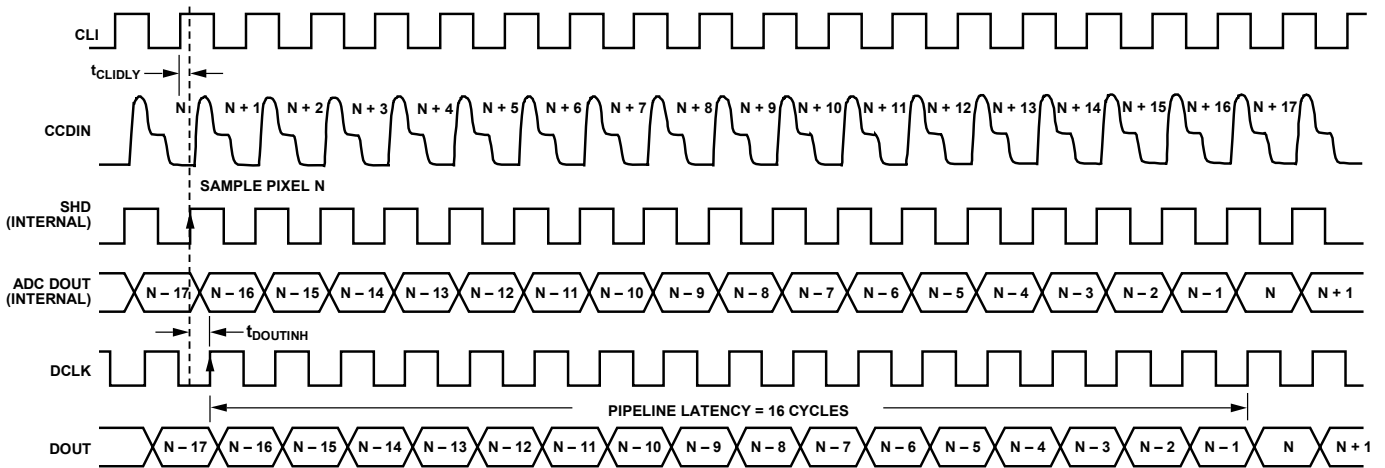
The pipeline delay through the AD9992 is shown in Figure 20. After the CCD input is sampled by SHD, there is a 16-cycle delay until the data is available.



- NOTES**
1. DATA OUTPUT (DOUT) AND DCLK PHASE ARE ADJUSTABLE WITH RESPECT TO THE PIXEL PERIOD.
 2. WITHIN ONE CLOCK PERIOD, THE DATA TRANSITION CAN BE PROGRAMMED TO 64 DIFFERENT LOCATIONS.
 3. DCLK CAN BE INVERTED WITH RESPECT TO DOUT BY USING THE DCLKINV REGISTER.

056891-020

Figure 19. Digital Output Phase Adjustment Using DOUTPHASEP Register



- NOTES**
1. TIMING VALUES SHOWN ARE SHDLOC = 0, WITH DCLKMODE = 0.
 2. HIGHER VALUES OF SHD AND/OR DOUT PHASE SHIFTS DOUT TRANSITION TO THE RIGHT, WITH RESPECT TO CLI LOCATION.
 3. RECOMMENDED VALUE FOR DOUT PHASE IS TO USE SHPLOC OR UP TO 15 EDGES FOLLOWING SHPLOC.

056891-021

Figure 20. Digital Data Output Pipeline Delay

HORIZONTAL CLAMPING AND BLANKING

The AD9992's horizontal clamping and blanking pulses are fully programmable to suit a variety of applications. Individual control is provided for CLPOB, PBLK, and HBLK in the different regions of each field. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout in order to accommodate different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 21. These two signals are programmed independently using the registers in Table 9. The start polarity for the CLPOB (and PBLK) signal is CLPOBPOL (PBLKPOL), and the first and second toggle positions of the pulse are CLPOBTOG1 (PBLKTOG1) and CLPOBTOG2 (PBLKTOG2). Both signals are active low and should be programmed accordingly.

A separate pattern for CLPOB and PBLK can be programmed for each vertical sequence. As described in the Vertical Timing Generation section, several V-sequences can be created, each containing a unique pulse pattern for CLPOB and PBLK. Figure 47 shows how the sequence change positions divide the readout field into different regions. By assigning a different V-sequence to each region, the CLPOB and PBLK signals can change with each change in the vertical timing.

CLPOB and PBLK Masking Areas

Additionally, the AD9992 allows the CLPOB and PBLK signals to be disabled in certain lines in the field without changing any of the existing CLPOB pattern settings.

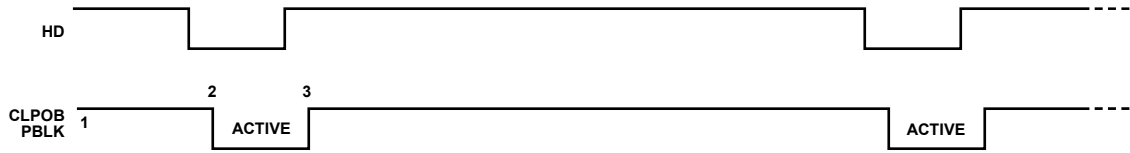
To use CLPOB (or PBLK) masking, the CLPMASKSTART (PBLKMASKSTART) and CLPMASKEND (PBLKMASKEND) registers are programmed to specify the start and end lines in the field where the CLPOB (PBLK) patterns are ignored. The three sets of start and end registers allow up to three CLPOB (PBLK) masking areas to be created.

The CLPOB and PBLK masking registers are not specific to a certain V-sequence; they are always active for any existing field of timing. During operation, to disable the CLPOB masking feature, these registers must be set to the maximum value of 0x1FFF or a value greater than the programmed VD length.

Note that to disable CLPOB (and PBLK) masking during power-up, it is recommended to set CLPMASKSTART (PBLKMASKSTART) to 8191 and CLPMASKEND (PBLKMASKEND) to 0. This prevents any accidental masking caused by register update events.

Table 9. CLPOB and PBLK Pattern Registers

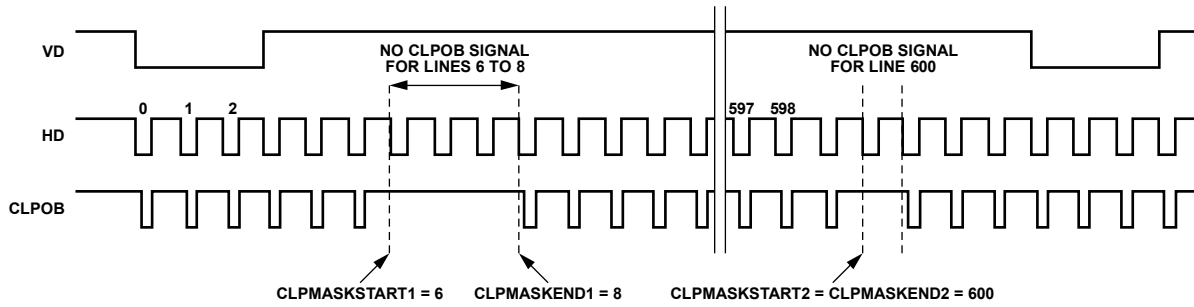
| Register | Length | Range | Description |
|---------------|--------|--------------------------|---|
| CLPOBPOL | 1b | High/low | Starting polarity of CLPOB for each V-sequence. |
| PBLKPOL | 1b | High/low | Starting polarity of PBLK for each V-sequence. |
| CLPOBTOG1 | 13b | 0 to 8191 pixel location | First CLPOB toggle position within line for each V-sequence. |
| CLPOBTOG2 | 13b | 0 to 8191 pixel location | Second CLPOB toggle position within line for each V-sequence. |
| PBLKTOG1 | 13b | 0 to 8191 pixel location | First PBLK toggle position within line for each V-sequence. |
| PBLKTOG2 | 13b | 0 to 8191 pixel location | Second PBLK toggle position within line for each V-sequence. |
| CLPMASKSTART | 13b | 0 to 8191 line location | CLPOB masking area—starting line within field (maximum of three areas). |
| CLPMASKEND | 13b | 0 to 8191 line location | CLPOB masking area—ending line within field (maximum of three areas). |
| PBLKMASKSTART | 13b | 0 to 8191 line location | PBLK masking area—starting line within field (maximum of three areas). |
| PBLKMASKEND | 13b | 0 to 8191 line location | PBLK masking area—ending line within field (maximum of three areas). |



PROGRAMMABLE SETTINGS:
 1 START POLARITY (CLAMP AND BLANK REGION ARE ACTIVE LOW).
 2 FIRST TOGGLE POSITION.
 3 SECOND TOGGLE POSITION.

05891-022

Figure 21. Clamp and Preblank Pulse Placement



05891-023

Figure 22. CLPOB Masking Example

Individual HBLK Patterns

The HBLK programmable timing shown in Figure 23 is similar to CLPOB and PBLK; however, there is no start polarity control. Only the toggle positions are used to designate the start and stop positions of the blanking period. Additionally, there are separate masking polarity controls for H1, H2, and HL that designate the polarity of the horizontal clock signals during the blanking period. Setting HBLKMASK_H1 high sets H1, and therefore H3, H5, and H7, low during the blanking, as shown in Figure 24. As with the CLPOB and PBLK signals, HBLK registers are available in each V-sequence, allowing different blanking signals to be used with different vertical timing sequences.

The AD9992 supports three modes of HBLK operation. HBLK Mode 0 supports basic operation and some support for special HBLK patterns. HBLK Mode 1 supports pixel mixing HBLK

operation. HBLK Mode 2 supports advanced HBLK operation. The following sections describe each mode in detail. Register parameters are described in detail in Table 10.

HBLK Mode 0 Operation

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions can be used to generate special HBLK patterns, as shown in Figure 25. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns can be created.

Separate toggle positions are available for even and odd lines. If alternation is not needed, the same values should be loaded into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

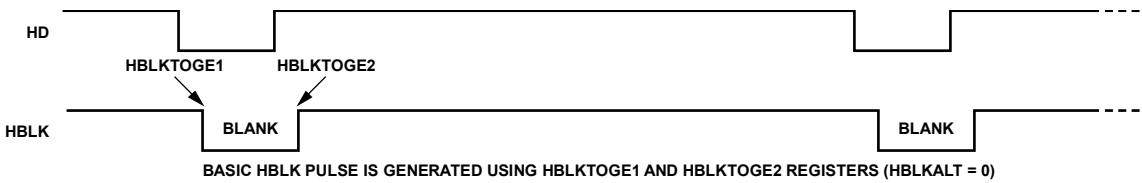


Figure 23. Typical Horizontal Blanking Pulse Placement (HBLKMODE = 0)

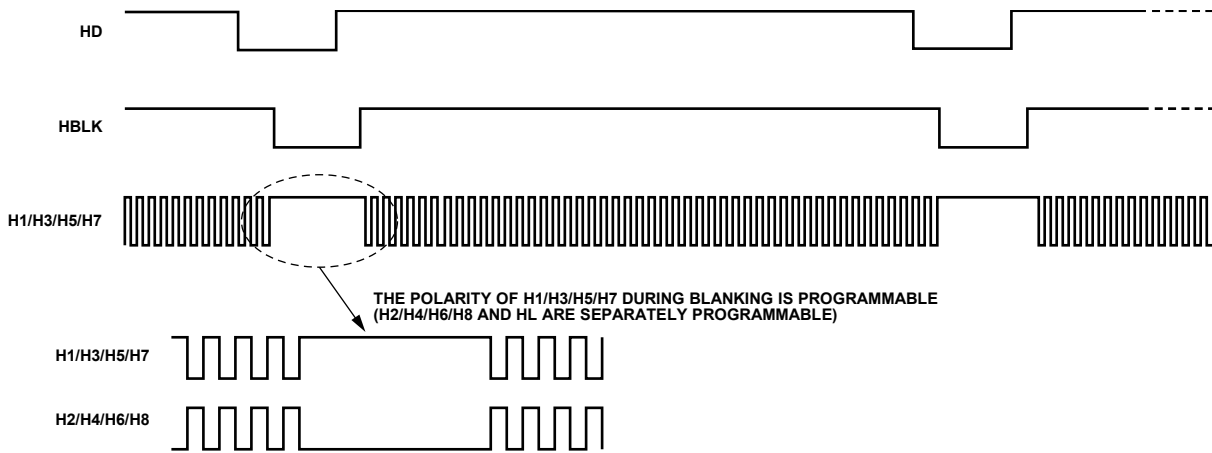


Figure 24. HBLK Masking Polarity Control

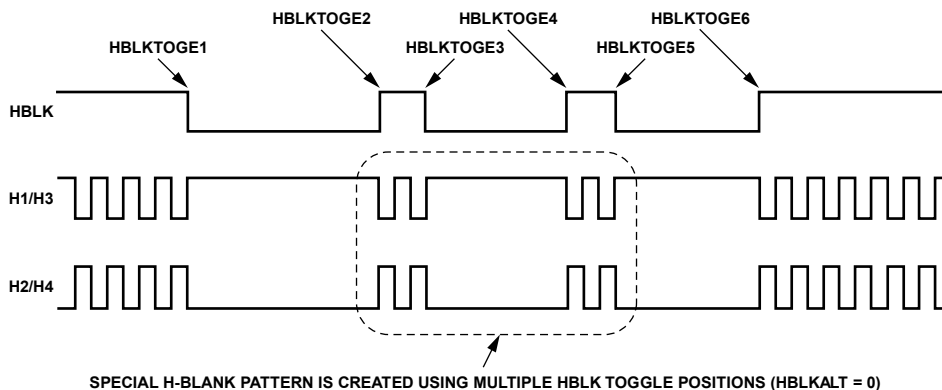
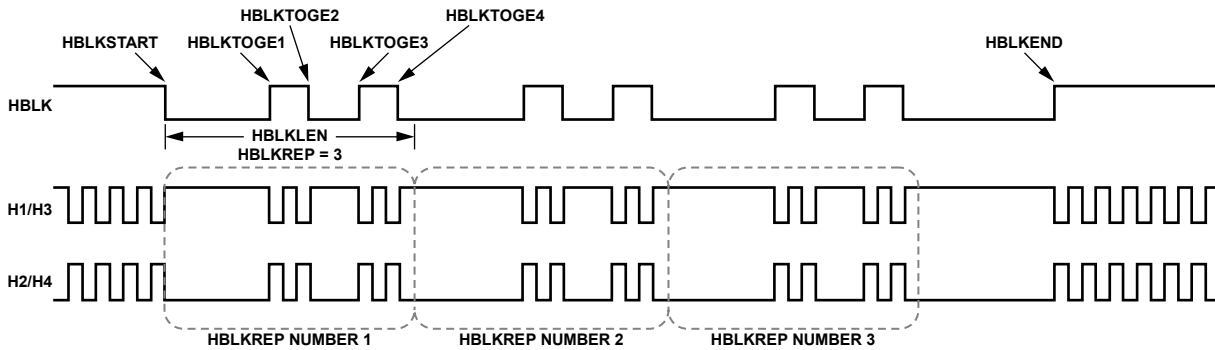


Figure 25. Using Multiple Toggle Positions for HBLK (HBLKMODE = 0)

Table 10. HBLK Pattern Registers

| Register | Length | Range | Description |
|---------------|--------|--|---|
| HBLKMODE | 2b | 0 to 2 HBLK modes | Enables different HBLK toggle position operation. 0: normal mode. Six toggle positions available for even and odd lines. If even/odd alternation is not needed, set toggles for even/odd the same. 1: pixel mixing mode. In addition to the six toggle positions, the HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP registers can be used to generate HBLK patterns. If even/odd alternation is not needed, set toggles for even/odd the same. 2: advanced HBLK mode. Divides HBLK interval into six repeat areas. Uses HBLKSTARTA/B/C and RA*H*REPA/B/C registers. 3: test mode only. Do not access. |
| HBLKSTART | 13b | 0 to 8191 pixel location | Start location for HBLK in HBLK Mode 1 and HBLK Mode 2. |
| HBLKEND | 13b | 0 to 8191 pixel location | End location for HBLK in HBLK Mode 1 and HBLK Mode 2. |
| HBLKLEN | 13b | 0 to 8191 pixels | HBLK length in HBLK Mode 1 and HBLK Mode 2. |
| HBLKREP | 13b | 0 to 8191 repetitions | Number of HBLK repetitions in HBLK Mode 1 and HBLK Mode 2. |
| HBLKMASK_H1 | 1b | High/low | Masking polarity for H1, H3, H5, H7 during HBLK. |
| HBLKMASK_H2 | 1b | High/low | Masking polarity for H2, H4, H6, H8 during HBLK. |
| HBLKMASK_HL | 1b | High/low | Masking polarity for HL during HBLK. |
| HBLKTOGO1 | 13b | 0 to 8191 pixel location | First HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGO2 | 13b | 0 to 8191 pixel location | Second HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGO3 | 13b | 0 to 8191 pixel location | Third HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGO4 | 13b | 0 to 8191 pixel location | Fourth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGO5 | 13b | 0 to 8191 pixel location | Fifth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGO6 | 13b | 0 to 8191 pixel location | Sixth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE1 | 13b | 0 to 8191 pixel location | First HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE2 | 13b | 0 to 8191 pixel location | Second HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE3 | 13b | 0 to 8191 pixel location | Third HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE4 | 13b | 0 to 8191 pixel location | Fourth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE5 | 13b | 0 to 8191 pixel location | Fifth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE6 | 13b | 0 to 8191 pixel location | Sixth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| RA0H1REPA/B/C | 12b | 0 to 15 HCLK pulses for each A, B, and C | HBLK Repeat Area 0. Number of H1 repetitions for HBLKSTARTA/B/C in HBLK Mode 2 for even lines; odd lines defined using HBLKALT_PAT. [3:0] RA0H1REPA. Number of H1 pulses following HBLKSTARTA. [7:4] RA0H1REPB. Number of H1 pulses following HBLKSTARTB. [11:8] RA0H1REPC. Number of H1 pulses following HBLKSTARTC. |
| RA1H1REPA/B/C | 12b | 0 to 15 HCLK pulses | HBLK Repeat Area 1. Number of H1 repetitions for HBLKSTARTA/B/C. |
| RA2H1REPA/B/C | 12b | 0 to 15 HCLK pulses | HBLK Repeat Area 2. Number of H1 repetitions for HBLKSTARTA/B/C. |
| RA3H1REPA/B/C | 12b | 0 to 15 HCLK pulses | HBLK Repeat Area 3. Number of H1 repetitions for HBLKSTARTA/B/C. |
| RA4H1REPA/B/C | 12b | 0 to 15 HCLK pulses | HBLK Repeat Area 4. Number of H1 repetitions for HBLKSTARTA/B/C. |
| RA5H1REPA/B/C | 12b | 0 to 15 HCLK pulses | HBLK Repeat Area 5. Number of H1 repetitions for HBLKSTARTA/B/C. |
| RA0H2REPA/B/C | 12b | 0 to 15 HCLK pulses for each A, B, and C | HBLK Repeat Area 0. Number of H2 repetitions for HBLKSTARTA/B/C in HBLK Mode 2 for even lines; odd lines defined using HBLKALT_PAT. [3:0] RA0H2REPA. Number of H2 pulses following HBLKSTARTA. [7:4] RA0H2REPB. Number of H2 pulses following HBLKSTARTB. [11:8] RA0H2REPC. Number of H2 pulses following HBLKSTARTC. |
| RA1H2REPA/B/C | 12b | 0 to 15 HCLK pulses | HBLK Repeat Area 1. Number of H2 repetitions for HBLKSTARTA/B/C. |
| RA2H2REPA/B/C | 12b | 0 to 15 HCLK pulses | HBLK Repeat Area 2. Number of H2 repetitions for HBLKSTARTA/B/C. |
| RA3H2REPA/B/C | 12b | 0 to 15 HCLK pulses | HBLK Repeat Area 3. Number of H2 repetitions for HBLKSTARTA/B/C. |
| RA4H2REPA/B/C | 12b | 0 to 15 HCLK pulses | HBLK Repeat Area 4. Number of H2 repetitions for HBLKSTARTA/B/C. |
| RA5H2REPA/B/C | 12b | 0 to 15 HCLK pulses | HBLK Repeat Area 5. Number of H2 repetitions for HBLKSTARTA/B/C. |
| HBLKSTARTA | 13b | 0 to 8191 pixel location | HBLK Repeat Area Start Position A for HBLK Mode 2. Set to 8191 if not used. |
| HBLKSTARTB | 13b | 0 to 8191 pixel location | HBLK Repeat Area Start Position B for HBLK Mode 2. Set to 8191 if not used. |
| HBLKSTARTC | 13b | 0 to 8191 pixel location | HBLK Repeat Area Start Position C for HBLK Mode 2. Set to 8191 if not used. |

| Register | Length | Range | Description |
|--------------|--------|-------------------------|---|
| HBLKALT_PAT1 | 3b | 0 to 5 even repeat area | HBLK Mode 2, Odd Field Repeat Area 0 pattern, selected from even field repeat areas previously defined. |
| HBLKALT_PAT2 | 3b | 0 to 5 even repeat area | HBLK Mode 2, Odd Field Repeat Area 1 pattern. |
| HBLKALT_PAT3 | 3b | 0 to 5 even repeat area | HBLK Mode 2, Odd Field Repeat Area 2 pattern. |
| HBLKALT_PAT4 | 3b | 0 to 5 even repeat area | HBLK Mode 2, Odd Field Repeat Area 3 pattern. |
| HBLKALT_PAT5 | 3b | 0 to 5 even repeat area | HBLK Mode 2, Odd Field Repeat Area 4 pattern. |
| HBLKALT_PAT6 | 3b | 0 to 5 even repeat area | HBLK Mode 2, Odd Field Repeat Area 5 pattern. |



H-BLANK REPEATING PATTERN IS CREATED USING HBLKLEN AND HBLKREP REGISTERS

Figure 26. HBLK Repeating Pattern Using HBLKMODE = 1

068891-027

HBLK Mode 1 Operation

Multiple repeats of the HBLK signal are enabled by setting HBLKMODE to 1. In this mode, the HBLK pattern can be generated using a different set of registers: HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP, along with the six toggle positions (see Figure 26).

Separate toggle positions are available for even and odd lines. If alternation is not needed, the same values should be loaded into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

Generating HBLK Line Alternation

HBLK Mode 0 and HBLK Mode 1 provide the ability to alternate different HBLK toggle positions on even and odd lines. HBLK line alternation can be used in conjunction with V-pattern odd/even alternation or on its own. Separate toggle positions are available for even and odd lines. If even/odd line alternation is not required, the same values should be loaded into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

Increasing H-Clock Width During HBLK

HBLK Mode 0 and HBLK Mode 1 allow the H1 to H8 pulse width to be increased during the HBLK interval. As shown in Figure 27, the H-clock frequency can be reduced by a factor of 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, and so on, up to 1/30. To enable this feature, the HCLK_WIDTH register (Address 0x34,

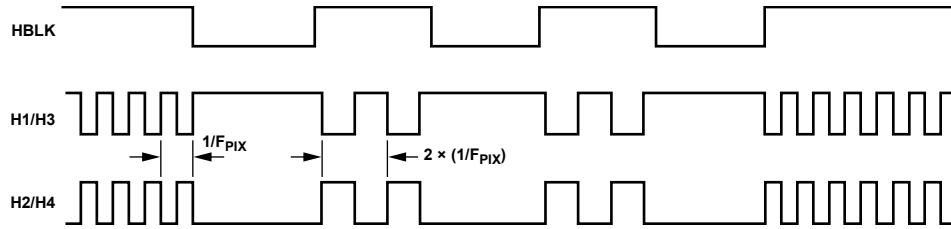
Bits [7:4]) is set to a value between 1 and 15. When this register is set to 0, the wide HCLK feature is disabled. The reduced frequency occurs only for H1 to H8 pulses that are located within the HBLK area.

The HCLK_WIDTH register is generally used in conjunction with special HBLK patterns to generate vertical and horizontal mixing in the CCD.

Note that the wide HCLK feature is available only in HBLK Mode 0 and HBLK Mode 1. HBLK Mode 2 does not support wide HCLKs.

Table 11. HCLK Width Register

| Register | Length | Description |
|------------|--------|---|
| HCLK_WIDTH | 4b | Controls H1 to H8 width during HBLK as a fraction of pixel rate 0: same frequency as pixel rate 1: 1/2 pixel frequency, that is, doubles the HCLK pulse width 2: 1/4 pixel frequency 3: 1/6 pixel frequency 4: 1/8 pixel frequency 5: 1/10 pixel frequency ... 15: 1/30 pixel frequency |



H-CLOCK FREQUENCY CAN BE REDUCED DURING HBLK BY 1/2 (AS SHOWN), 1/4, 1/6, 1/8, 1/10, 1/12, AND SO ON, UP TO 1/30 USING HBLKWIDTH REGISTER

Figure 27. Generating Wide H-Clock Pulses During HBLK Interval

06991-028

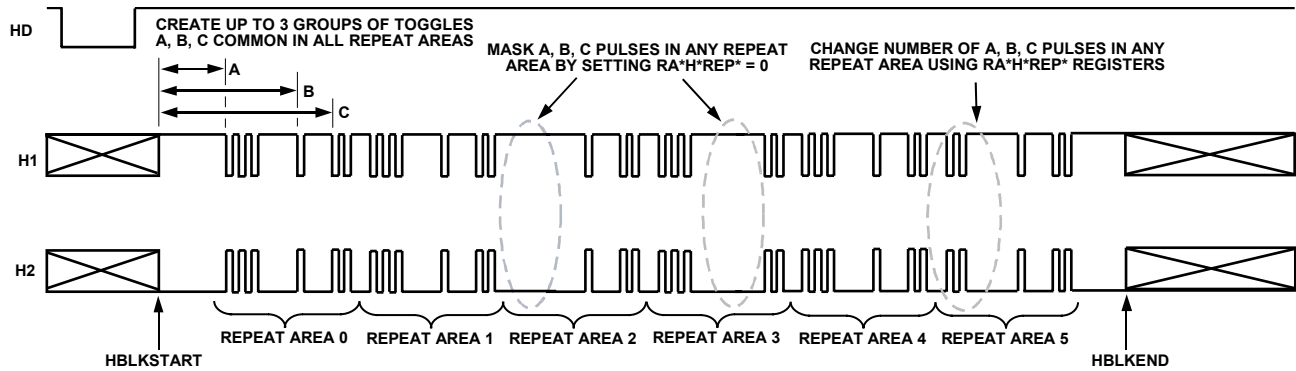


Figure 28. HBLK Mode 2 Operation

06991-029

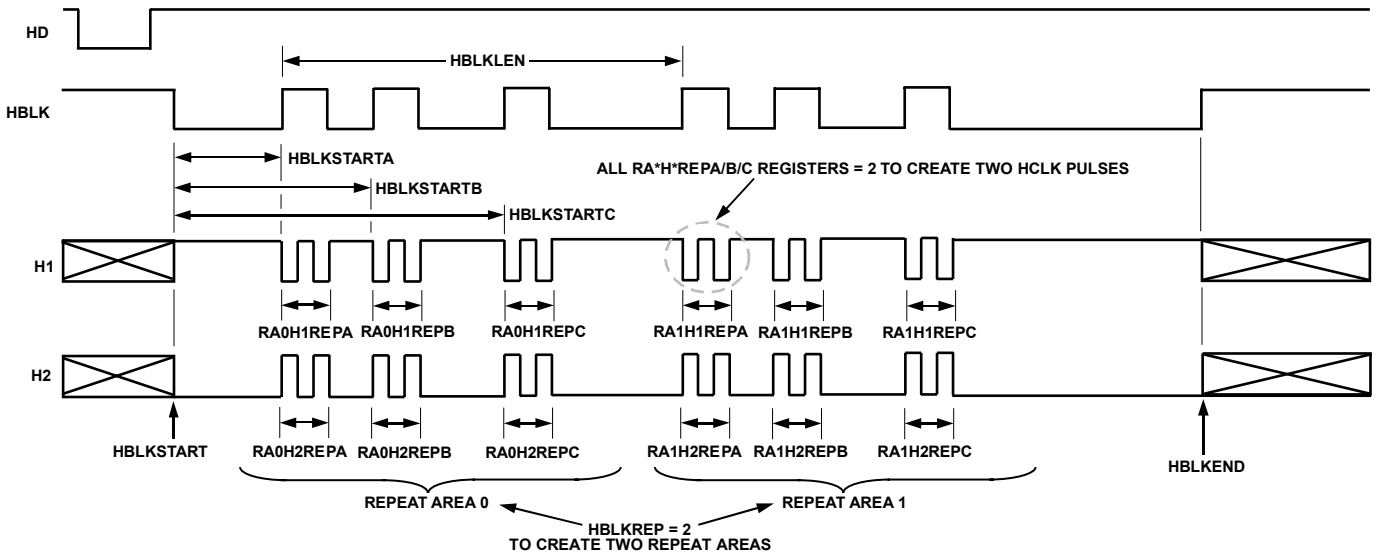


Figure 29. HBLK Mode 2 Registers

06991-030

HBLK Mode 2 Operation

HBLK Mode 2 allows more advanced HBLK pattern operation. If multiple areas of HCLK pulses that are unevenly spaced apart from one another are needed, HBLK Mode 2 can be used. Using a separate set of registers, HBLK Mode 2 can divide the HBLK region into up to six repeat areas (see Table 10). As shown in Figure 29, each repeat area shares a common group of toggle positions, HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC. However, the number of toggles following each start position can be unique in each repeat area by using the RAH1REP and RAH2REP registers. As shown in Figure 28, setting the RAH1REPA/RAH1REPB/RAH1REPC or RAH2REPA/RAH2REPB/RAH2REPC registers to 0 masks HCLK groups from appearing in a particular repeat area. Figure 29 shows only two repeat areas being used, although six are available. It is possible to program a separate number of repeat area repetitions for H1 and H2, but generally the same value is used for both H1 and H2. Figure 29 shows an example of RA0H1REPA/RA0H1REPB/RA0H1REPC = RA0H2REPA/RA0H2REPB/RA0H2REPC = RA1H1REPA/RA1H1REPB/RA1H1REPC = RA1H2REPA/RA1H2REPB/RA1H2REPC = 2.

Furthermore, HBLK Mode 2 allows a different HBLK pattern on even and odd lines. The HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC registers, as well as the RAH1REPA/RAH1REPB/RAH1REPC and RAH2REPA/RAH2REPB/RAH2REPC registers, define operation for the even lines. For separate control of the odd lines, the HBLKALT_PAT registers specify up to six repeat areas on the odd lines by reordering the repeat areas used for the even lines. New patterns are not available, but the order of the previously defined repeat areas on the even lines can be changed for the odd lines to accommodate advanced CCD operation.

HORIZONTAL TIMING SEQUENCE EXAMPLE

Figure 30 shows an example CCD layout. The horizontal register contains 28 dummy pixels, which occur on each line clocked from the CCD. In the vertical direction, there are 10 optical black (OB) lines at the front of the readout and two at the back of the readout. The horizontal direction has four OB pixels in the front and 48 in the back.

Figure 31 shows the basic sequence layout to be used during the effective pixel readout. The 48 OB pixels at the end of each line are used for the CLPOB signals. PBLK is optional and is often used to blank the digital outputs during the HBLK time. HBLK is used during the vertical shift interval.

Because PBLK is used to isolate the CDS input (see the Analog Preblanking section), the PBLK signal should not be used during CLPOB operation. The change in the offset behavior that occurs during PBLK impacts the accuracy of the CLPOB circuitry.

The HBLK, CLPOB, and PBLK parameters are programmed in the V-sequence registers. More elaborate clamping schemes, such as adding in a separate sequence to clamp in the entire shield OB lines, can be used. This requires configuring a separate V-sequence for clocking out the OB lines.

The CLPMASK registers are also useful for disabling the CLPOB on a few lines without affecting the setup of the clamping sequences. It is important that CLPOB be used only during valid OB pixels. During other portions on the frame timing, such as vertical blanking or SG line timing, the CCD does not output valid OB pixels. Any CLPOB pulse that occurs during this time causes errors in clamping operation and changes in the black level of the image.

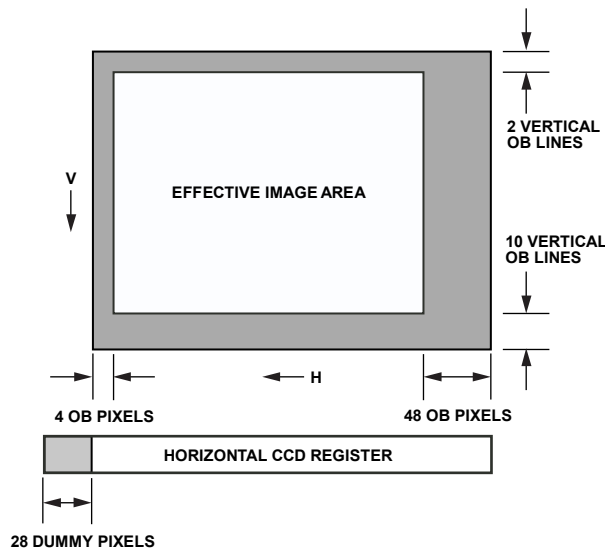
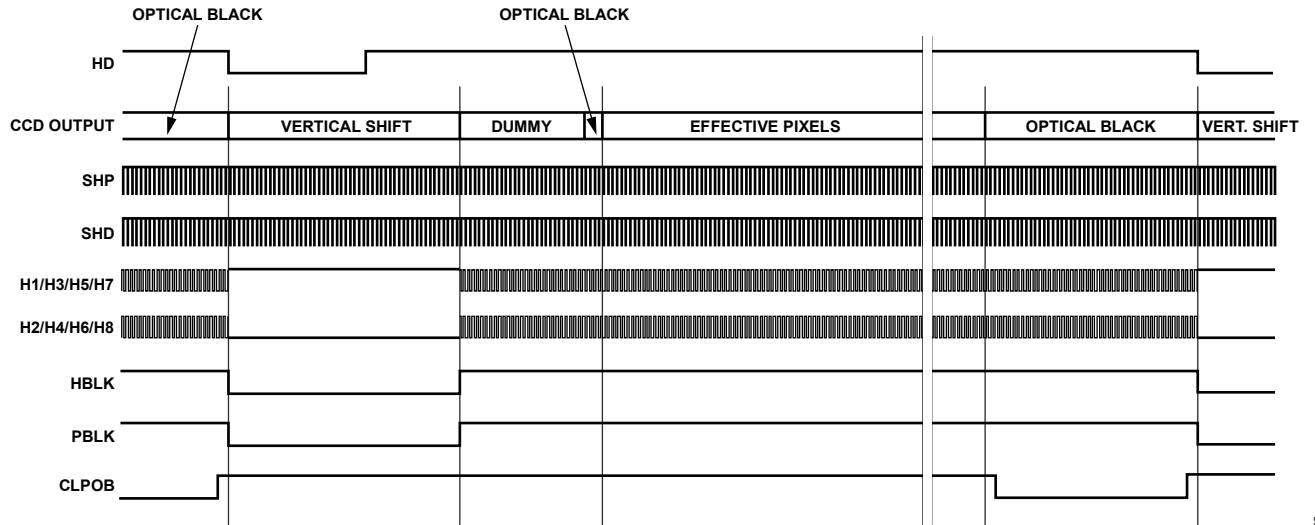


Figure 30. Example CCD Configuration

05891-031



NOTES
 1. PBLK ACTIVE (LOW) SHOULD NOT BE USED DURING CLPOB ACTIVE (LOW).

Figure 31. Horizontal Sequence Example

05691-132

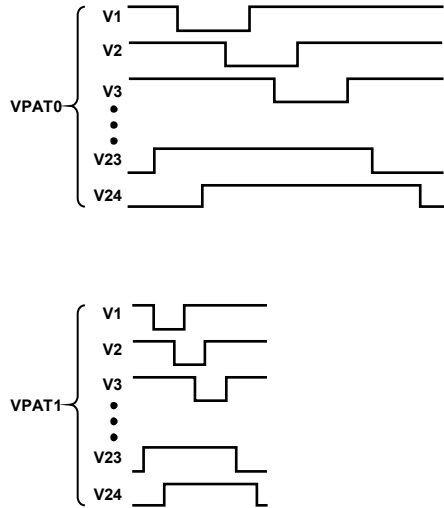
VERTICAL TIMING GENERATION

The AD9992 provides a flexible solution for generating vertical CCD timing and can support multiple CCDs and different system architectures. The vertical transfer clocks are used to shift each line of pixels into the horizontal output register of the CCD. The AD9992 allows these outputs to be individually programmed into various readout configurations by using a 4-step process.

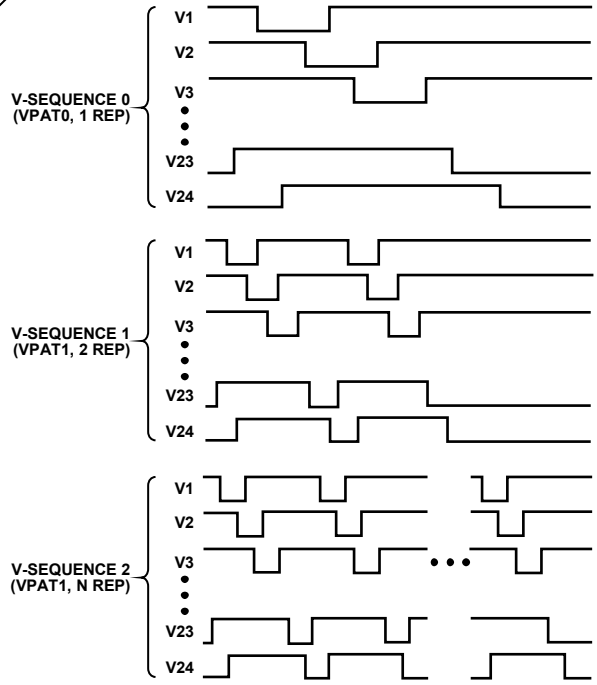
Figure 32 shows an overview of how the vertical timing is generated in four steps.

1. The individual pulse patterns for V1 to V24 are created by using the vertical pattern group registers.
2. The V-pattern groups are used to build the sequences, which is where additional information is added.
3. The readout for an entire field is constructed by dividing the field into different regions and then assigning a sequence to each region. Each field can contain up to nine different regions to accommodate different steps of the readout, such as high speed line shifts and unique vertical line transfers. The total number of V-patterns, V-sequences, and fields is programmable, but limited by the number of registers.
4. The MODE registers allow the different fields to be combined in any order for various readout configurations.

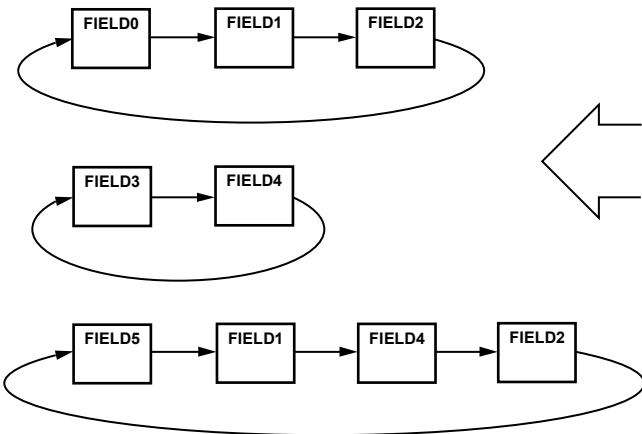
1 CREATE THE VERTICAL PATTERN GROUPS, UP TO FOUR TOGGLE POSITIONS FOR EACH OUTPUT.



2 BUILD THE V-SEQUENCES BY ADDING START POLARITY, LINE START POSITION, NUMBER OF REPEATS, ALTERNATION, GROUP A/B/C/D INFORMATION, AND HBLK/CLPOB PULSES.



4 USE THE MODE REGISTERS TO CONTROL WHICH FIELDS ARE USED, AND IN WHAT ORDER (MAXIMUM OF SEVEN FIELDS MAY BE COMBINED IN ANY ORDER).



3 BUILD EACH FIELD BY DIVIDING INTO DIFFERENT REGIONS AND ASSIGNING A DIFFERENT V-SEQUENCE TO EACH (MAXIMUM OF NINE REGIONS IN EACH FIELD).

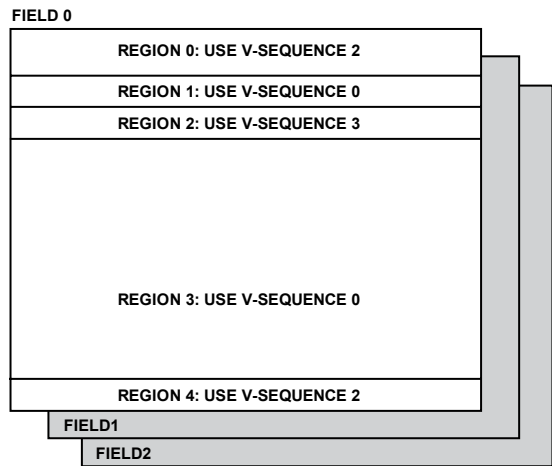


Figure 32. Summary of Vertical Timing Generation

06891-033

Vertical Pattern Groups (VPAT)

The vertical pattern groups define the individual pulse patterns for each V1 to V24 output signal. Table 12 summarizes the registers available for generating each of the V-pattern groups. The first, second, third, and fourth toggle positions (VTOG1, VTOG2, VTOG3, and VTOG4) are the pixel locations within the line where the pulse transitions. All toggle positions are 13-bit values, allowing their placement anywhere in the horizontal line.

More registers are included in the vertical sequence registers to specify the output pulses. VPOL specifies the start polarity for each signal; VSTART specifies the start position of the V-pattern group within the line; VLEN designates the total length of the V-pattern group, which determines the number of pixels between each of the pattern repetitions when repetitions are used.

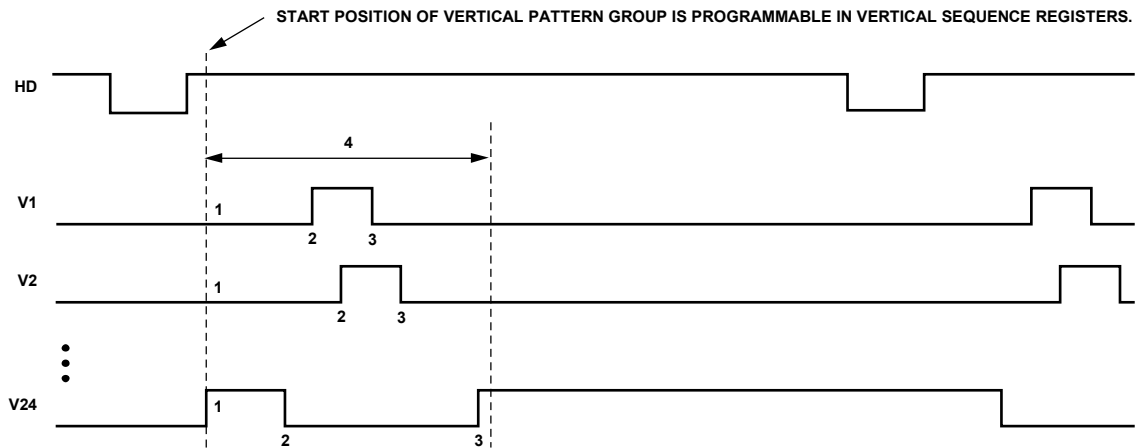
The VSTART position is actually an offset value for each toggle position. The actual pixel location for each toggle, measured from the HD falling edge (Pixel 0), is equal to the VSTART value plus the toggle position.

When the selected V-output is designated as a VSG pulse, either the VTOG1/VTOG2 or VTOG3/VTOG4 pair is selected using V-Sequence Address 0x02, VSGPATSEL. All four toggle positions are not simultaneously available for VSG pulses.

All unused V-channels must have their toggle positions programmed to either 0 or maximum value. This prevents unpredictable behavior because the default values of the V-pattern group registers are unknown.

Table 12. Vertical Pattern Group Registers

| Register | Length | Description |
|----------|--------|---|
| VTOG1 | 13b | First toggle position within line for each V1 to V24 output, relative to VSTART value |
| VTOG2 | 13b | Second toggle position, relative to VSTART value |
| VTOG3 | 13b | Third toggle position, relative to VSTART value |
| VTOG4 | 13b | Fourth toggle position, relative to VSTART value |



PROGRAMMABLE SETTINGS:
¹START POLARITY (LOCATED IN V-SEQUENCE REGISTERS).
²FIRST TOGGLE POSITION.
³SECOND TOGGLE POSITION (THIRD AND FOURTH TOGGLE POSITIONS ALSO AVAILABLE FOR MORE COMPLEX PATTERNS).
⁴TOTAL PATTERN LENGTH FOR ALL VERTICAL OUTPUTS (LOCATED IN VERTICAL SEQUENCE REGISTERS).

Figure 33. Vertical Pattern Group Programmability

06891-004

VERTICAL SEQUENCES (VSEQ)

The vertical sequences are created by selecting one of the V-pattern groups and adding repeats, start position, horizontal clamping, and blanking information. The V-sequences are programmed using the registers shown in Table 13. Figure 34 shows how the different registers are used to generate each V-sequence.

The VPATSELA, VPATSELB, VPATSELC, and VPATSELD registers select which V-pattern is used in a given V-sequence. Having four groups available allows different vertical outputs to be mapped to different V-patterns. The selected V-pattern group can have repetitions added for high speed line shifts or for line binning by using the VREP registers for odd and even lines. Generally, the same number of repetitions is programmed

into both registers. If a different number of repetitions is required on odd and even lines, separate values can be used for each register (see the Generating Line Alternation for V-Sequences and HBLK section). The VSTARTA and VSTARTB registers specify where in the line the V-pattern group starts. The VMASK_EN register is used in conjunction with the FREEZE/RESUME registers to enable optional masking of the V-outputs. Either or both of the FREEZE1/RESUME1 and FREEZE2/RESUME2 registers can be enabled.

The line length (in pixels) is programmable using the HDLEN registers. Each V-sequence can have a different line length to accommodate various image readout techniques. The maximum number of pixels per line is 8192. The last line of the field is programmed separately using the HDLASTLEN register, which is located in the field register section.

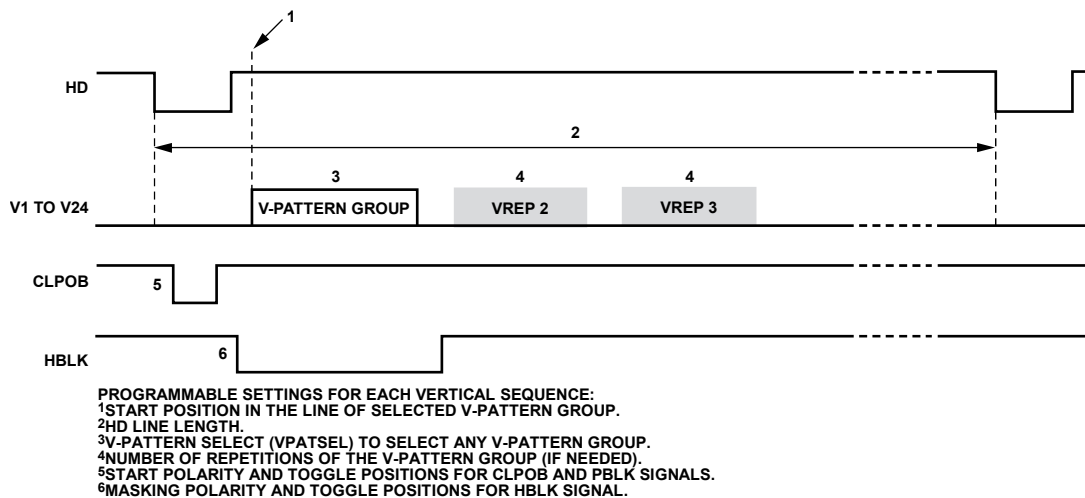


Figure 34. V-Sequence Programmability

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AD9992

Table 13. Summary of V-Sequence Registers (see Table 9 and Table 10 for the HBLK, CLPOB, and PBLK Register Summary)

| Register | Length | Description |
|---------------|--------|---|
| HOLD | 4b | Use in conjunction with VMASK_EN. 1 = HOLD function instead of FREEZE/RESUME function. |
| VMASK_EN | 4b | Enables the masking of V1 to V24 outputs at the locations specified by the FREEZE/RESUME registers. 1 = enable masking for all groups. One bit for each set of Freeze and Resume Positions 1 to 4. |
| CONCAT_GRP | 4b | Combines toggle positions of Groups A/B/C/D when enabled. Only Group A settings for start, polarity, length, and repetition are used when this mode is selected. 0 = disable. 1 = enable the addition of all toggle positions from VPATSELA/B/C/D. 2 = test mode only. Do not use. ... 15 = test mode only. Do not use. |
| VREP_MODE | 2b | Selects line alternation for V-output repetitions. Note separate control for Group A and Groups B/C/D. 0 = disable alternation. Group A uses VREPA_1, Groups B/C/D use VREP_EVEN for all lines. 1 = 2-line. Group A alternates VREPA_1 and VREPA_2. Groups B/C/D alternate VREP_EVEN and VREP_ODD. 2 = 3-line. Group A alternates VREPA_1, VREPA_2, and VREPA_3. Groups B/C/D follow a VREP_EVEN, VREP_ODD, VREP_ODD, VREP_EVEN, VREP_ODD, VREP_ODD pattern. 3 = 4-line. Group A alternates VREPA_1, VREPA_2, VREPA_3, VREPA_4. Groups B/C/D follow 2-line alternation. |
| LASTREPLEN_EN | 4b | Enables a separate pattern length to be used during the last repetition of the V-sequence. One bit for each group (A, B, C, and D). Set bit high to enable. Group A is the LSB. Recommended value is enabled. |
| LASTTOG_EN | 4b | Enables a final toggle position to be added at the end of the V-sequence. The toggle position is shared by all V-outputs in the same group. One bit for each group. Set bit high to enable. Group A is the LSB. |
| HDLENE | 13b | HD line length for even lines in the V-sequence. |
| HDLENO | 13b | HD line length for odd lines in the V-sequence. |
| VPOL_A | 24b | Group A start polarity bits for each V1 to V24 output. |
| VPOL_B | 24b | Group B start polarity bits for each V1 to V24 output. |
| VPOL_C | 24b | Group C start polarity bits for each V1 to V24 output. |
| VPOL_D | 24b | Group D start polarity bits for each V1 to V24 output. |
| GROUPSEL_0 | 24b | Assigns each V1 to V12 output to either Group A/B/C/D. Two bits for each signal. Bits [1:0] are for V1, Bits [3:2] are for V2 ... Bits [23:22] are for V12. 0 = assign to Group A, 1 = Group B, 2 = Group C, and 3 = Group D. |
| GROUPSEL_1 | 24b | Assigns each V13 to V24 output to either Group A/B/C/D. Two bits for each signal. Bits [1:0] are for V13, Bits [3:2] are for V14 ... Bits [23:22] are for V24. 0 = assign to Group A, 1 = Group B, 2 = Group C, and 3 = Group D. |
| VPATSELA | 5b | Selected V-pattern for Group A. |
| VPATSELB | 5b | Selected V-pattern for Group B. |
| VPATSELC | 5b | Selected V-pattern for Group C. |
| VPATSELD | 5b | Selected V-pattern for Group D. |
| VSTARTA | 13b | Start position for the selected V-pattern Group A. |
| VSTARTB | 13b | Start position for the selected V-pattern Group B. |
| VSTARTC | 13b | Start position for the selected V-pattern Group C. |
| VSTARTD | 13b | Start position for the selected V-pattern Group D. |
| VLENA | 13b | Length of selected V-pattern Group A. |
| VLENB | 13b | Length of selected V-pattern Group B. |
| VLENC | 13b | Length of selected V-pattern Group C. |
| VLEND | 13b | Length of selected V-pattern Group D. |
| VREPA_1 | 13b | Number of repetitions for the V-Pattern Group A for first lines (even). |
| VREPA_2 | 13b | Number of repetitions for the V-Pattern Group A for second lines (odd). |
| VREPA_3 | 13b | Number of repetitions for the V-Pattern Group A for third lines. |
| VREPA_4 | 13b | Number of repetitions for the V-Pattern Group A for fourth lines. |
| VREPB_ODD | 13b | Number of repetitions for the V-Pattern Group B for odd lines. |
| VREPC_ODD | 13b | Number of repetitions for the V-Pattern Group C for odd lines. |

| Register | Length | Description |
|---------------|--------|---|
| VREPD_ODD | 13b | Number of repetitions for the V-Pattern Group D for odd lines. |
| VREPB_EVEN | 13b | Number of repetitions for the V-Pattern Group B for even lines. |
| VREPC_EVEN | 13b | Number of repetitions for the V-Pattern Group C for even lines. |
| VREPD_EVEN | 13b | Number of repetitions for the V-Pattern Group D for even lines. |
| FREEZE1 | 13b | Pixel location where the V-outputs freeze or hold (see VMASK_EN). Also used as VALTSEL0_EVEN [12:0] register when Special VSEQALT_EN mode is enabled. |
| FREEZE2 | 13b | Pixel location where the V-outputs freeze or hold (see VMASK_EN). Also used as VALTSEL1_EVEN [12:0] register when Special VSEQALT_EN mode is enabled. |
| FREEZE3 | 13b | Pixel location where the V-outputs freeze or hold (see VMASK_EN). Also used as VALTSEL0_ODD [12:0] register when Special VSEQALT_EN mode is enabled. |
| FREEZE4 | 13b | Pixel location where the V-outputs freeze or hold (see VMASK_EN). Also used as VALTSEL1_ODD [12:0] register when Special VSEQALT_EN mode is enabled. |
| RESUME1 | 13b | Pixel location where the V-outputs resume operation (see VMASK_EN). Also used as VALTSEL0_EVEN [17:13] register when Special VSEQALT_EN mode is enabled. |
| RESUME 2 | 13b | Pixel location where the V-outputs resume operation (see VMASK_EN). Also used as VALTSEL1_EVEN [17:13] register when Special VSEQALT_EN mode is enabled. |
| RESUME3 | 13b | Pixel location where the V-outputs resume operation (see VMASK_EN). Also used as VALTSEL0_ODD [17:13] register when Special VSEQALT_EN mode is enabled. |
| RESUME4 | 13b | Pixel location where the V-outputs resume operation (see VMASK_EN). Also used as VALTSEL1_ODD [17:13] register when Special VSEQALT_EN mode is enabled. |
| LASTREPLEN_A | 13b | Separate length for last repetition of vertical pulses. Must be enabled using LASTREPLEN_EN. Should be programmed to a value equal to the VLENA register. |
| LASTREPLEN_B | 13b | Separate length for last repetition of vertical pulses. Must be enabled using LASTREPLEN_EN. Should be programmed to a value equal to the VLENB register. |
| LASTREPLEN_C | 13b | Separate length for last repetition of vertical pulses. Must be enabled using LASTREPLEN_EN. Should be programmed to a value equal to the VLENC register. |
| LASTREPLEN_D | 13b | Separate length for last repetition of vertical pulses. Must be enabled using LASTREPLEN_EN. Should be programmed to a value equal to the VLEND register. |
| LASTTOG_A | 13b | Optional fifth toggle position for the vertical signals. Must be enabled using LASTTOG_EN. Note that the toggle position is common for all vertical signals. |
| LASTTOG_B | 13b | Optional fifth toggle position for the vertical signals. Must be enabled using LASTTOG_EN. Note that the toggle position is common for all vertical signals. |
| LASTTOG_C | 13b | Optional fifth toggle position for the vertical signals. Must be enabled using LASTTOG_EN. Note that the toggle position is common for all vertical signals. |
| LASTTOG_D | 13b | Optional fifth toggle position for the vertical signals. Must be enabled using LASTTOG_EN. Note that the toggle position is common for all vertical signals. |
| VSEQALT_EN | 1b | Special V-sequence alternation mode is enabled when this register is programmed high. |
| VALT_MAP | 1b | Enables the use of FREEZE/RESUME register locations to specify the VALTSEL0 and VALTSEL1 registers. Must be enabled if VSEQALT mode is enabled. |
| VALTSEL0_EVEN | 18b | Select lines for special V-sequence alternation mode for even lines. Used to concatenate VPAT Groups A/B/C/D into unique merged patterns. Setting is used to specify one segment, with up to a maximum of 18 segments. |
| VALTSEL1_EVEN | 18b | Select lines for special V-sequence alternation mode for even lines. Used to concatenate VPAT Groups A/B/C/D into unique merged patterns. Setting is used to specify one segment, with up to a maximum of 18 segments. |
| VALTSEL0_ODD | 18b | Select lines for special V-sequence alternation mode for odd lines. Used to concatenate VPAT Groups A/B/C/D into unique merged patterns. Setting is used to specify one segment, with up to a maximum of 18 segments. |
| VALTSEL1_ODD | 18b | Select lines for special V-sequence alternation mode for odd lines. Used to concatenate VPAT Groups A/B/C/D into unique merged patterns. Setting is used to specify one segment, with up to a maximum of 18 segments. |
| SPC_PAT_EN | 1b | Enable special V-pattern to be inserted into one repetition of a VPATA series. SPC_PAT_EN [0]: set to 1 to enable VPATB to be used as special pattern insertion. SPC_PAT_EN [1]: set to 1 to enable VPATC to be used as special pattern insertion. SPC_PAT_EN [2]: set to 1 to enable VPATD to be used as special pattern insertion. |

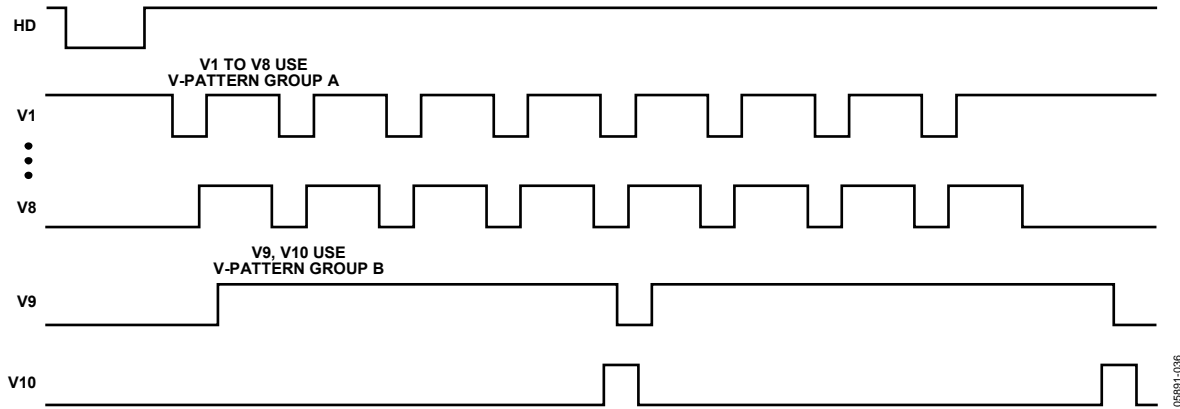


Figure 35. Using Separate Group A and Group B Patterns

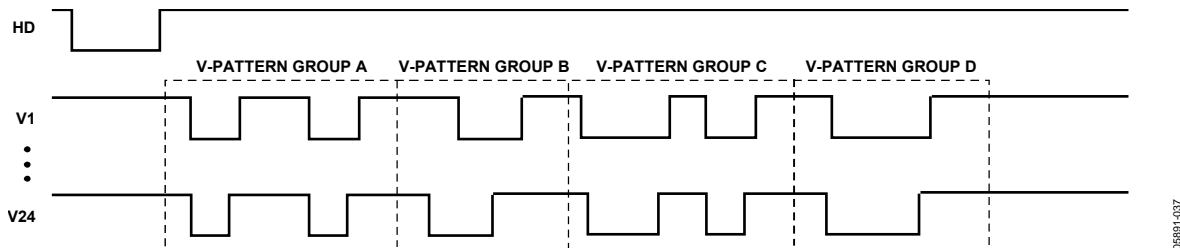


Figure 36. Combining Multiple V-Patterns Using CONCAT_GRP = 1

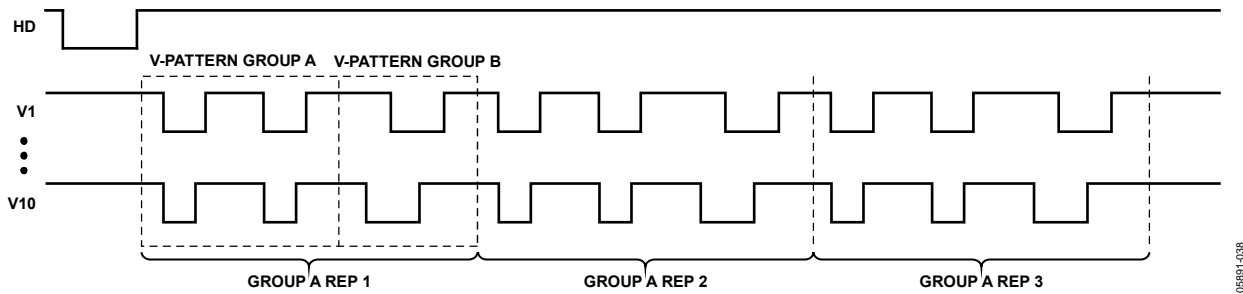


Figure 37. Combining Group A and Group B Patterns with Repetition

Group A/Group B/Group C/Group D Selection

The AD9992 has the flexibility to use four different V-pattern groups in a vertical sequence. In general, the vertical outputs use the same V-pattern group during a particular sequence. It is possible to assign some of the outputs to a different V-pattern group, which can be useful in certain CCD readout modes.

The GROUPSEL registers are used to select Group A, Group B, Group C, or Group D for each V-output. In general, only a single V-pattern group is needed for the vertical outputs; therefore, Group A should be selected for all outputs by default (GROUPSEL_0, GROUPSEL_1 = 0x00). In this configuration, all outputs use the V-pattern group specified by the VPATSELA register.

If additional flexibility is needed, some outputs can be set to Group B, Group C, or Group D in the GROUPSEL registers. In this case, those selected outputs use the V-pattern group specified by the VPATSELB, VPATSELC, or VPATSELD registers. Figure 35 shows an example where outputs V9 and V10 are using a separate V-Pattern Group B to perform special CCD timing.

Another application of the Group A, Group B, Group C, and Group D registers is to combine up to four different V-pattern groups together for more complex patterns. This is accomplished by setting the CONCAT_GRP register (Address 0x00, Bits [13:10]) equal to 0x01. This setting combines the toggle positions from the V-pattern groups specified by registers VPATSELA, VPATSELB, VPATSELC, and VPATSELD for a

maximum of up to 16 toggle positions. Example timing for the CONCAT_GRP = 1 feature is shown in Figure 36.

If only two groups are needed (up to eight toggle positions) for the specified timing, the VPATSELB, VPATSEL C, and VPATSELD registers can be programmed to the same value. If only three groups are needed, VPATSEL C and VPATSELD can be programmed to the same value. Following this approach conserves register memory if the four separate V-patterns are not needed.

Note that when CONCAT_GRP is enabled, the Group A settings are used only for start position, polarity, length, and repetitions. All toggle positions for Group A, Group B, Group C, and Group D are combined together and applied using the settings in the VSTARTA, VPOL_A, VLENA, and VREPA registers.

Special Vertical Sequence Alternation (SVSA) Mode

The AD9992 has additional flexibility for combining four different V-pattern groups in a random sequence that can be programmed for specific CCD requirements. This mode of operation allows custom vertical sequences for CCDs that require more complex vertical timing patterns. For example, using the special vertical sequence alternation mode, it is possible to support random pattern concatenation, with additional support for odd/even line alternation.

Figure 38 illustrates four common and repetitive vertical pattern segments, A through D, that are derived from the complete vertical pattern. Figure 39 illustrates how each group can be concatenated together in an arbitrary order.

To enable the SVSA mode, write the VSEQALT_EN bit, Address 0x20 Bit [13], equal to 0x01. The location of the VALTSEL registers is shared with the VPAT registers for V24. When SVSA mode is enabled, the VALTSEL register function is selected.

To create SVSA timing, divide the complete vertical timing pattern into four common and repetitive segments. Identify the related segments as VPATA, VPATB, VPATC, or VPATD. Up to four toggle positions for each segment can be programmed using the V-pattern registers.

Table 14 shows how the segments are specified using a 2-bit representation. Each bit from VALTSEL0 and VALTSEL1 are combined to produce four values, corresponding to patterns A, B, C, and D.

Table 14. VALTSEL Bit Settings for Even and Odd Lines

| Parameter | VALTSEL BIT SETTINGS | | | |
|----------------------------------|----------------------|---|---|---|
| VALTSEL0_EVEN | 0 | 0 | 1 | 1 |
| VALTSEL1_EVEN | 0 | 1 | 0 | 1 |
| VALTSEL0_ODD | 0 | 0 | 1 | 1 |
| VALTSEL1_ODD | 0 | 1 | 0 | 1 |
| Resulting pattern for even lines | A | B | C | D |
| Resulting pattern for odd lines | A | B | C | D |

When the entire pattern is divided, program VALTSEL0 (even and odd) [17:0] and VALTSEL1 (even and odd) [17:0] so that the segments will be concatenated in the desired order. If separate odd and even lines are not required, set the odd and even registers to the same value.

Figure 40 illustrates the process of using six vertical pattern segments that have been concatenated into a small, merged pattern.

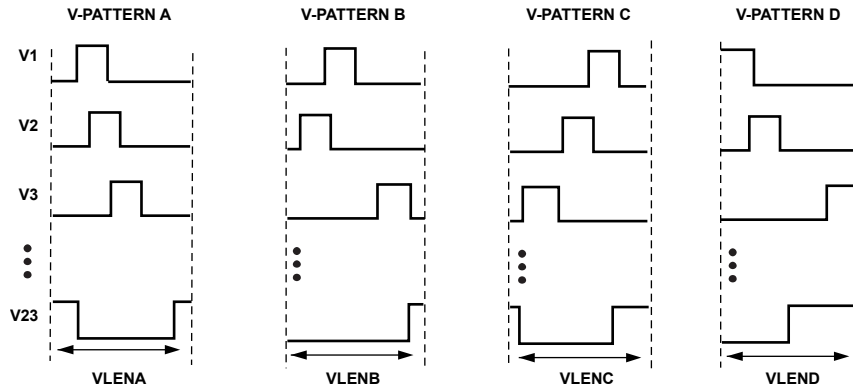
Program the register VREPA_1 to specify the number of segments that will be concatenated into each merged pattern. The maximum number of segments that can be concatenated to create a merged pattern is 18. Program VLENA, VLENB, VLENC, VLEND to be of equal length. Finally, program HBLK to generate the proper H-clock timing using the procedure for HBLK Mode 2 described in the HBLK Mode 2 Operation section.

It is important to note that because the FREEZE/RESUME registers are used to specify the VALTSEL registers, the VALT_MAP register must be enabled when using the special VALT mode.

Table 15. VALTSEL Register Locations¹

| Register Function When VSEQALT_EN = 1 | Register Location |
|--|-------------------------------|
| VALTSEL0_EVEN [12:0] | VSEQ register FREEZE1 [12:0] |
| VALTSEL0_EVEN [17:13] | VSEQ register RESUME1 [17:13] |
| VALTSEL1_EVEN [12:0] | VSEQ register FREEZE2 [12:0] |
| VALTSEL1_EVEN [17:13] | VSEQ register RESUME2 [17:13] |
| VALTSEL0_ODD [12:0] | VSEQ register FREEZE3 [12:0] |
| VALTSEL0_ODD [17:13] | VSEQ register RESUME3 [17:13] |
| VALTSEL1_ODD [12:0] | VSEQ register FREEZE4 [12:0] |
| VALTSEL1_ODD [17:13] | VSEQ register RESUME4 [17:13] |

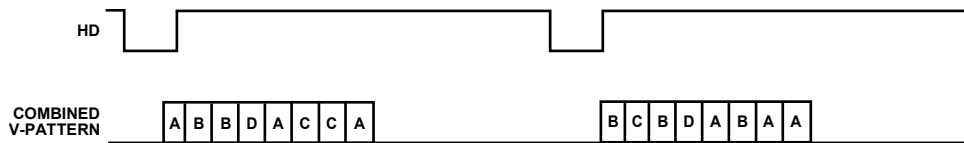
¹ The VALT_MAP register must be set to 1 to enable the use of VALTSEL registers.



NOTES
 1. EACH SEGMENT MUST BE THE SAME LENGTH.
 VLENA = VLENB = VLENC = VLEND.

Figure 38. Vertical Timing Divided Into Four Segments: VPATA, VPATB, VPATC, and VPATD

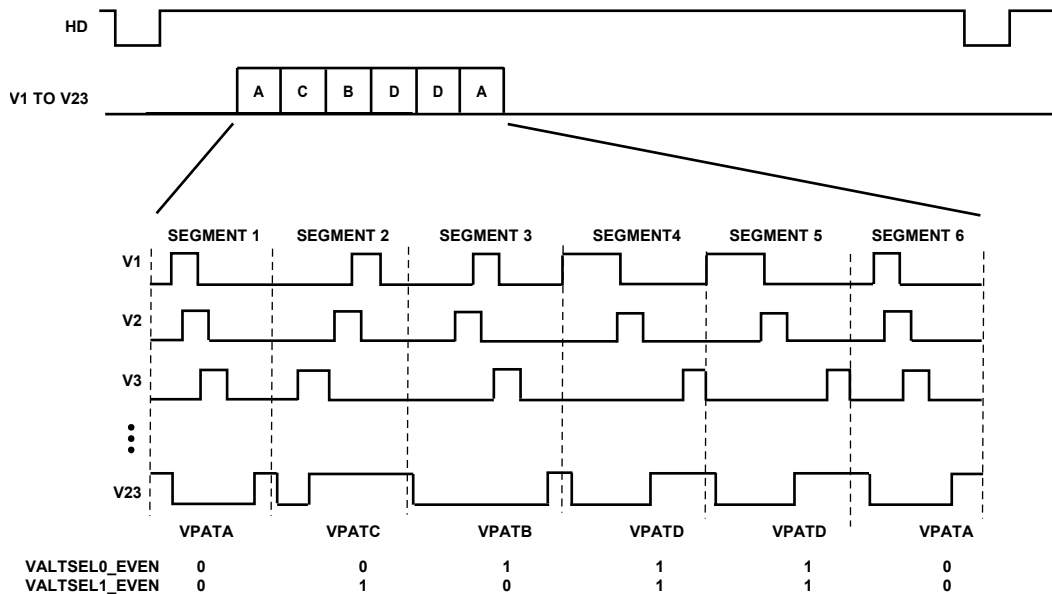
05891-039



NOTES
 1. ABLE TO CONCATENATE PATTERNS TOGETHER ARBITRARILY.
 2. EACH PATTERN CAN HAVE UP TO FOUR TOGGLES PROGRAMMED.
 3. MAY CONCATENATE UP TO 18 PATTERNS INTO A MERGED PATTERN.
 4. ODD AND EVEN LINES CAN HAVE A DIFFERENT PATTERN CONCATENATION SPECIFIED BY VALTSEL EVEN AND ODD REGISTERS.

Figure 39. Concatenating Each VPAT Group in Arbitrary Order

05891-040



NOTES
 1. SIX V-PATTERN SEGMENTS CONCATENATED INTO A MERGED PATTERN.
 2. COMMON AND REPETITIVE VTP SEGMENTS DERIVED FROM THE COMPLETE VTP PATTERN.
 3. VALTSEL REGISTERS SPECIFY SEGMENT ORDER TO CREATE THE CONCATENATED MERGED PATTERN.

Figure 40. Example of Special V-Sequence Alternation Mode Using VALTSEL Registers to Specify Segment Order

05891-041

Using the LASTREPLEN_EN

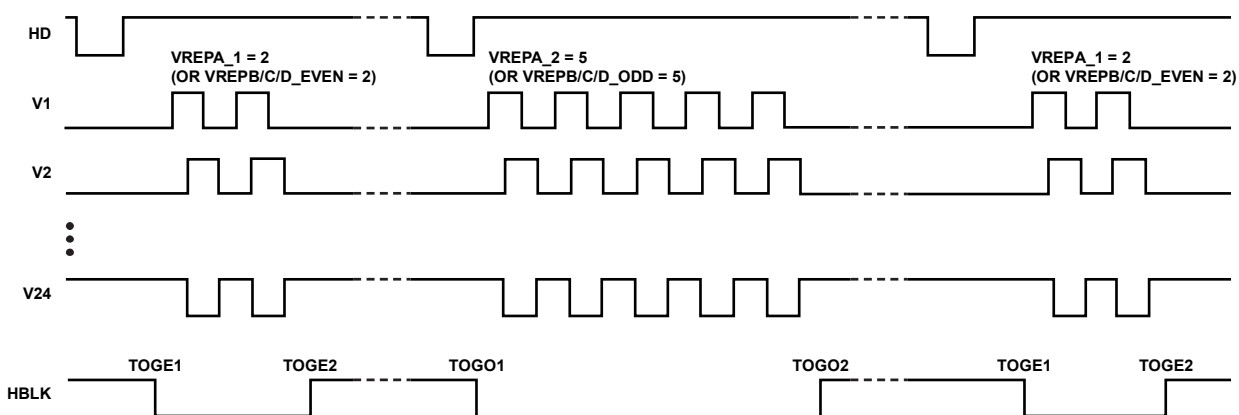
The LASTREPLEN_EN register (Address 0x00, Bits [19:16] in the sequence registers) is used to enable a separate pattern length to be used in the final repetition of several pulse repetitions. It is recommended that the LASTREPLEN_EN register bits be set high (enabled) and the LASTREPLEN_A, LASTREPLEN_B, LASTREPLEN_C, and LASTREPLEN_D registers be set to a value equal to the VLENA, VLENB, VLENC, and VLEND register values, respectively.

Generating Line Alternation for V-Sequences and HBLK

During low resolution readout, some CCDs require a different number of vertical clocks on alternate lines. The AD9992 can support this by using the VREP registers. This allows a different number of V-pattern group repetitions to be programmed on

odd and even lines. Only the number of repeats can be different in odd and even lines, while the V-pattern group remains the same. There are separate controls for the assigned Group A, Group B, Group C, and Group D patterns. All groups can support odd and even line alternation. Group A uses the VREPA_1 and VREPA_2 registers; Group B, Group C, and Group D use the corresponding VREP_ODD and VREP_EVEN registers. With the additional VREPA_3 and VREPA_4 registers, Group A can also support 3-line and 4-line alternation.

As discussed in the Generating HBLK Line Alternation section, the HBLK signal can be alternated for odd and even lines. Figure 41 shows an example of V-pattern group repetition alternation and HBLK Mode 0 alternation used together.



NOTES

1. THE NUMBER OF REPEATS FOR V-PATTERN GROUPS A/B/C/D CAN BE ALTERNATED ON ODD AND EVEN LINES.
2. GROUP A ALSO SUPPORTS 3- AND 4-LINE ALTERNATION USING THE ADDITIONAL VREPA_3 AND VREPA_4 REGISTERS.
3. THE HBLK TOGGLE POSITIONS CAN BE ALTERNATED BETWEEN ODD AND EVEN LINES TO GENERATE DIFFERENT HBLK PATTERNS.

Figure 41. Odd/Even Line Alternation of V-Pattern Group Repetitions and HBLK Toggle Positions

05891-042

Vertical Masking Using FREEZE/RESUME Registers

As shown in Figure 42 and Figure 43, the FREEZE/RESUME registers are used to temporarily mask the V-outputs. The pixel locations to begin the masking (FREEZE) and end the masking (RESUME) create an area in which the vertical toggle positions are ignored. At the pixel location specified in the FREEZE register, the V-outputs are held static at their current dc state, high or low. The V-outputs are held until the pixel location specified by the RESUME register is reached, at which point the signals continue with any remaining toggle positions, if any exist. Four sets of

FREEZE/RESUME registers are provided, allowing the vertical outputs to be interrupted up to four times in the same line. The FREEZE and RESUME Positions 1 to 4 are enabled independently and applied to all groups (Group A, Group B, Group C, and Group D) using the VMASK_EN register.

Note that when masking is enabled, each group (Group A, Group B, Group C, and Group D) uses the same FREEZE/RESUME positions.

Note that the FREEZE/RESUME registers are also used as the VALTSEL0 and VALTSEL1 registers during special vertical alternation mode.

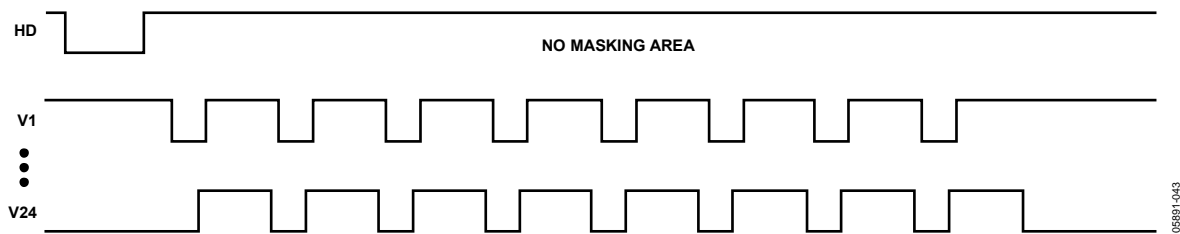
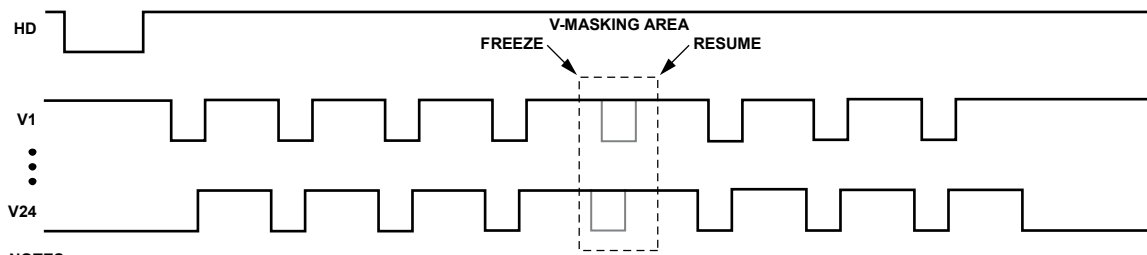


Figure 42. No FREEZE/RESUME

05891-043



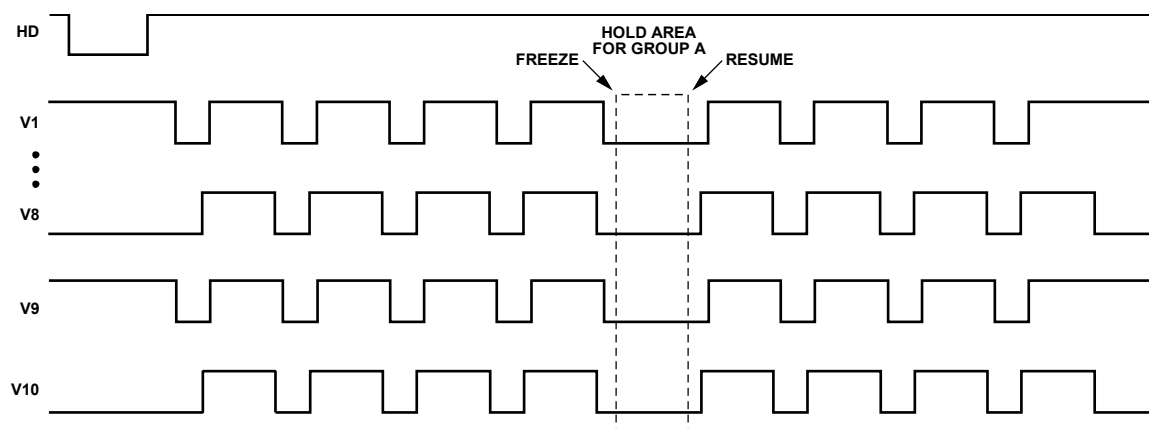
NOTES
 1. ALL TOGGLE POSITIONS WITHIN THE FREEZE/RESUME MASKING AREA ARE IGNORED. H-COUNTER CONTINUES TO COUNT DURING MASKING.
 2. FOUR SEPARATE MASKING AREAS ARE AVAILABLE, USING FREEZE1/RESUME1, FREEZE2/RESUME2, FREEZE3/RESUME3, AND FREEZE4/RESUME4 REGISTERS.

Figure 43. Using FREEZE/RESUME

05891-044

Hold Area Using FREEZE/RESUME Registers

The FREEZE/RESUME registers can also be used to create a hold area in which the V-outputs are temporarily held and later continued, starting at the point where they were held. As shown in Figure 44, this is different than the VMASK_EN register because the V-outputs continue from where they stopped rather than continuing from where they would have been. The hold area temporarily stops the pixel counter for the V-outputs, while the V-masking allows the counter to continue in the masking area.



NOTES

1. WHEN HOLD = 1 FOR ANY V-SEQUENCE GROUP, THE FREEZE AND RESUME REGISTERS ARE USED TO SPECIFY THE HOLD AREA.
2. ABOVE EXAMPLE: V1 TO V10 ARE ASSIGNED TO GROUP A. HOLD BIT FOR GROUP A = 1.
3. H-COUNTER FOR GROUP A (V1 TO V10) STOPS DURING HOLD AREA.

Figure 44. Hold Area for Group A

05891-045

Special Pattern Insertion

Additional flexibility is available using the SPC_PAT_EN registers, which allows a Group B, C, or D pattern to be inserted into a series of Group A repetitions. This feature is useful when a different pattern is needed at the start, end, or middle of a sequence.

Figure 45 shows an example of a sweep region using VPATA with multiple repetitions where a single repetition of VPATB has been added into the middle of the sequence. Figure 46 shows more detail on how to set the registers to achieve the desired timing.

Note that VREPB is used to specify which repetition number has the special pattern inserted instead of VPATA. VPATB always has priority over VPATC or VPATD if more than one SPC_PAT_EN bit is enabled (SPC_PAT_EN [0] has priority).

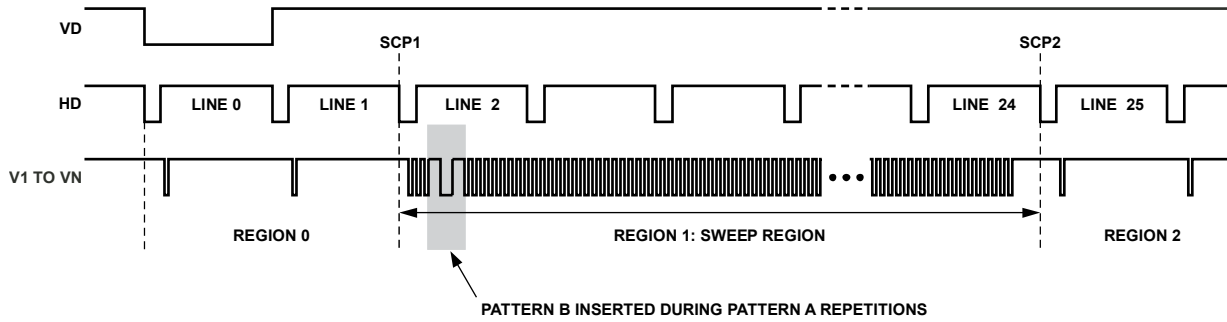
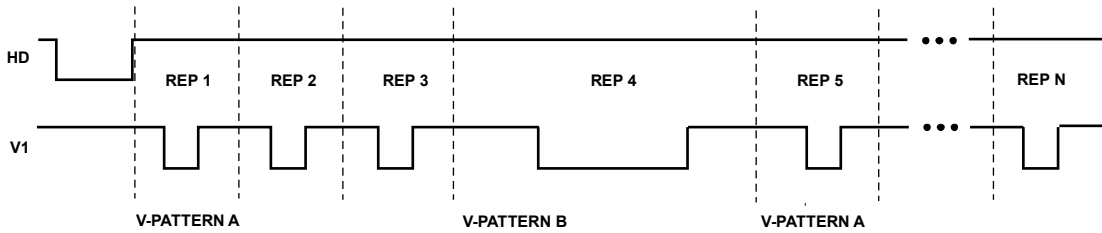


Figure 45. Example of Special Pattern Insertion



| | |
|--|---|
| REGISTER SETTINGS: SPC_PAT_EN[0] = 1 VREPA = N VREPB = 4 | DESCRIPTION: V-PATTERN B IS USED AS SPECIAL PATTERN TOTAL NUMBER OF REPS USED FOR SEQUENCE (N REPS) REP 4 USES V-PATTERN B INSTEAD OF V-PATTERN A |
|--|---|

NOTES
 1. VSTARTB MUST BE SET EQUAL TO VSTARTA.

Figure 46. Example of Special Pattern Insertion, Detail

Complete Field: Combining V-Sequences

After the V-sequences are created, they are combined to create different readout fields. A field consists of up to nine regions, and within each region, a different V-sequence can be selected. Figure 47 shows how the sequence change positions (SCP) designate the line boundary for each region and how the SEQ registers then select which V-sequence is used in each region. Registers to control the VSG outputs are also included in the field registers. Table 16 summarizes the registers used to create the different fields.

The SEQ registers, one for each region, select which of the V-sequences are active in each region. The MULT_SWEEP registers, one for each region, are used to enable sweep mode and/or multiplier mode in any region. The SCP registers create the line boundaries for each region. The VDLEN register specifies the total number of lines in the field. The HDLEN registers specifies the total number of pixels per line, and the

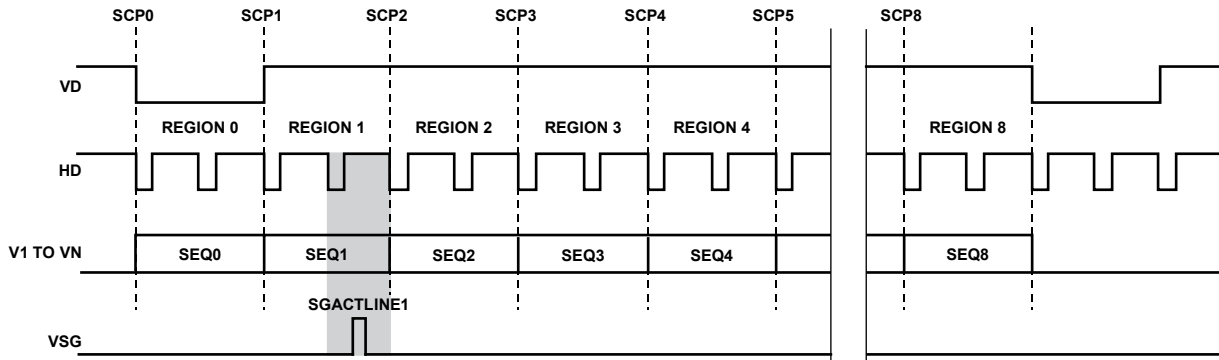
HDLASTLEN register specifies the number of pixels in the last line of the field. The VPATSECOND register is used to add a second V-pattern group to the V1 to V10 outputs in the vertical sensor gate (VSG) line.

The SGMASK register is used to enable or disable each individual VSG output. There are two bits for each VSG output to enable separate masking in SGACTLINE1 and SGACTLINE2.

Setting a masking bit high masks the output; setting it low enables the output. The VSGPATSEL register assigns one of the eight SG patterns to each VSG output. The individual SG patterns are created separately using the SG pattern registers. The SGACTLINE1 register specifies which line in the field contains the VSG outputs. The optional SGACTLINE2 register allows the same VSG pulses to be repeated on a different line. Separate masking is not available for SGACTLINE1 and SGACTLINE2.

Table 16. Field Registers (CLPOB, PBLK Masking Shown in Table 9)

| Register | Length | Range | Description |
|------------|--------|------------------------|--|
| SEQx | 5b | 0 to 31 V-sequence no. | Selected V-sequence for each region in the field. |
| MULT_SWEEP | 2b | 0 to 3 | Enables multiplier mode and/or sweep mode for each region. 0: multiplier off, sweep off. 1: multiplier off, sweep on. 2: multiplier on, sweep off. 3: multiplier on, sweep on. |
| SCP | 13b | 0 to 8191 line no. | Sequence change position for each region. |
| VDLEN | 13b | 0 to 8191 lines | Total number of lines in each field. |
| HDLASTLEN | 13b | 0 to 8191 pixels | Length in pixels of the last HD line in each field. |
| VSGPATSEL | 24b | High/low | VSGPATSEL selects which V-pattern toggle positions are used. When set to 0, Toggle 1 and Toggle 2 are used. When set to 1, Toggle 3 and Toggle 4 are used. [0]: XV1 selection (0 = use TOG1, TOG2; 1 = use TOG3, TOG4). ... [23]: XV24 selection. |
| SGMASK | 24b | High/low, each VSG | Set high to mask each individual VSG output. [0]: XV1 mask. ... [23]: XV24 mask. |
| SGACTLINE1 | 13b | 0 to 8191 line no. | Selects the line in the field where the VSG signals are active. |
| SGACTLINE2 | 13b | 0 to 8191 line no. | Selects a second line in the field to repeat the VSG signals. If not used, set this equal to SGACTLINE1 or to the maximum value. |



- FIELD SETTINGS:**
1. SEQUENCE CHANGE POSITIONS (SCP0 TO SCP8) DEFINE EACH OF THE NINE AVAILABLE REGIONS IN THE FIELD.
 2. SEQ0 TO SEQ8 SELECT THE DESIRED V-SEQUENCE FOR EACH REGION.
 3. SGACTION1 REGISTER SELECTS WHICH HD LINE IN THE FIELD CONTAINS THE SENSOR GATE PULSE(S).

Figure 47. Complete Field is Divided into Regions

05891-048

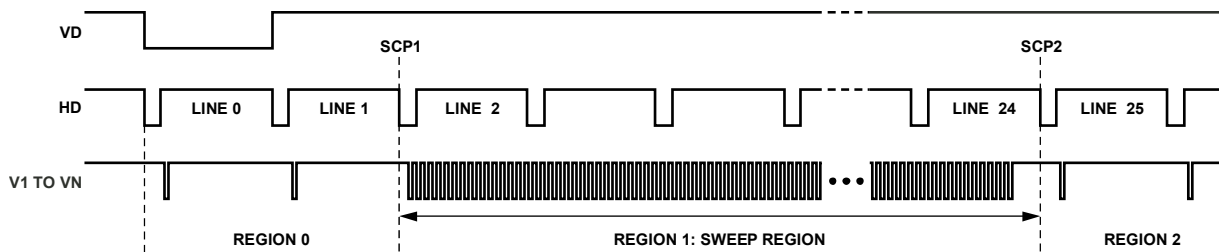


Figure 48. Example of Sweep Region for High Speed Vertical Shift

05891-048

Sweep Mode Operation

The AD9992 contains an additional mode of vertical timing operation called sweep mode. This mode is used to generate a large number of repetitive pulses that span across multiple HD lines. An example of where this mode is needed is at the start of the CCD readout operation. At the end of the image exposure before the image is transferred by the sensor gate pulses, the vertical interline CCD registers should be free of all charge. This can be accomplished by quickly shifting out any charge using a long series of pulses from the vertical outputs. Depending on the vertical resolution of the CCD, up to 3000 clock cycles might be needed to shift the charge out of each vertical CCD line. This operation spans across multiple HD line lengths. Normally, the AD9992 vertical timing must be contained within one HD line length, but when sweep mode is enabled, the HD boundaries are ignored until the region is finished. To enable sweep mode within any region, program the appropriate SWEEP register to high.

Figure 48 shows an example of the sweep mode operation. The number of vertical pulses needed depends on the vertical resolution of the CCD. The toggle positions for the V1 to V24 signals are generated using the V-pattern registers (shown in Table 12). A single pulse is created using the polarity and toggle position registers. The number of repetitions is then programmed to match the number of vertical shifts required by the CCD. Repetitions are programmed into the V-sequence registers (shown in Table 13) by using the VREP registers. This produces a pulse train of the appropriate length. Normally, the pulse train is truncated at the end of the HD line length, but when sweep mode is enabled for this region, the HD boundaries are ignored. In Figure 48, the sweep region occupies 23 HD lines. After the sweep mode region is complete, normal sequence operation resumes in the next region. When using sweep mode, be sure to set the region boundaries (using the sequence change positions) to the appropriate lines to prevent the sweep operation from overlapping the next V-sequence.

Multiplier Mode

To generate very wide vertical timing pulses, a vertical region can be configured into a multiplier region. This mode uses the V-pattern registers in a slightly different manner. Multiplier mode can be used to support unusual CCD timing requirements, such as vertical pulses that are wider than the 13-bit V-pattern toggle position counter. In general, the 13-bit toggle position counter can be used with the sweep mode feature to support very wide pulses; however, multiplier mode can be used to generate even wider pulses.

The start polarity and toggle positions are still used in the same manner as the standard V-pattern group programming, but VLEN is used differently. Instead of using the pixel counter (HD counter) to specify the toggle position locations (VTOG1, VTOG 2, VTOG 3, and VTOG 4) of the V-pattern group, the VLEN is multiplied with the VTOG position to allow very long pulses to be generated. To calculate the exact toggle position, which is counted in pixels after the start position, use the following equation:

$$\text{Multiplier Mode Toggle Position} = \text{VTOG} \times \text{VLEN}$$

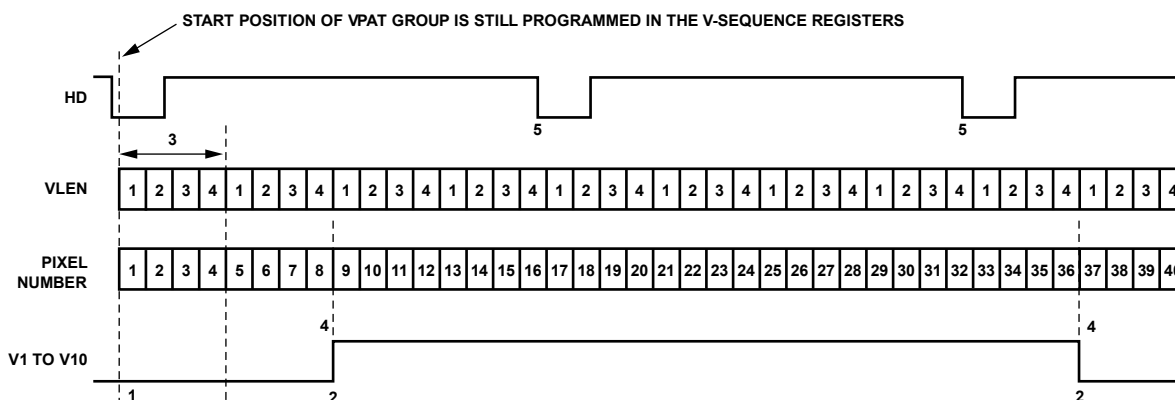
Because the VTOG register is multiplied by VLEN, the resolution of the toggle position placement is reduced. If VLEN = 4, the toggle position precision is reduced to 4-pixel increments instead of to single-pixel increments.

Table 17 summarizes how the V-pattern group registers are used in multiplier mode operation. In multiplier mode, the VREP registers must always be programmed to the same value as the highest toggle position.

Figure 49 illustrates this operation. The first toggle position is 2, and the second toggle position is 9. In nonmultiplier mode, this causes the V-sequence to toggle at Pixel 2 and then at Pixel 9 within a single HD line. However, in multiplier mode toggle positions are multiplied by the value of VLEN (in this case, 4); therefore, the first toggle occurs at Pixel 8, and the second toggle occurs at Pixel 36. Sweep mode has also been enabled to allow the toggle positions to cross the HD line boundaries.

Table 17. Multiplier Mode Register Parameters

| Register | Length | Range | Description |
|----------|--------|--------------------------|---|
| MULTI | 1b | High/low | High enables multiplier mode. |
| VPOL | 1b | High/low | Starting polarity of V1 to V10 signals in each V-pattern group. |
| VTOG | 13b | 0 to 8191 pixel location | Toggle positions for V1 to V10 signals in each V-pattern group. |
| VLEN | 13b | 0 to 8191 pixels | Used as multiplier factor for toggle position counter. |
| VREP | 13b | 0 to 8191 pixel location | VREP_EVEN/VREP_ODD must be set to the same value as the highest VTOG value. |



- MULTIPLIER MODE V-PATTERN GROUP PROPERTIES:**
- ¹START POLARITY (STARTPOL = 0).
 - ²FIRST, SECOND, AND THIRD TOGGLE POSITIONS (VTOG1 = 2, VTOG2 = 9).
 - ³LENGTH OF VPAT COUNTER (VLEN = 4); THIS IS THE MINIMUM RESOLUTION FOR TOGGLE POSITION CHANGES.
 - ⁴TOGGLE POSITIONS OCCUR AT LOCATION EQUAL TO (VTOG × VLEN).
 - ⁵IF SWEEP REGION IS ENABLED, THE V-PULSES MAY ALSO CROSS THE HD BOUNDRIES, AS SHOWN ABOVE.

Figure 49. Example of Multiplier Region for Wide Vertical Pulse Timing

06891-050

Vertical Sensor Gate (Shift Gate) Patterns

In an interline CCD, the vertical sensor gate (VSG) pulses are used to transfer the pixel charges from the light-sensitive image area into light-shielded vertical registers. From the light-shielded vertical registers, the image is clocked out line-by-line using the vertical transfer pulses (XV signals) in conjunction with the high speed horizontal clocks. The AD9992 has 24 vertical signals, and each signal can be assigned as a VSG pulse instead of an XV pulse.

Table 18 summarizes the VSG control registers, which are mostly located in the field registers space (see Table 16). The VSGSELECT register (Address 0x1C in the fixed address space) determines which vertical outputs are assigned as VSG pulses. When a signal is selected to be a VSG pulse, only the starting polarity and two of the V-pattern toggle positions are used. The VSGPATSEL register in the sequence registers is used to assign either TOG1 and TOG2 or TOG3 and TOG4 to the VSG signal.

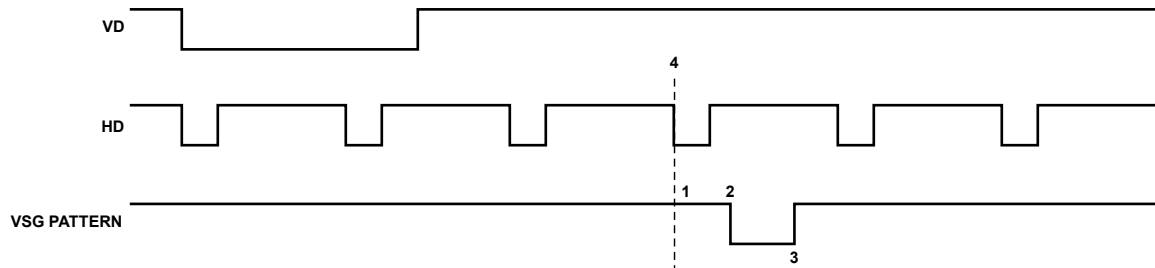
Note that only two of the four V-pattern toggle positions are available when a vertical signal is selected to be a VSG pulse.

The SGACTION1 and SGACTION2 registers are used to select which line in the field is the VSG line. The VSG active line location is used to reference when the substrate clocking (SUBCK) signal begins to operate in each field. For more information, see the Substrate Clock Operation (SUBCK) section.

Also located in the field registers, the SGMASK register selects which individual VSG pulses are active in a given field. Therefore, all SG patterns to be preprogrammed into the V-pattern registers and the appropriate pulses for the different fields can be enabled separately.

Table 18. VSG Control Registers (also see Field Registers in Table 16)

| Register | Length | Range | Description |
|---|--------|--------------------|---|
| VSGSELECT (Located in Fixed Address Space, 0x1C) | 24b | High/low | Selection of VSG signals from XV signals. Set to 1 to make signal a VSG. [0]: XV1 selection (0 = XV pulse; 1 = VSG pulse). [1]: XV2 selection. ... [23]: XV24 selection. |
| VSGPATSEL | 24b | High/low | When VSG signal is selected using the VSGSELECT register, VSGPATSEL selects which V-pattern toggle positions are used. When set to 0, Toggle 1 and Toggle 2 are used. When set to 1, Toggle 3 and Toggle 4 are used. [0]: XV1 selection (0 = use TOG1, TOG2; 1 = use TOG3, TOG4). [1]: XV2 selection. ... [23]: XV24 selection. |
| SGMASK | 24b | High/low, each VSG | Set high to mask each individual VSG output. [0]: XV1 mask. ... [23]: XV24 mask. |
| SGACTION1 | 13b | 0 to 8191 line no. | Selects the line in the field where the VSG signals are active. |
| SGACTION2 | 13b | 0 to 8191 line no. | Selects a second line in the field to repeat the VSG signals. If not used, set this equal to SGACTION1 or to the maximum value. |



PROGRAMMABLE SETTINGS FOR EACH PATTERN:
¹START POLARITY OF PULSE (FROM VPOL IN SEQUENCE REGISTERS).
²FIRST TOGGLE POSITION (FROM V-PATTERN REGISTERS).
³SECOND TOGGLE POSITION (FROM V-PATTERN REGISTERS).
⁴ACTIVE LINE FOR VSG PULSES WITHIN THE FIELD (FROM FIELD REGISTERS).

Figure 50. Vertical Sensor Gate Pulse Placement

058B1051

MODE Registers

The MODE registers are used to select the field timing of the AD9992. Typically, all of the field, V-sequence, and V-pattern information is programmed into the AD9992 at startup. During operation, the MODE registers allow the user to select any combination of field timing to meet the requirements of the system. The advantage of using the MODE registers in conjunction with preprogrammed timing is that it greatly reduces the system programming requirements during camera operation. Only a few register writes are required when the camera operating mode is changed, rather than having to program all of the vertical timing information with each camera mode change.

A basic still camera application can require six fields of vertical timing—one for draft mode operation, one for autofocusing, and four for still image readout. All of the register timing information for the six fields is loaded at startup. Then, during camera operation, the MODE registers select which field timing is active, depending on how the camera is being used.

Table 19 shows how the MODE registers are used. The MODE register (Address 0x2A) specifies how many total fields are used. Any value from 1 to 7 can be selected using these three bits. The other two registers (0x2B and 0x2C) are used to select

which of the programmed fields are used and in which order. Up to seven fields can be used in a single MODE write. The AD9992 starts with the field timing specified by FIELD0, and on the next VD, switches to the timing specified by FIELD1, and so on. After completing the total number of fields specified by MODE, the AD9992 repeats by starting at the first field. This continues until a new write to the MODE register occurs. Figure 53 shows example MODE register settings for different field configurations.

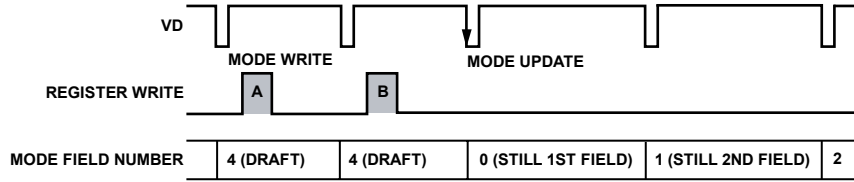
Note that only a write to Address 0x2C properly resets the field counter. Therefore, when changing the values in any of the mode registers, it is recommended that all three registers are updated together in the same field (VD period).

Caution

The MODE registers are SCK updated by default. If they are configured as VD-updated registers by writing Address 0xB4 = 0x03FF and Address 0xB5 = 0xFC00, the new MODE information is updated on the second VD falling edge after the write occurs, rather than on the first VD falling edge. See Figure 52 for an example.

Table 19. MODE Registers—VD Updated

| Address | Name | Length | Description |
|---------|--------|--------|--|
| 2A | MODE | 3b | Total number of fields to cycle through. Set from 1 to 7. |
| 2B | FIELD0 | 5b | Selected FIELD (from FIELD registers in configurable memory) for the first field to cycle through. |
| | FIELD1 | 5b | Selected FIELD (from FIELD registers in configurable memory) for the second field to cycle through. |
| | FIELD2 | 5b | Selected FIELD (from FIELD registers in configurable memory) for the third field to cycle through. |
| | FIELD3 | 5b | Selected FIELD (from FIELD registers in configurable memory) for the fourth field to cycle through. |
| | FIELD4 | 5b | Selected FIELD (from FIELD registers in configurable memory) for the fifth field to cycle through. |
| 2C | FIELD5 | 5b | Selected FIELD (from FIELD registers in configurable memory) for the sixth field to cycle through. |
| | FIELD6 | 5b | Selected FIELD (from FIELD registers in configurable memory) for the seventh field to cycle through. |

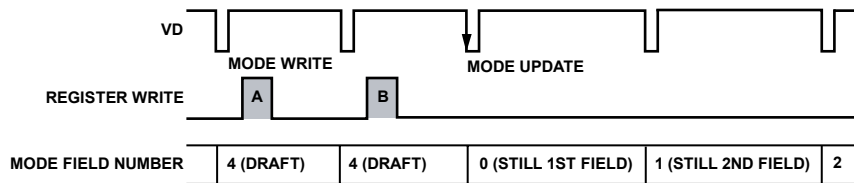


EXAMPLE MODE REGISTER CHANGE:
 REGISTER WRITE A—WRITE TO MODE REGISTERS 0x2A, 0x2B, 0x2C TO SPECIFY CHANGE FROM DRAFT MODE (FIELD4) TO STILL MODE (FIELD0/1/2/3).
 REGISTER WRITE B—WRITE TO VGA GAIN OR ANY NEW REGISTER VALUES NEEDED FOR STILL FRAME OPERATION, SUCH AS NEW FIELD INFORMATION.

NOTES
 1. NEW MODE INFORMATION IS UPDATED AT SECOND VD FALLING EDGE AFTER SERIAL WRITE A.

05891-053

Figure 51. Update of MODE Register, SCK Updated (Default Setting)



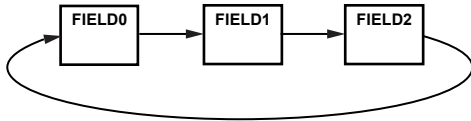
EXAMPLE MODE REGISTER CHANGE:
 REGISTER WRITE A—WRITE TO MODE REGISTERS 0x2A, 0x2B, 0x2C TO SPECIFY CHANGE FROM DRAFT MODE (FIELD4) TO STILL MODE (FIELD0/1/2/3).
 REG. WRITE B—WRITE TO VGA GAIN OR ANY NEW REGISTER VALUES NEEDED FOR STILL FRAME OPERATION, SUCH AS NEW FIELD INFORMATION.

NOTES
 1. NEW MODE INFORMATION IS UPDATED AT SECOND VD FALLING EDGE AFTER SERIAL WRITE A.

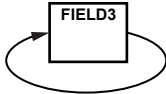
05891-053

Figure 52. Update of MODE Register if Changed to VD-Updated Register

EXAMPLE 1:
 TOTAL FIELDS = 3, FIRST FIELD = FIELD0, SECOND FIELD = FIELD1, THIRD FIELD = FIELD2
 MODE SETTINGS:
 0x2A = 0x3
 0x2B = 0x820
 0x2C = 0x0



EXAMPLE 2:
 TOTAL FIELDS = 1, FIRST FIELD = FIELD3
 MODE SETTINGS:
 0x2A = 0x1
 0x2B = 0x3
 0x2C = 0x0



EXAMPLE 3:
 TOTAL FIELDS = 4, FIRST FIELD = FIELD5, SECOND FIELD = FIELD1, THIRD FIELD = FIELD4, FOURTH FIELD = FIELD2
 MODE SETTINGS:
 0x2A = 0x4
 0x2B = 0x11025
 0x2C = 0x0

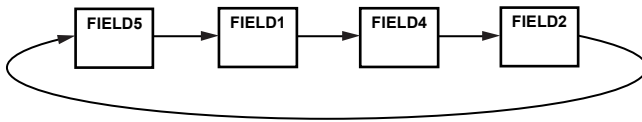


Figure 53. Using the MODE Registers to Select Field Timing

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VERTICAL TIMING EXAMPLE

To better understand how the AD9992 vertical timing generation is used, consider the example CCD timing chart in Figure 54. This example illustrates a CCD using a general 3-field readout technique. As described in the previous field section, each readout field must be divided into separate regions to perform each step of the readout. The sequence change positions (SCP) determine the line boundaries for each region, and the SEQx registers assign a particular V-sequence to each region. The V-sequences contain the specific timing information required in each region: V1 to V6 pulses (using V-pattern groups), HBLK/CLPOB timing, and VSG patterns for the SG active lines.

This timing example requires four regions for each of the three fields, labeled Region 0, Region 1, Region 2, and Region 3. Because the AD9992 allows many individual fields to be programmed, FIELD0, FIELD1, and FIELD2 can be used to meet the requirements of this timing example. The four regions for each field are very similar in this example, but the individual registers for each field allow flexibility to accommodate other timing charts.

Region 0 is a high speed, vertical shift region. Sweep mode can be used to generate this timing operation with the desired number of high speed vertical pulses needed to clear any charge from the CCD's vertical registers.

Region 1 consists of only two lines and uses standard single-line, vertical shift timing. The timing of this region area is the same as the timing in Region 3.

Region 2 is the sensor gate line where the VSG pulses transfer the image into the vertical CCD registers. This region might require the use of the second V-pattern group for the SG active line.

Region 3 also uses the standard single-line, vertical shift timing, the same timing as Region 1. Four regions are required in each of the three fields.

The timing for Region 1 and Region 3 is essentially the same, reducing the complexity of the register programming. Other registers need to be used during the actual readout operation. These include the MODE registers, shutter control registers (PRIMARY_ACTION, SUBCK, GPO for MSHUT, and VSUB control) and AFE gain register.

Important Note Regarding Signal Polarities

When programming the AD9992 to generate the V1 to V24 and SUBCK signals, the external V-driver circuit usually inverts these signals. Carefully check the required timing signals needed at the input and the output of the V-driver circuit being used and adjust the polarities of the AD9992 outputs accordingly.

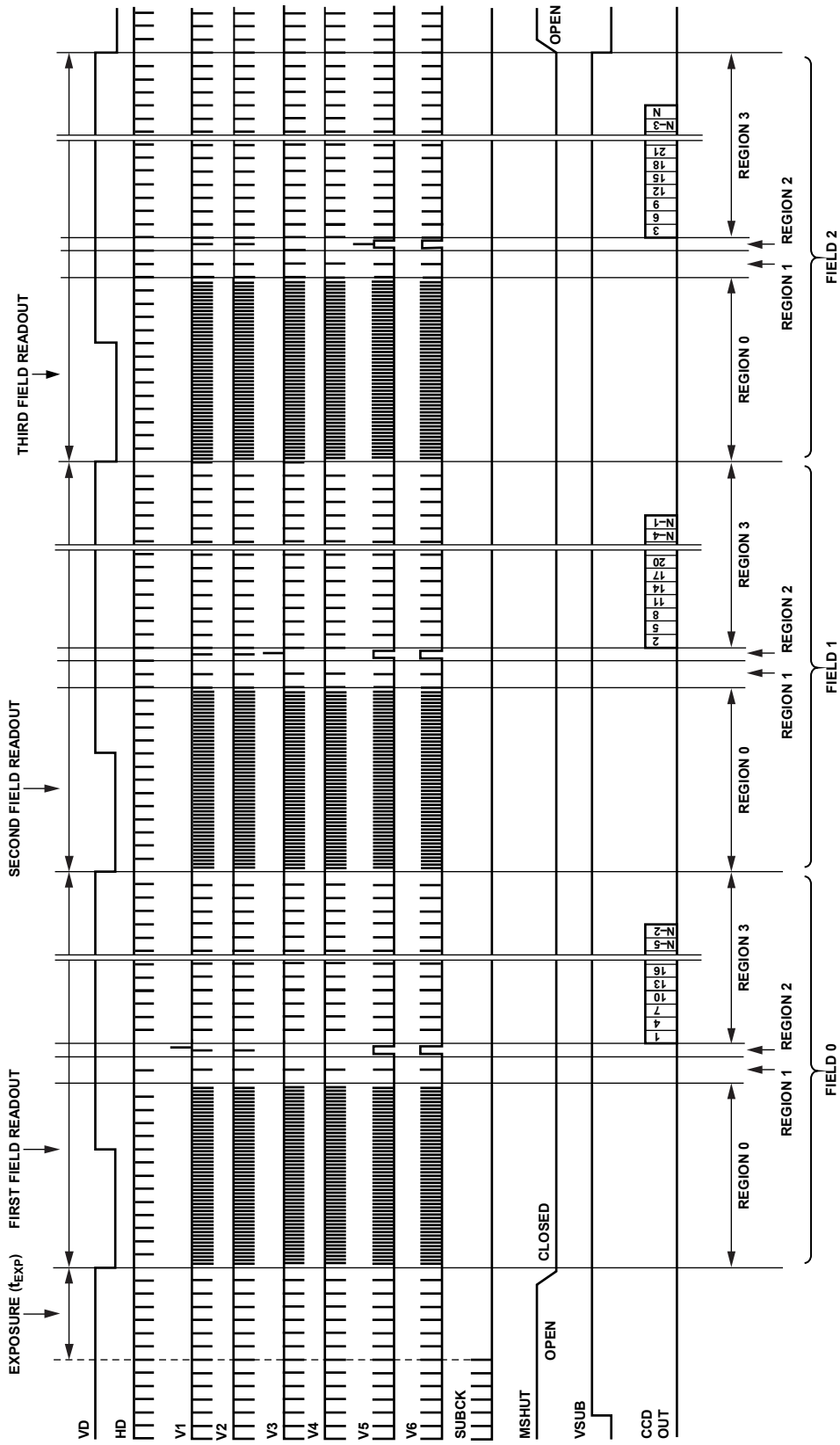


Figure 54. CCD Timing Example—Dividing Each Field into Regions

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SHUTTER TIMING CONTROL

The AD9992 supports the generation of electronic shuttering (SUBCK) and also features flexible general-purpose outputs (GPO) to control mechanical shuttering, CCD substrate bias switching, and strobe circuitry. In the following documentation, the terms sense gate (SG) and vertical sense gate (VSG) are used interchangeably.

SUBSTRATE CLOCK OPERATION (SUBCK)

The CCD image exposure time is controlled by the substrate clock signal (SUBCK), which pulses the CCD substrate to clear out accumulated charge. The AD9992 supports three types of electronic shuttering: normal, high precision, and low speed. Along with the SUBCK pulse placement, the AD9992 can accommodate different readout configurations to further suppress the SUBCK pulses during multiple field readouts.

The SUBCK signal is a programmable string of pulses, each occupying a line following the primary sense gate active line, SGACTLINE1 (registers are shown in Table 20). The SUBCK signal has programmable pulse width, line placement, and number of pulses to accurately control the exposure time.

SUBCK: Normal Operation

By default, the AD9992 operates in the normal SUBCK configuration, in which the SUBCK signal is pulsing in every VD field (see Figure 55). The SUBCK pulse occurs once per line, and the total number of repetitions within the field determines the length of the exposure time. The SUBCK pulse polarity and toggle positions within a line are programmable using the SUBCK_POL and SUBCK_TOG1 registers (see Table 20). The number of SUBCK pulses per field is programmed in the SUBCKNUM register (Address 0x75).

As shown in Figure 55, the SUBCK pulses always begin in the line following the SG-active line, which is specified in the SGACTLINE registers for each field. The SUBCK_POL, SUBCK_TOG1, SUBCK_TOG2, SUBCKNUM, and SUBCKSTARTLINE registers are updated at the start of the line after the sensor gate line, as described in the Updating New Register Values section.

SUBCK: High Precision Operation

High precision shuttering is used in the same manner as normal shuttering but uses an additional register to control the last SUBCK pulse. In this mode, the SUBCK still pulses once per line, but the last SUBCK in the field has an additional SUBCK pulse, whose location is determined by the SUBCKHP_TOG registers, as shown in Figure 56. Finer resolution of the exposure time is possible using this mode. Leaving the SUBCKHP_TOG registers set to its maximum value (0xFFFFF) disables the last SUBCK pulse (default setting).

SUBCK: Low Speed Operation

Normal and high precision shutter operations are used when the exposure time is less than 1 field. For exposure times greater than 1 field, the low speed (LS) shutter features can be used. The AD9992 includes a field counter (primary field counter) to regulate long exposure times. The primary field counter must be activated (Address 0x70) to serve as the trigger for the LS operation. The durations of the LS exposure and read are specified by the SGMASK_NUM and SUBCKMASK_NUM register (Address 0x74), respectively. As shown in Figure 57, this mode suppresses the SUBCK and VSG outputs for up to 8192 fields (VD periods).

To activate an LS shutter operation, trigger the start of the exposure by writing to the PRIMARY_ACTION register bits according to the desired effect. When the primary counter is activated, the next VD period becomes the first active period of the exposure for which the VSG and SUBCK masks are applied.

Optionally, if the SUBCKMASK_SKIP1 register is enabled, the AD9992 ignores the first VSG and SUBCK masks in the subsequent fields. This is generally desired so that the exposure time begins in the field after the exposure operation is initiated. Figure 57 shows operation with SUBCKMASK_SKIP1 = 1.

If the PRIMARY_ACTION register is used while the SUBCKMASK_NUM and SGMASK_NUM registers are set to 0, the behavior of the SUBCK and VSG signals are not different from the normal shutter or high precision shutter operations. Therefore, the primary field counter can be used for other tasks (described in the General-Purpose Outputs (GPOS) section) without disrupting the normal activity. In addition, there exists a secondary field counter that has no effect on the SUBCK and VSG signals. These counters are described in detail in the Field Counters section.

SUBCK Start Line

By default, the SUBCK pulses begin in the line following SGACTLINE1. For applications where the SUBCK pulse should be suppressed for one or more lines following the VSG line, the SUBCKSTARTLINE register can be programmed. This register setting delays the start of the SUBCK pulses until the specified number of lines following SGACTLINE1.

Caution

A value of 1 should not be used in the SUBCKSTARTLINE register. A value of 0 is used to specify the SUBCK pulses to begin in the next line after the SG line. A value of 2 is used to specify the SUBCK pulses to begin two lines after the SG line, and so on.

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Read After Exposure

To read the CCD data after exposure, the SG should resume normal activity while the SUBCK remains null. By default, the AD9992 generates the VSG pulses in every field. When only a single exposure and a single frame read is desired, such as is the case in the preview mode, the VSG and SUBCK pulses can operate in every field.

Other applications require that a greater number of frames are read, in which case SUBCK must be masked until the readout is

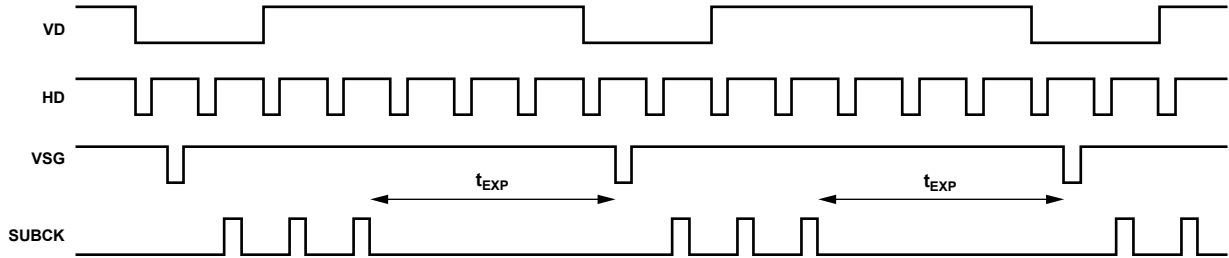
finished. The SUBCKMASK_NUM register specifies the total number of fields (exposure and read) to mask SUBCK. A 2-field CCD frame read mode typically requires two additional fields of SUBCK masking (SUBCKMASK_NUM = 2). A 3-field, 6-phase CCD requires three additional fields of SUBCK masking after the read begins (SUBCKMASK_NUM = 3).

Note that the SUBCKMASK_SKIP1 register setting allows SUBCK pulses at the beginning of the field of exposure.

Table 20. SUBCK and Exposure/Read Register Parameters

| Register | Length | Range | Description |
|-----------------------------|--------|----------------------------|--|
| SGMASK_NUM | 13b | 0 to 8191 no. of fields | Exposure duration (number of fields to suppress VSG) for LS operation. |
| SUBCKMASK_NUM | 13b | 0 to 8191 no. of fields | Exposure plus readout duration (number of fields to suppress SUBCK) for LS. |
| SUBCKMASK_SKIP1 | 1b | On/off | Suppress SG/SUBCK masks for one field (default = 0). Typically set to 1. |
| SUBCKSTARTLINE ¹ | 13b | 0, 2 to 8191 line location | Line location to start the SUBCK pulses, relative to SGLINE location. A value of 1 is invalid. See the SUBCK Start Line section. |
| SUBCKNUM ¹ | 13b | 1 to 8191 no. of pulses | Total number of SUBCKs per field, at 1 pulse per line. Must be <VDLEN. |
| SG_SUPPRESS ¹ | 1b | On/off | Suppress the SG and allow SUBCK to finish at SUBCKNUM. |
| SUBCK_TOG1 | 13b | 0 to 8191 pixel locations | SUBCK Toggle Position 1. |
| SUBCK_TOG2 | 13b | 0 to 8191 pixel locations | SUBCK Toggle Position 2. |
| SUBCK_POL | 1b | Low/high | SUBCK start polarity. |
| SUBCKHP_TOG1 | 13b | 0 to 8191 pixel locations | Hi-precision SUBCK Toggle Position 1. Selectable as SG or VD updated. |
| SUBCKHP_TOG2 | 13b | 0 to 8191 pixel locations | Hi-precision SUBCK Toggle Position 2. Selectable as SG or VD updated. |

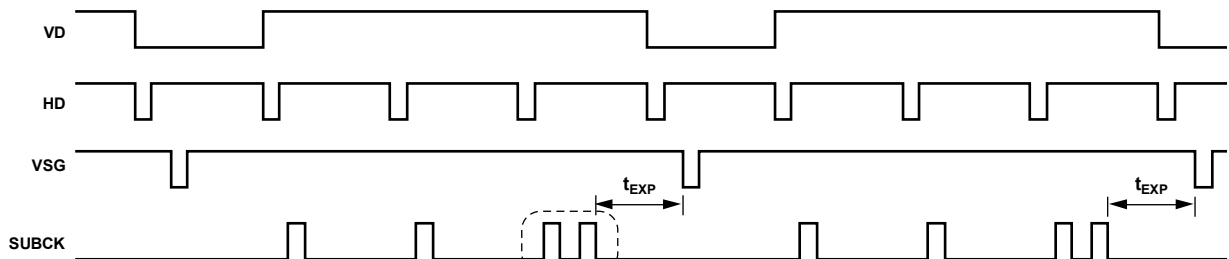
¹ Register is not VD updated but is updated at the start of the line after the sensor gate line.



- SUBCK PROGRAMMABLE SETTINGS:**
1. PULSE POLARITY USING THE SUBCK_POL REGISTER.
 2. NUMBER OF PULSES WITHIN THE FIELD USING THE SUBCKNUM REGISTER (SUBCKNUM = 3 IN THE ABOVE EXAMPLE).
 3. PIXEL LOCATION OF PULSE WITHIN THE LINE AND PULSE WIDTH PROGRAMMED USING THE SUBCK1 TOGGLE POSITION REGISTERS.

Figure 55. Normal SUBCK Operation

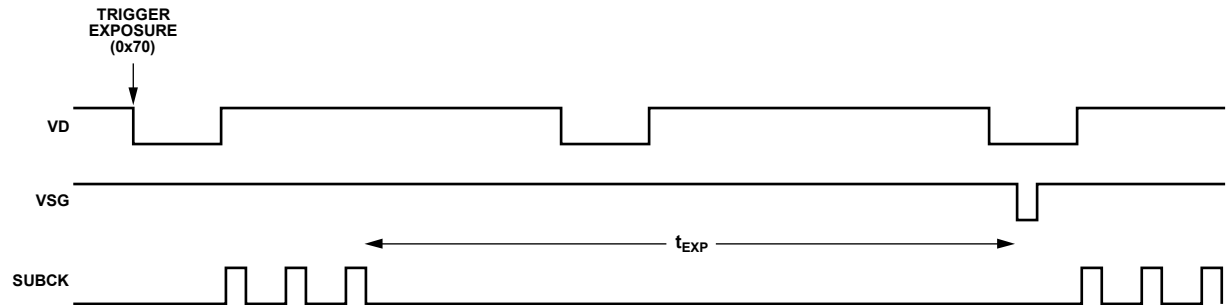
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- NOTES**
1. SECOND SUBCK PULSE IS ADDED IN THE LAST SUBCK LINE.
 2. LOCATION OF SECOND PULSE IS FULLY PROGRAMMABLE USING THE SUBCKHP TOGGLE POSITION REGISTERS.

Figure 56. High Precision SUBCK Operation

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- NOTES**
1. SUBCK CAN BE SUPPRESSED FOR MULTIPLE FIELDS BY PROGRAMMING THE EXPOSURE REGISTER TO BE GREATER THAN 0.
 2. ABOVE EXAMPLE USES EXPOSURE = 1.
 3. TRIGGER REGISTER MUST ALSO BE USED TO START THE LOW SPEED EXPOSURE.
 4. VD/HD OUTPUTS CAN ALSO BE SUPPRESSED USING THE VDHDOFF REGISTER = 1.

Figure 57. Low Speed SUBCK Operation

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FIELD COUNTERS

The AD9992 contains three field counters (primary, secondary, and mode). When these counters are active, they increment with each VD cycle. The mode counter is the field counter used with the mode register to control the vertical timing signals, which was discussed in the MODE Registers section. The primary and secondary counters are more flexible and are generally used for shuttering signal applications. Both the primary and secondary counters have several modes of operation that are dictated by Address 0x70, including

- Normal (single count)
- RapidShot (repeating count)
- ShotDelay (delayed count)

- ShotDelay with RapidShot
- Manual exposure
- Manual readout
- Force to idle

The primary counter regulates the expose and read actions by regulating the SUBCK and VSG signals. In addition, if the RapidShot feature is used with the primary counter, the SUBCK and VSG masking automatically repeats as necessary for multiple expose/read cycles. The secondary counter has no effect on the SUBCK or VSG signal. Both counters can be used to regulate the general-purpose signals described in the General-Purpose Outputs (GPOS) section.

Table 21. Primary/Secondary Field Counter Registers (Address 0x70, Address 0x71, and Address 0x72)

| Register | Length | Description |
|--|------------------------|--|
| PRIMARY_ACTION SECOND_ACTION | 3b 3b | 0: idle, no counter action. GPO signals can still be controlled using polarity or GP_PROTOCOL = 1. 1: activate counter. Single cycle of counter from 1 to counter maximum value, and then returns to idle state. 2: RapidShot. After reaching maximum counter value, counter wraps and repeats until reset. 3: ShotTimer. Active single cycle of counter after added delay of N fields (use the corresponding DELAY register). 4: ShotTimer with RapidShot. Same as 2, with added delay of N fields between each repetition. 5: manual exposure. Primary counter stays in exposure until manual readout or reset to idle. This mode keeps the SUBCK and VSG pulses masked indefinitely. 6: manual readout. Primary counter switches to readout (VSG pulses becomes active). 7: force to idle. |
| PRIMARY_MAX SECOND_MAX VDHD_MASK | 13b 12b 3b | Primary counter maximum value. Secondary counter maximum value. Mask VD/HD during counter operation. |
| PRIMARY_DELAY PRIMARY_SKIP SECOND_DELAY SECOND_SKIP | 13b 1b 13b 1b | ShotTimer. Number of fields to delay before the next primary count (exposure) starts. If using ShotTimer with RapidShot, delay value is used between each repeat. When using ShotTimer with RapidShot, use primary delay value only before first count (exposure). ShotTimer. Number of fields to delay before the next secondary count starts. If using ShotTimer with RapidShot, delay value is used between each repeat. When using ShotTimer with RapidShot, use secondary delay value only before first count. |

GENERAL-PURPOSE OUTPUTS (GPOS)

The AD9992 provides programmable outputs to control a mechanical shutter, strobe/flash, the CCD bias select signal, or any other external component with general-purpose (GP) signals. Eight GP signals, with up to four toggles each, are available that can be programmed and assigned to special GPO pins. These pins are bidirectional and allow visibility (as an output) and external control (as an input) of HBLK, PBLK, CLPOB, and OUTCONTROL. The registers introduced in this section are described in Table 22.

GP Toggles

When configured as an output, each GPO1 to GPO8 output can deliver a signal that is the result of programmable toggle positions. The GP signals are independent and can be linked to either a specific VD period or over a range of VD periods via the primary or secondary field counters through the GP protocol register (Address 0x73). As a result of their associations with the field counters, the GP toggles inherit the characteristics of the field counters, such as RapidShot and ShotDelay. To use the GP toggles

1. Program the toggle positions (Address 0x7A to Address 0xA9).
2. Program the protocol (Address 0x73).
3. Program the counter parameters (Address 0x71 to Address 0x72).
4. Activate the counter (Address 0x70).

For Protocol 1 (no counter association), skip Steps 3 and 4.

With these four steps, the GP signals can be programmed to accomplish many common tasks. Careful protocol selection and application of the field counters yields efficient results to allow the GP signals smooth integration with concurrent operations.

Note that the SUBCK and VSG masks are linked to the primary counter; however, if their parameters are 0, the GPO can use the primary counter without expose/read activity.

The secondary counter is independent and can be used simultaneously with the primary counter. Some applications may require the use of both primary and secondary field counters with different GPO protocols, start times, and durations. Such operations are easily handled by the AD9992.

Several simple examples of GPO applications using only one GPO and one field counter follow. These examples can be used as building blocks for more complex GPO activity. In addition, specific GPO signals can be passed through a 4-input LUT to realize combinational logic between them. For example, GP1 and GP2 can be sent through an XOR look-up table, and the result can be delivered on GP1, GP2, or both. Also, either GP1 or GP2 can deliver their original toggles.

Table 22. GPO Registers

| Register | Length | Range | Description |
|---------------|--------|---------------|--|
| GP1_PROTOCOL | 3b | 0 to 7 | 0: idle. |
| GP2_PROTOCOL | 3b | 0 to 7 | 1: no counter association, use MANUAL_TRIG bits to enable each GP signal. |
| GP3_PROTOCOL | 3b | 0 to 7 | 2: link to primary counter. |
| GP4_PROTOCOL | 3b | 0 to 7 | 3: link to secondary counter. |
| GP5_PROTOCOL | 3b | 0 to 7 | 4: link to mode counter (from vertical timing generation). |
| GP6_PROTOCOL | 3b | 0 to 7 | 5: primary repeat (allows GP signals to repeat with RapidShot). |
| GP7_PROTOCOL | 3b | 0 to 7 | 6: secondary repeat (allows GP signals to repeat with RapidShot). |
| GP8_PROTOCOL | 8b | 0 to 7 | 7: keep on. |
| MANUAL_TRIG | 8b | Off/on | Manual trigger for each GP signal, for use with Protocol 1. |
| GP<1:8>_POL | 8b | Low/high | Starting polarity for GP signals, only updated during PROTOCOL = 0. |
| SEL_GP<1:8> | 8b | Off/on | 1: select GP toggles visible at GPO1 to GPO8 when output is enabled (default); 0: select vertical signals visible at GPO4 to GPO8 when output is enabled. GPO4: SUBCK. GPO5: XV21. GPO6: XV22. GPO7: XV23. GPO8: XV24. |
| GPO_OUTPUT_EN | 8b | Off/on | 1: enable GPO1 to GPO8 outputs (one bit per output); 0: disable GPO1 to GPO8 outputs, pins will be high-Z state (default). |
| GP*_USE_LUT | 8b | Off/on | Send GP signals through a programmable look-up table (LUT). |
| LUT_FOR_GP12 | 4b | Logic setting | Desired logic to be realized on GP1 combined with GP2. |
| LUT_FOR_GP34 | 4b | Logic setting | Desired logic to be realized on GP3 combined with GP4. |

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| Register | Length | Range | Description |
|--------------|--------|-----------------|--|
| LUT_FOR_GP56 | 4b | Logic setting | Desired logic to be realized on GP5 combined with GP6. |
| LUT_FOR_GP78 | 4b | Logic setting | Desired logic to be realized on GP7 combined with GP8. Example logic settings for LUT_FOR_GPxy: 0x6 = GPy XOR GPx (see Figure 63). 0x7 = GPy NAND GPx. 0x8 = GPy AND GPx. 0xE = GPy OR GPx. |
| GP*_TOG*_FD | 13b | 0 to 8191 field | Field of activity, relative to primary and secondary counter for corresponding toggle. |
| GP*_TOG*_LN | 13b | 0 to 8191 line | Line of activity for corresponding toggle. |
| GP*_TOG*_PX | 13b | 0 to 8191 pixel | Pixel of activity for corresponding toggle. |
| GPO_INT_EN | 1b | Off/on | When set to 1, internal signals are viewable on GPO5 to GPO8. GPO5: OUTCONTROL. GPO6: HBLK. GPO7: CLPOB. GPO8: PBLK. |

Single-Field Toggles

Single-field toggles occur in the next field only. There can be up to four toggles in the field. The mode is set with GP_PROTOCOL equal to 1, and then the toggles are triggered in the next field by writing to the MANUAL_TRIG register (0x70 [13:6]). In this mode, the field toggle settings must be set to a value of 1. Two consecutive fields do not have activity. If toggles are required to repeat in the next field, the MANUAL_TRIG register can be written to in consecutive fields.

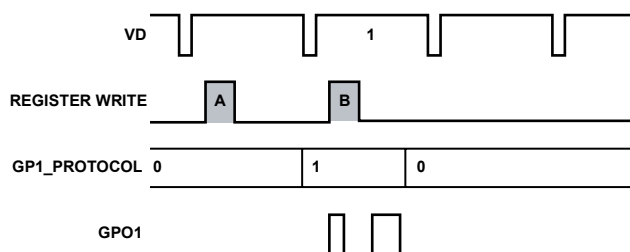
Preparation

The GP toggle positions can be programmed any time prior to use. For example,

```
0x7A ← 0x000A001
0x7B ← 0x0002000
0x7C ← 0x000000F
0x7D ← 0x00C4002
0x7E ← 0x0004000
0x7F ← 0x00000B3
```

Details

```
A) Field 0: 0x70 ← 0x0000040
              0x73 ← 0x0000001
B) Field 1: 0x73 ← 0x0000000
```



NOTES
 1. THE FIELD TOGGLE POSITION MUST BE SET TO 1 WHEN GP_PROTOCOL IS 1.
 CAUTION! THE GP_PROTOCOL MUST BE RESET BEFORE USING AGAIN.

Figure 58. Single-Field Toggles Using GP_PROTOCOL = 1

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Scheduled Toggles

Scheduled toggles are programmed to occur during any upcoming field. For example, there can be one toggle in Field 1, two toggles in Field 3, and a last toggle in Field 4. The mode is set with GP_PROTOCOL = 2 or GP_PROTOCOL = 3. Mode 2 tells the GPO to obey the primary field counter, and Mode 3 tells the GPO to obey the secondary field counter.

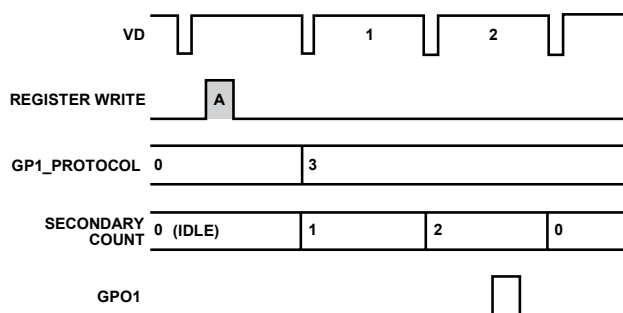
Preparation

The GP toggle positions can be programmed any time prior to use. For example,

```
0x7A ← 0x00C4002
0x7B ← 0x0004000
0x7C ← 0x00000B3
```

Details

```
A) Field 0: 0x70 ← 0x0000008
              0x73 ← 0x0000003
```



CAUTION! THE PRIMARY COUNTER REGULATES THE SUBCK AND VSG ACTIVITY. LINK A GPO TO THE PRIMARY COUNTER ONLY IF IT IS TO HAPPEN DURING EXPOSURE/READ.

Figure 59. Scheduled Toggles Using GP_PROTOCOL = 3

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AD9992

RapidShot Sequences

RapidShot technology provides continuous repetition of scheduled toggles.

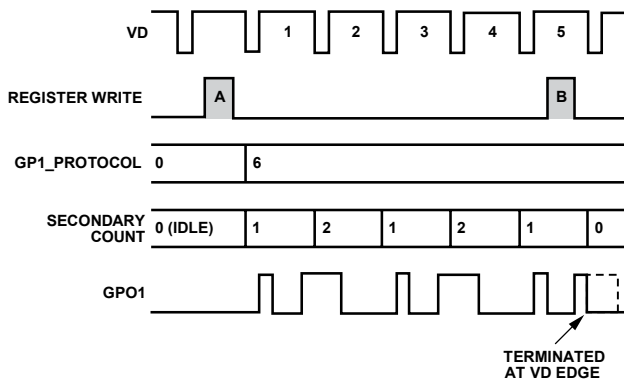
Preparation

The GP toggle positions can be programmed any time prior to use. For example,

```
0x71 ← 0x0004000
0x7A ← 0x000A001
0x7B ← 0x0002000
0x7C ← 0x000000F
0x7D ← 0x00C4002
0x7E ← 0x0004000
0x7F ← 0x00000B3
0x73 ← 0x0000006
```

Details

A) Field 0: 0x70 ← 0x0000010
 B) Field 2: 0x70 ← 0x0000007



NOTES
 1. THE GP PROTOCOLS ARE THE SAME AS THE SCHEDULED TOGGLES, EXCEPT THE TOGGLES CAN BE EXCLUDED FROM REPETITION BY CHOOSING GP PROTOCOL 2 OR 3.
 CAUTION! THE FIELD COUNTER MUST BE FORCED INTO IDLE STATE TO TERMINATE REPETITIONS.

Figure 60. RapidShot Toggle Operation Using GP_PROTOCOL = 6

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ShotDelay Sequences

ShotDelay technology provides internal delay of scheduled toggles. The delay is in terms of fields.

Preparation

The GP toggle positions can be programmed any time prior to use. For example,

```
0x71 ← 0x0004000
0x72 ← 0x000C000
0x7A ← 0x000A001
0x7B ← 0x0002000
0x7C ← 0x000000F
0x73 ← 0x0000003
```

Details

A) Field 0: 0x70 ← 0x0000018

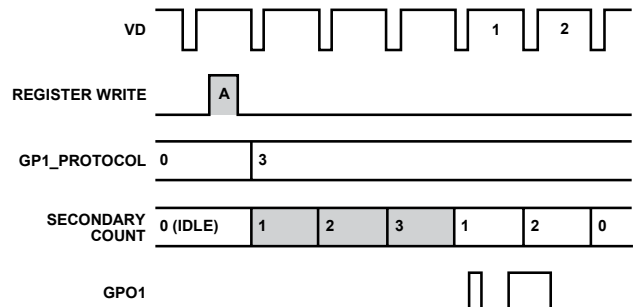


Figure 61. ShotDelay Toggle Operation Using GP_PROTOCOL = 3

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GP LOOK-UP TABLES (LUT)

The AD9992 is equipped with a look-up table for each pair of consecutive GP signals when configured as outputs. GP1 is always combined with GP2, GP3 is always combined with GP4, GP5 is always combined with GP6, and GP7 is always combined with GP8. The external GPO outputs from each pair can output the result of the LUT or the original GP internal signal.

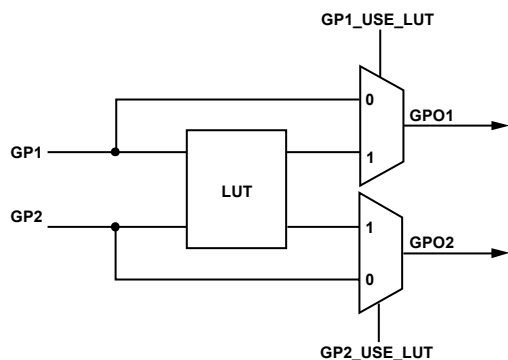
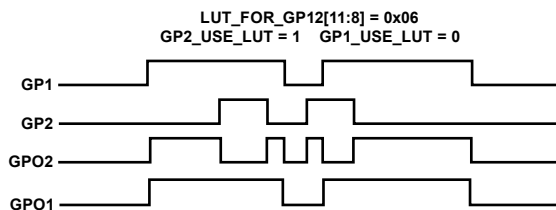


Figure 62. Internal LUT for GP1 and GP2 Signals

Address 0x79 dictates the behavior of the LUT and which signals receive the result. Each 4-bit LUT_FOR_GPxy register can realize any logic combination of GPx and GPy. For example, Table 23 shows how the register values of LUT_FOR_GP12 [11:8] are determined. XOR, NAND, AND, and OR results are shown, but any 4-bit combination is possible. A simple example of XOR gating is shown in Figure 63.

Table 23. LUT Results Based on GP1, GP2 Values

| GP2 | GP1 | LUT: XOR | LUT: NAND | LUT: AND | LUT: OR |
|-----|-----|----------|-----------|----------|---------|
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 |



NOTES
1. LOGIC COMBINATION (XOR) OF PROGRAMMED TOGGLES GP1 AND GP2.

Figure 63. LUT Example for GP1 XOR GP2

Field Counter and GPO Limitations

The following is a summary of the known limitations of the field counters and GPO signals that dictate usability.

- The field counter trigger (PRIMARY_ACTION and SECONDARY_ACTION registers, Address 0x70) is self-reset at the start of every VD period. Therefore, there must be one VD period between sequential programming to that address.
- If GP*_PROTOCOL = 1, it must be manually reset to GP*_PROTOCOL = 0 one VD period before it can be used again. If manual toggles are desired in sequential fields, the MANUAL_TRIG register should be used in conjunction with GP*_PROTOCOL = 1.

COMPLETE EXPOSURE/READOUT OPERATION USING PRIMARY COUNTER AND GPO SIGNALS

Figure 64 demonstrates a typical expose/read cycle while exercising the GPO signals. Using a 3-field CCD with an exposure time that is greater than one field but less than two fields in duration, requires a total of five fields for the entire exposure/readout operation. Other exposure times and other CCD field configurations require modification of these example settings.

Note that if the MODE registers are changed to be VD updated, as shown in the MODE Registers section and in Figure 52, the MODE update will be delayed by one additional field. This should be accounted for in selecting the number of fields to cycle and which VD location to write to the MODE registers.

1. The primary counter is used to control the masking of VSG and SUBCK during exposure/readout. The PRIMARY_MAX register should be set equal to the total number of fields used for exposure and readout. In this example, PRIMARY_MAX = 5.

The SUBCK masking should not occur immediately at the next VD edge (Step 2), because this would define an exposure time that begins in the previous field. Write to the PRIMARY_DELAY register to delay the masking of VSG and SUBCK pulses in the first exposure field. In this example, MASKDELAY = 1.

Write to the SUBCKMASK_NUM register (Address 0x74) to specify the number of fields to mask SUBCK while the CCD data is read. In this example, SUBCKMASK_NUM = 4.

Write to the SGMASK_NUM register (Address 0x74) to specify the number of fields to mask VSG outputs during exposure. In this example, SGMASK_NUM = 1.

Write to the PRIMARY_ACTION register (Address 0x70) to trigger the GP1 (STROBE), GP2 (MSHUT), and GP3 (VSUB) signals and to start the expose/read operation.

Write to the MODE registers to configure the next five fields. The first two fields during exposure are the same as the current draft mode fields, and the following three fields are the still-frame readout fields. The register settings for the draft mode field and the three readout fields are previously programmed. Note that if the MODE registers are changed to VD updated, only one field of exposure should be included (the second one) because the MODE settings will be delayed an extra field.

2. VD/HD falling edge updates the serial writes from 1.
3. GP3 (VSUB) output turns on at the field/line/pixel specified. VSUB Example 1 and Example 2 use GP3TOG1_FD = 1.
4. GP1 (STROBE) output turns on and off at the location specified.
5. GP2 (MSHUT) output turns off at the location specified.
6. The next VD falling edge automatically starts the first read field.
7. The next VD falling edge automatically starts the second read field.
8. The next VD falling edge automatically starts the third read field.
9. Write to the MODE register to reconfigure the single draft mode field timing. Note that if the MODE registers are changed to VD updated, this write should occur one field earlier.
10. VD/HD falling edge updates the serial writes from 9. VSG outputs return to draft mode timing. SUBCK output resumes operation. GP2 (MSHUT) output returns to the on position (active or open). GP3 (VSUB) output returns to the off position (inactive).

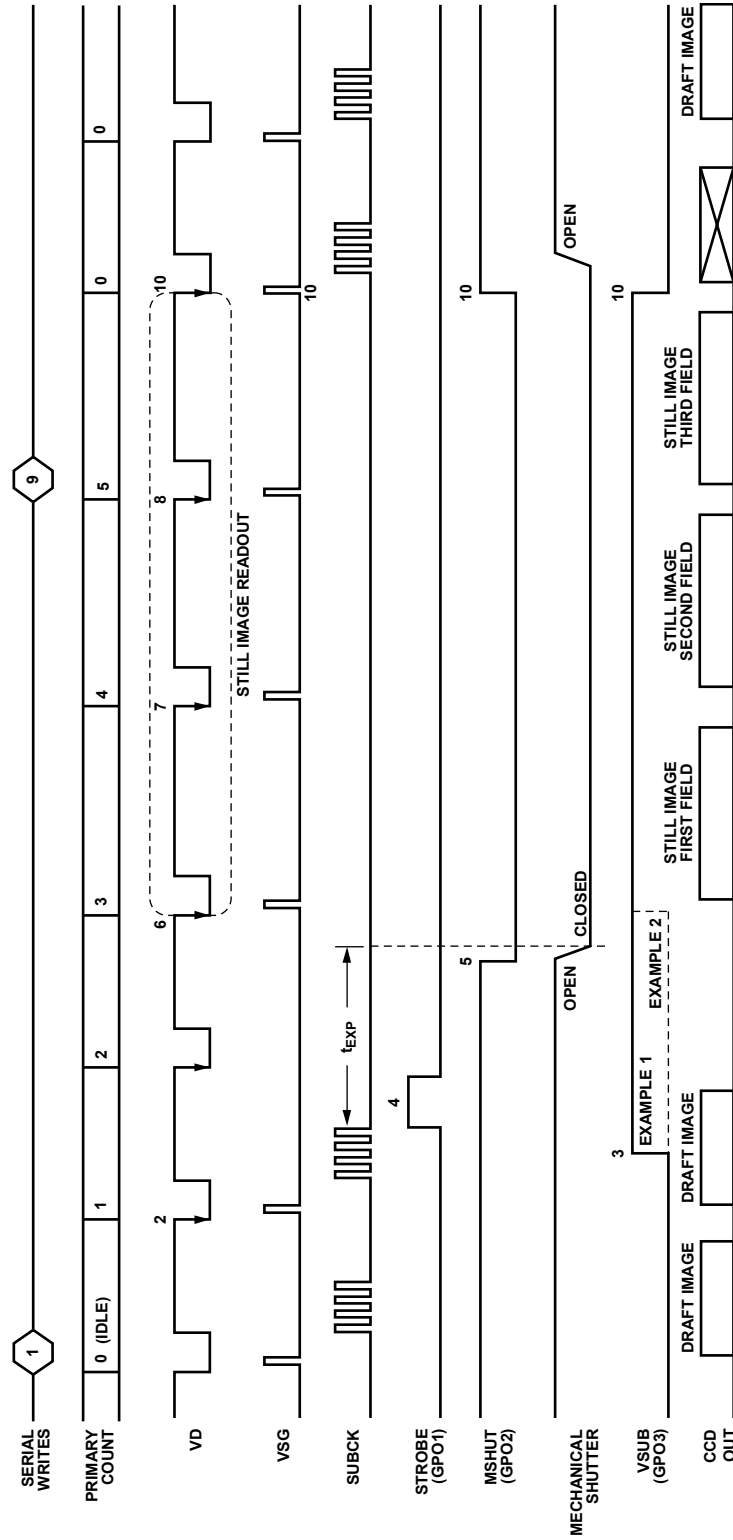


Figure 64. Complete Exposure/Readout Operation Using Primary Counter and GPO Signals

MANUAL SHUTTER OPERATION USING ENHANCED SYNC MODES

The AD9992 also supports an external signal to control exposure, using the SYNC input. Generally, the SYNC input is used as an asynchronous reset signal during master mode operation. When the enhanced SYNC mode is enabled, the SYNC input provides additional control of the exposure operation.

Normal SYNC Mode (Mode 1)

By default, the SYNC input is used in master mode for synchronizing the internal counters of the AD9992 with external timing. The SYNC During Master Mode Operation section describes how horizontal, vertical, and field designator signals are reset by the rising edge of the SYNC pulse. Figure 65 also shows how this mode operates, highlighting the behavior of the mode field designator.

Enhanced SYNC Modes (Modes 2 and 3)

The enhanced SYNC modes can be used to accommodate unique synchronization requirements during exposure operations. In SYNC Mode 2, the V and VSG outputs are suspended and the VD output is masked. The V-outputs are held at the dc value established by the Sequence 0 start polarities. There is no SCP operation, but the H-counter is still enabled. Finally, the AFE sampling clocks, HD, H/RG, CLPOB, HBLK, are operational and use Sequence 0 behavior. See Figure 66 for more details.

To enable the enhanced SYNC modes, set the register ENH_SYNC_EN (Address 0x13 Bit [3]) to 1.

Mode 3 uses all of these features, but the V-outputs are continuous through the SYNC pulse interval. VD control pulses are masked during the SYNC interval, and the HD pulse can also be masked, if required. See Figure 67.

It is important to note that in both of these enhanced modes, the SYNC pulse resets the counters at both the falling edge and the rising edge of the SYNC pulse.

Register Update and Field Designator

When using special SYNC Mode 2 or 3, the VD-updated registers, such as PRIMARY_ACTION, are not updated during the SYNC interval, and the SCP0 function is ignored and held at 0 (see Figure 68).

When using either SYNC Mode 2 or 3, both the rising and falling edges increment the internal field designator; therefore, the new register data takes effect and VTP information is updated to new SEQ0 data. However, this does not occur if the MODE register is to create an output of one field. In that case, the region, sequence, and group information does not change (see Figure 69).

Shutter Operation in SLR Mode

Referring to Figure 70,

1. To turn on VSUB, write to the appropriate GP registers to trigger VSUB and start the manual exposure [PRIMARY_ACTION = 5]. This change takes effect after the next VD, and SUBCK is suppressed during the exposure and readout phases.
2. To turn on MSHUT during the interval between the next VD and SYNC, write to the appropriate GP register. When MSHUT is in the on position, it has line and pixel control. This change takes effect on the SYNC falling edge since there is an internal VD.
3. If the MODE register is programmed to cycle through multiple fields (5, 7, 3, 5, 7, 3, ..., in this example), the internal field designator increments. If the MODE register is not required to increment, set up the MODE register such that it outputs only one field. This prevents the MODE counter from incrementing during the SYNC interval.
4. Write to the manual readout trigger to begin the manual readout [PRIMARY_ACTION = 6]. Write to the appropriate GP registers to trigger MSHUT to toggle low at the end of the exposure. This change takes effect on the SYNC rising edge during readout. Since VD register update is disabled, the trigger takes effect on the SYNC rising edge. The MSHUT falling edge is aligned to the SYNC rising edge. Because the MSHUT falling edge is aligned with VD, it may be necessary to insert a dummy VD to delay the readout.

Note that since the internal exposure counter (PRIMARY counter) is not used during manual SYNC mode operation and the VD register update is disabled, control is lost on the fine placement of the GP signals for VSUB, MSHUT, and STROBE edges while SYNC is low.

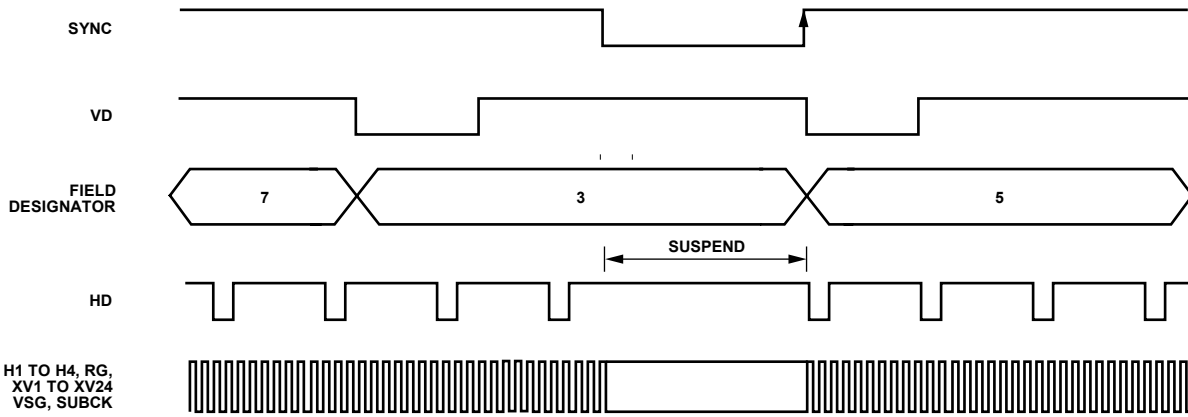
New Serial Registers

SYNC Modes 2 and 3 are controlled using the registers listed in Table 24.

Table 24. Registers for Enhanced SYNC Modes

| Register | Length | Description |
|--------------|--------|--|
| ENH_SYNC_EN | 1b | HI active to enable (default LO) |
| SYNC_MASK_V | 1b | HI active to enable masking (default LO) |
| SYNC_MASK_VD | 1b | HI active to enable masking (default HI) |
| SYNC_MASK_HD | 1b | HI active to enable masking (default HI) |

Note that registers for enhanced SYNC modes are located at Address 0x13 Bits [6:3].

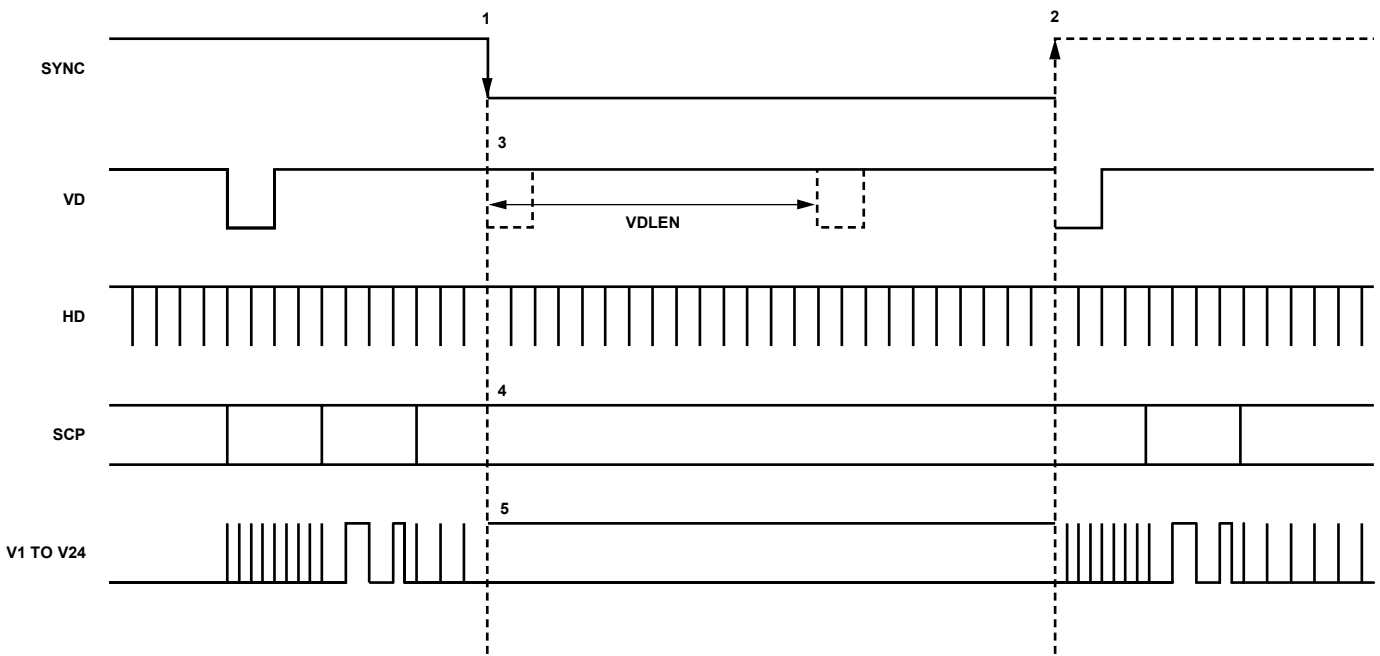


NOTES

1. THE SYNC RISING EDGE RESETS VD/HD AND COUNTERS TO 0.
2. SYNC POLARITY IS PROGRAMMABLE USING SYNCPOL REGISTER (ADDR 0x13).
3. DURING SYNC LOW, ALL INTERNAL COUNTERS ARE RESET AND VD/HD CAN BE SUSPENDED USING THE SYNCSPEND REGISTER (ADDR 0x13).
4. THE SYNC RISING EDGE CAUSES THE INTERNAL FIELD DESIGNATOR TO INCREMENT.
5. IF SYSCSUSPEND = 1, VERTICAL CLOCKS, H1 TO H4, AND RG ARE HELD AT THE SAME POLARITY SPECIFIED BY OUTCONTROL = LOW.
6. IF SYNCSPEND = 0, ALL CLOCK OUTPUTS CONTINUE TO OPERATE NORMALLY UNTIL SYNC RESET EDGE.

Figure 65. Default Mode 1

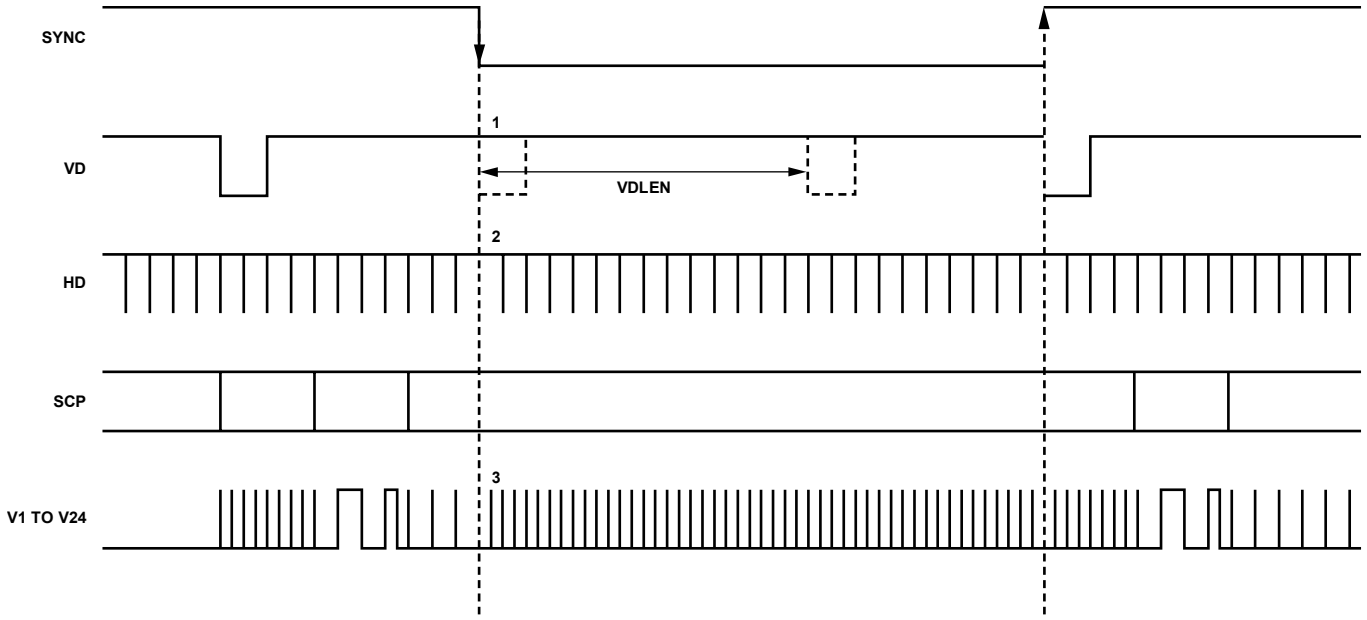
06891-083



- 1 FALLING EDGE RESYNCS THE CIRCUIT TO THE LINE/PIXEL NUMBER 0. VD AND HD INTERNALLY RESYNC.
- 2 RISING EDGE RESETS COUNTERS.
- 3 VD IS DISABLED DURING SYNC. THE REGISTER IS PROGRAMMABLE.
- 4 SCP, HBLK, AND CLPOB ARE HELD AT SEQ0 VALUE.
- 5 V1 TO V24 SIGNALS ARE HELD AT THE V-OUTPUT START POLARITY.

Figure 66. Enhanced SYNC Mode 2 with Vertical Signals Held at VTP Start Value

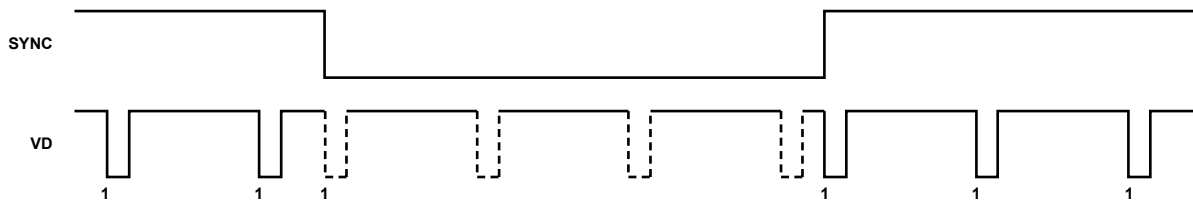
06891-084



¹SYNC_MASK_VD IS A NEW REGISTER. HI WILL MASK VD. DEFAULT = HI.
²SYNC_MASK_HD IS A NEW REGISTER. HI WILL MASK HD. DEFAULT = LO.
³V-OUTPUT PULSES CONTINUE IN SEQUENCE.

Figure 67. Enhanced SYNC Mode 3

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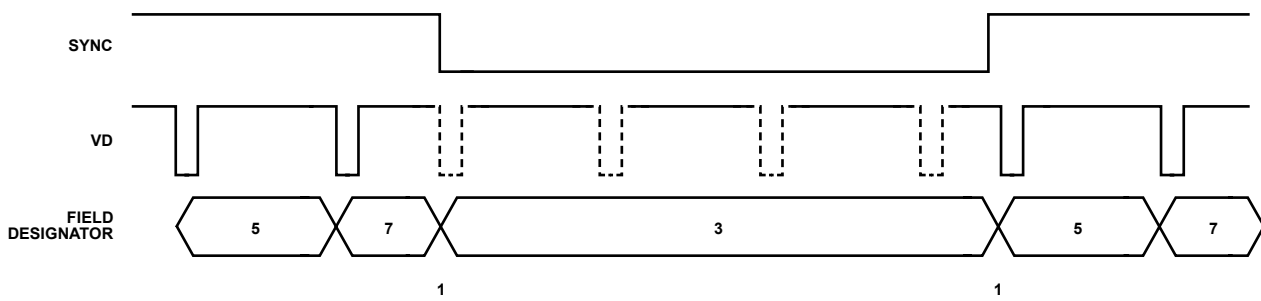
¹VD REGISTERS ARE UPDATED HERE.

NOTES

1. VD-UPDATED REGISTERS (FOR EXAMPLE, PRIMARY_ACTION) ARE DISABLED DURING THE SYNC INTERVAL.

Figure 68. Register Update Behavior

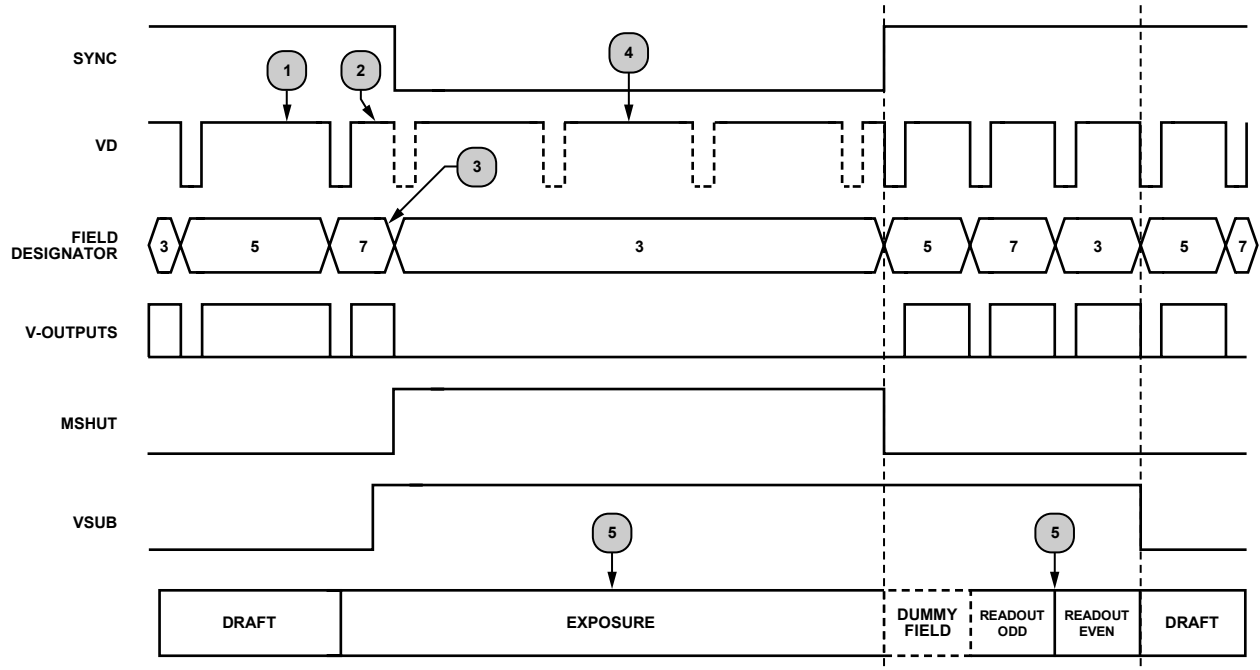
05891-086



¹FIELD DESIGNATOR IS INCREMENTED ON BOTH SYNC EDGES.

Figure 69. Special SYNC Mode Effect on Field Designator

05891-087



- 1SEE THE SHUTTER OPERATION IN SLR MODE SECTION.
- 2SEE THE SHUTTER OPERATION IN SLR MODE SECTION.
- 3SEE THE SHUTTER OPERATION IN SLR MODE SECTION.
- 4SEE THE SHUTTER OPERATION IN SLR MODE SECTION.
- 5SUBCK OUTPUT IS SUPPRESSED DURING EXPOSURE AND READOUT WHEN EXPOSURE TRIGGER IS USED.

Figure 70. Enhanced SYNC Mode—Manual Shutter Operation, SLR Mode

05981-088

ANALOG FRONT-END DESCRIPTION AND OPERATION

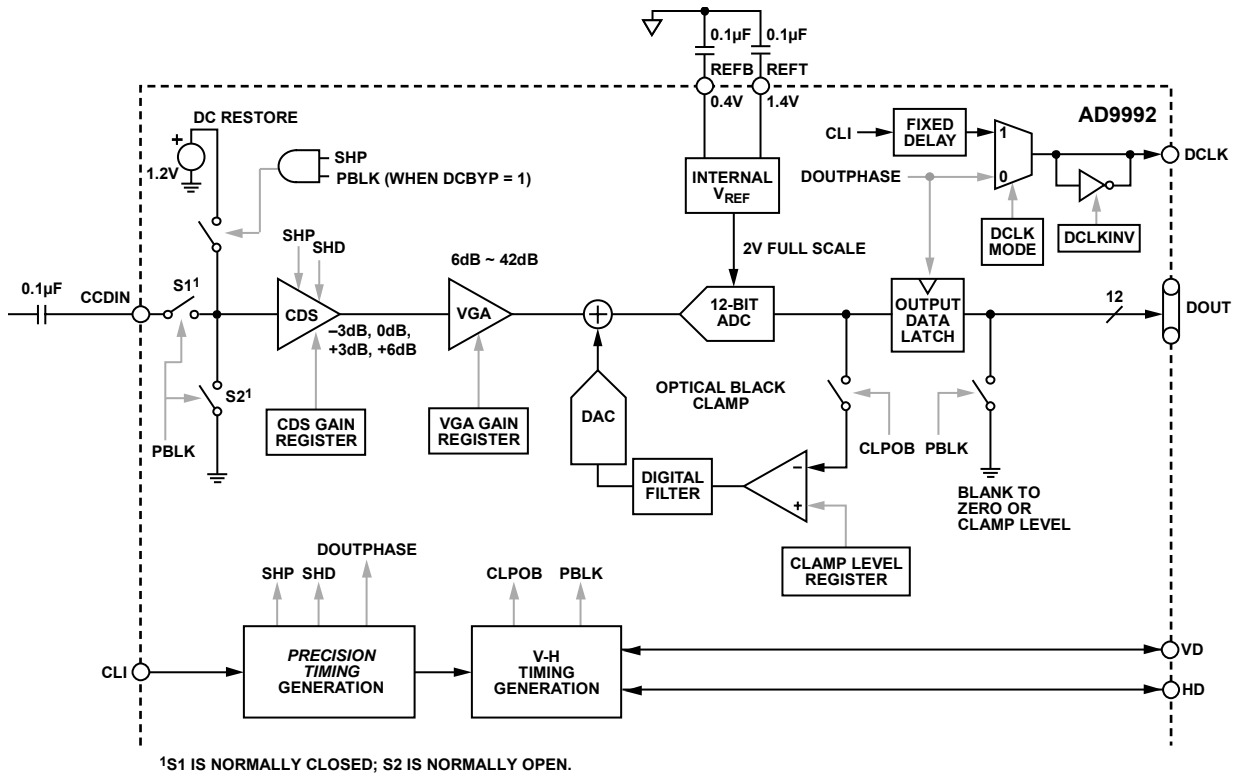


Figure 71. Analog Front-End Functional Block Diagram

The AD9992 signal processing chain is shown in Figure 71. Each processing step is essential for achieving a high quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external 0.1 μF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.2 V, making it compatible with the 1.8 V core supply voltage of the AD9992. The dc restore switch is active during the SHP sample pulse time.

The dc restore circuit can be disabled when the optional PBLK signal is used to isolate large-signal swings from the CCD input (see Analog Preblanking). Bit [6] of AFE Register Address 0x00 controls whether the dc restore is active during the PBLK interval.

Analog Preblanking

During certain CCD blanking or substrate clocking intervals, the CCD input signal to the AD9992 can increase in amplitude beyond the recommended input range. The PBLK signal can be used to isolate the CDS input from large-signal swings. While PBLK is active (low), the CDS input is internally shorted to ground.

Note that because the CDS input is shorted during PBLK, the CLPOB pulse should not be used during the same active time as the PBLK pulse.

Correlated Double Sampler (CDS)

The CDS circuit samples each CCD pixel twice to extract the video information and to reject low frequency noise. The timing shown in Figure 18 illustrates how the two internally generated CDS clocks, SHP and SHD, are used to sample the reference level and data level of the CCD signal, respectively. The placement of the SHP and SHD sampling edges is determined by the setting of the SHPLOC and SHDLOC registers located at Address 0x37. Placement of these two clock signals is critical for achieving the best performance from the CCD.

The CDS gain is variable in three steps by using the AFE Address 0x04: -3 dB, 0 dB (default), and +3 dB. Improved noise performance results from using the +3 dB setting, but the input range will be reduced (see Analog Specifications).

Variable Gain Amplifier

The VGA stage provides a gain range of approximately 6 dB to 42 dB, programmable with 10-bit resolution through the serial digital interface. A gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. When compared to 1 V full-scale systems, the equivalent gain range is 0 dB to 36 dB.

The VGA gain curve follows a linear-in-dB characteristic. The exact VGA gain is calculated for any gain register value by

$$\text{Gain (dB)} = (0.0358 \times \text{Code}) + 5.75 \text{ dB}$$

where *Code* is the range of 0 to 1023.

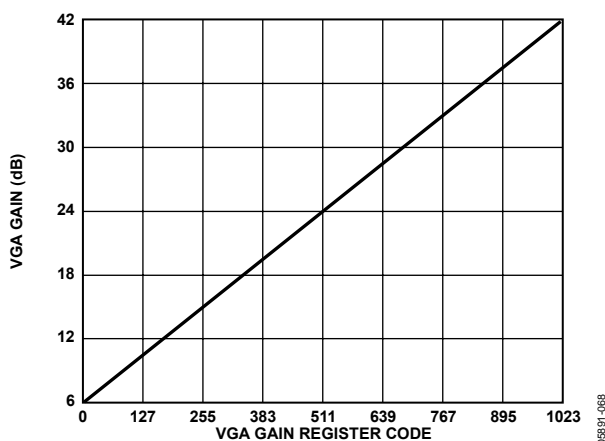


Figure 72. VGA Gain Curve

ADC

The AD9992 uses a high performance ADC architecture optimized for high speed and low power. Differential non-linearity (DNL) performance is typically better than 0.5 LSB. The ADC uses a 2 V input range. See Figure 4 and Figure 6 for typical linearity and noise performance plots for the AD9992.

Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference, selected by the user in the clamp level register. The value can be programmed between 0 LSB and 255 LSB in 1023 steps. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a DAC. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during postprocessing, the AD9992 optical

black clamping can be disabled using Bit D2 in the AFE Register Address 0x00. When the loop is disabled, the clamp level register can still be used to provide fixed offset adjustment.

Note that if the CLPOB loop is disabled, higher VGA gain settings reduce the dynamic range because the uncorrected offset in the signal path is gained up.

The CLPOB pulse should be aligned with the CCD's optical black pixels. It is recommended that the CLPOB pulse duration be at least 20 pixels wide. Shorter pulse widths can be used, but the ability for the loop to track low frequency variations in the black level will be reduced. See the Horizontal Clamping and Blanking section for timing examples.

Digital Data Outputs

The AD9992 digital output data is latched using the rising edge of the DOUTPHASE register value, as shown in Figure 71. Output data timing is shown in Figure 19 and Figure 20. It is also possible to leave the output latches transparent, so that the data outputs are valid immediately from the ADC. Programming the AFE Register Address 0x01, Bit D1, to 1 sets the output latches to transparent. The data outputs can also be disabled (three-stated) by setting the AFE Register Address 0x01, Bit D0, to 1.

The DCLK output can be used for external latching of the data outputs. By default, the DCLK output tracks the values of the DOUTPHASE registers. By changing the DCLKMODE register, the DCLK output can be held at a fixed phase, and the DOUTPHASE register values are ignored. The DCLK output can also be inverted with respect to DOUT, using the DCLKINV register bit.

The switching of the data outputs can couple noise back into the analog signal path. To minimize switching noise, it is recommended that the DOUTPHASE registers be set to the same edge as the SHP sampling location, or up to 15 edges after the SHP sampling location. Other settings can produce good results, but experimentation is necessary. It is recommended that the DOUTPHASE location not occur between the SHD sampling location and 15 edges after the SHD location. For example, if SHDLOC = 0, DOUTPHASE should be set to an edge location of 16 or greater. If adjustable phase is not required for the data outputs, the output latch can be left transparent using Address 0x01, Bit D1.

The data output coding is normally straight binary, but the coding can be changed to gray coding by setting the AFE Register Address 0x01, Bit D2, to 1.

POWER-UP SEQUENCE FOR MASTER MODE

When the AD9992 is powered up, the following sequence is recommended (refer to Figure 73 for each step). Note that a SYNC signal is required for master mode operation. If an external SYNC pulse is not available, it is possible to generate an internal SYNC event by writing to the SWSYNC register.

1. Turn on the power supplies for AD9992 and start the master clock, CLI.
2. Reset the internal AD9992 registers by writing 1 to the SW_RST register (Address 0x10).
3. By default, Vertical Outputs V1 to V24 are low. If necessary, write to the Standby3 output polarity (Address 0x26) to set different polarities for the vertical outputs in order to avoid damage to the V-driver and CCD. Write to Address 0x1C to configure each V-output as a vertical transfer clock (XV) or sensor pulse (VSG).
4. Power-up the V-driver supplies, VH and VL, anytime after Step 3 is complete to set the proper polarities.
5. Load the required registers to configure the necessary vertical timing, horizontal timing, high speed timing, and shutter timing. Set the recommended start-up Address 0xD8 to 0x888.
6. To place the part into normal power operation, write 0x04 to register 0x00. This sets the STANDBY register (AFE Register Address 0x00, Bits [1:0]) to normal operation and enables the OB clamp (AFE Register Address 0x00, Bit [2]). If the CLO output is being used to drive a crystal, also power up the CLO oscillator by writing 1 to Address 0x15.
7. By default, the internal timing core is held in a reset state, with TGCORE_RSTB register = 0. Write 1 to the TGCORE_RSTB register (Address 0x14) to start the internal timing core operation. Note if a 2× clock is used for the CLI input, the CLIDIVIDE register (0x0D) should be set to 1 before resetting the timing core.
8. Configure the AD9992 for master mode timing by writing 1 to the MASTER register (Address 0x20).
9. Write 1 to the OUTCONTROL register (Address 0x11). This allows the outputs to become active after the next SYNC rising edge. Normally OUTCONTROL takes effect after the next VD edge; however, because the part is just being powered up, there is no VD edge until the rising edge of the SYNC signal.
10. Generate a SYNC event. If SYNC is high at power-up, bring the SYNC input low for a minimum of 100 ns, and then bring SYNC high again. This causes the internal counters to reset and starts VD/HD operation. The first VD/HD edge allows VD-updated register updates to occur, including OUTCONTROL to enable all outputs. If a hardware SYNC is not available, the SWSYNC register (Address 0x13, Bit [14]) can be used to initiate a SYNC event.

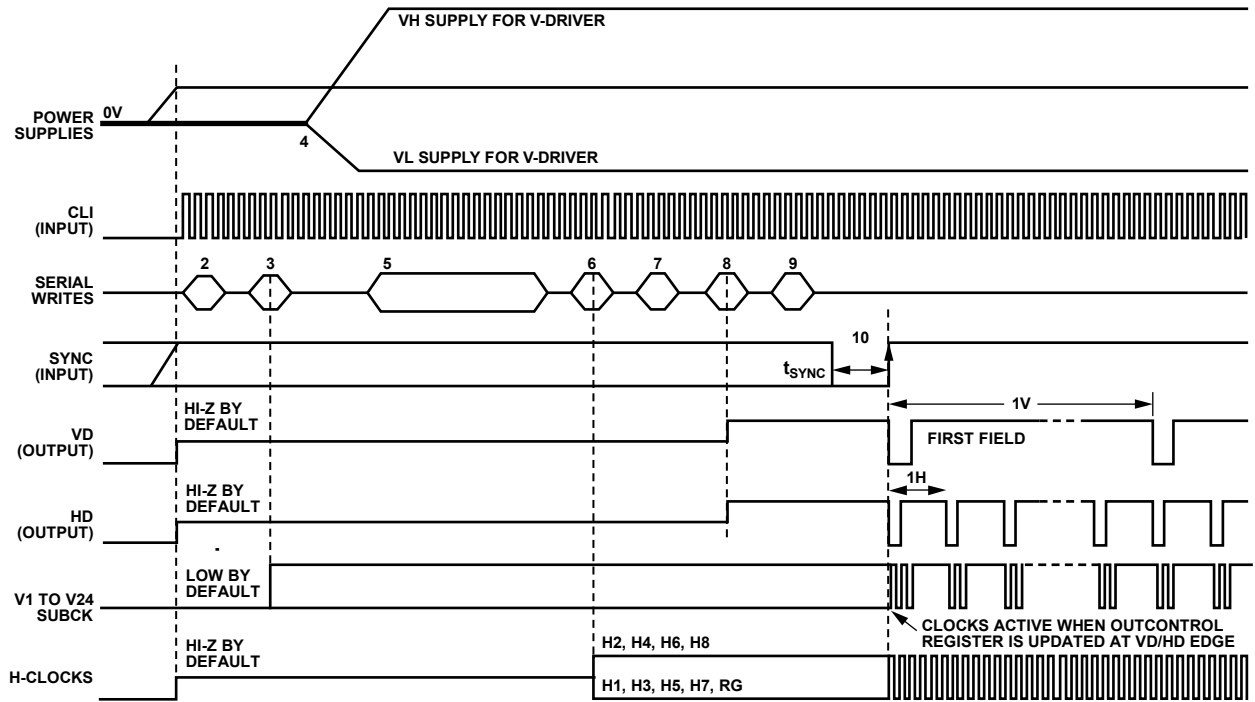


Figure 73. Recommended Power-Up Sequence and Synchronization, Master Mode

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Table 25. Power-Up Register Write Sequence

| Address | Data | Description |
|--------------|--------------|--|
| 0x10 | 0x01 | Reset all registers to default values |
| 0x26 | User-defined | Standby3 vertical output polarities |
| 0x20 to 0xFF | User-defined | Horizontal, vertical, shutter timing |
| 0xD8 | 0x888 | Configure start-up register |
| 0x00 | 0x04 | Power-up the AFE, enables OB clamp |
| 0x15 | 0x01 | Starts CLO oscillator (if using crystal) |
| 0x14 | 0x01 | Starts internal timing core |
| 0x20 | 0x01 | Configure for master mode |
| 0x11 | 0x01 | Enable all outputs after SYNC |
| 0x13 | 0x4XX1 | SWSYNC (if using software SYNC) |

Using the SWSYNC Register

If an external SYNC pulse is not available, it is possible to generate an internal SYNC in the AD9992 by writing 1 to the SWSYNC register (Address 0x13, Bit [14]). If the software SYNC option is used, the SYNC input (Pin D3) should be low (V_{SS}) during power-up. The SYNCENABLE register (Address 0x13, Bit [0]) should be set high.

SYNC During Master Mode Operation

The hardware SYNC input can be used anytime during operation to synchronize the AD9992 counters with external timing, as shown in Figure 74. The operation of the digital outputs can be suspended during the SYNC operation by setting the SYNCSPEND register (Address 0x13, Bit [2]) to 1. If SYNCSPEND = 1, the polarities of the outputs are held at the same state as OUTCONTROL = low, as shown in Table 26.

Power-Up and Synchronization in Slave Mode

The power-up procedure for slave mode operation is the same as the procedure for master mode operation with two exceptions:

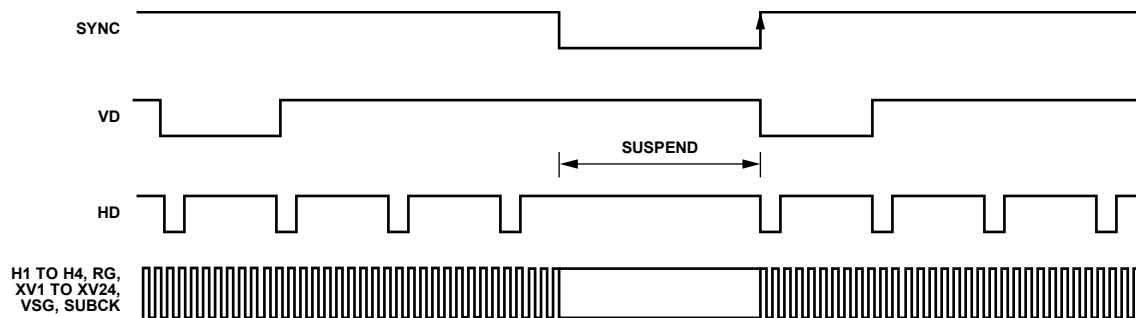
- Eliminate Step 8. Do not write the part into master mode.
- No SYNC pulse is required in slave mode. Substitute Step 10 with starting the external VD and HD signals. This synchronizes the part, allows the register updates, and starts the timing operation.

When the AD9992 is used in slave mode, the VD/HD inputs are used to synchronize the internal counters. After a falling edge of VD, there is a latency of 36 master clock CLI edges after the falling edge of HD until the internal H-counter is reset. The reset operation is shown in Figure 75.

Additional Restrictions in Slave Mode

When operating in slave mode, the following restrictions should be noted:

- The HD falling edge should be located in the same CLI clock cycle as the VD falling edge, or later than the VD falling edge. The HD falling edge should not be located within five cycles prior to the VD falling edge.
- If possible, all start-up serial writes should be performed with VD and HD disabled. This prevents unknown behavior caused by partial updating of registers before all information is loaded.

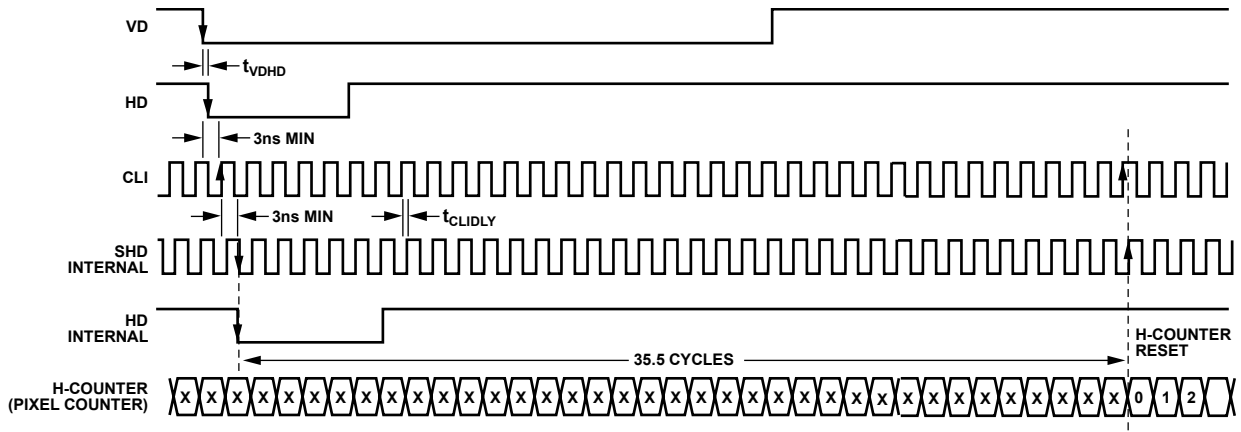


NOTES

1. THE SYNC RISING EDGE RESETS VD/HD AND COUNTERS TO 0.
2. SYNC POLARITY IS PROGRAMMABLE USING SYNCPOL REGISTER (ADDR 0x13).
3. DURING SYNC LOW, ALL INTERNAL COUNTERS ARE RESET AND VD/HD CAN BE SUSPENDED USING THE SYNCSPEND REGISTER (ADDR 0x13).
4. IF SYNCSPEND = 1, VERTICAL CLOCKS, H1 TO H4, AND RG ARE HELD AT THE SAME POLARITY SPECIFIED BY OUTCONTROL = LOW.
5. IF SYNCSPEND = 0, ALL CLOCK OUTPUTS CONTINUE TO OPERATE NORMALLY UNTIL THE SYNC RESET EDGE.

Figure 74. SYNC Timing to Synchronize the AD9992 with External Timing

06981-070



- NOTES**
- EXTERNAL HD FALLING EDGE IS LATCHED BY CLI RISING EDGE, AND THEN LATCHED AGAIN BY SHD INTERNAL FALLING EDGE.
 - INTERNAL H-COUNTER IS ALWAYS RESET 35.5 CLOCK CYCLES AFTER THE INTERNAL HD FALLING EDGE.
 - DEPENDENT ON THE VALUE OF SHDLOC, H-COUNTER RESET CAN OCCUR 36 OR 37 CLI CLOCK EDGES AFTER THE EXTERNAL HD FALLING EDGE.
 - SHDLOC = 0 IS SHOWN IN ABOVE EXAMPLE. IN THIS CASE, THE H-COUNTER RESET OCCURS 36 CLI RISING EDGES AFTER HD FALLING EDGE.
 - HD FALLING EDGE SHOULD OCCUR COINCIDENT WITH VD FALLING EDGE (WITHIN SAME CLI CYCLE) OR AFTER VD FALLING EDGE. HD FALLING EDGE SHOULD NOT OCCUR WITHIN FIVE CLI CYCLES PRIOR TO THE VD FALLING EDGE.

Figure 75. External VD/HD and Internal H-Counter Synchronization, Slave Mode

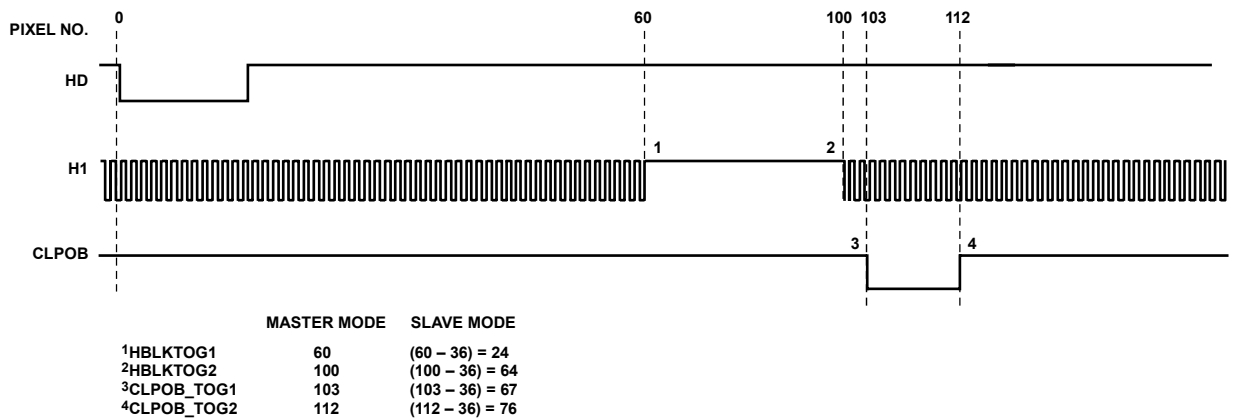


Figure 76. Example of Slave Mode Register Setting to Obtain Desired Toggle Positions

Vertical Toggle Position Placement Near Counter Reset

An additional consideration during the reset of the internal counters is the vertical toggle position placement. Prior to the internal counters being reset, there is a region of 36 pixels during which no toggle positions should be programmed.

As shown in Figure 77, for master mode the last 36 pixels before the HD falling edge must not be used for toggle position placement of the V, VSG, SUBCK, HBLK, PBLK, or CLPOB pulses.

Figure 78 shows the same example for slave mode. The same restriction applies: the last 36 pixels before the counters are reset cannot be used. However, in slave mode, the counter reset is delayed with respect to VD/HD placement, so the inhibited area is different than it is in master mode.

It is recommended that Pixel Location 0 not be used for any of the toggle positions for the VSG and SUBCK pulses.

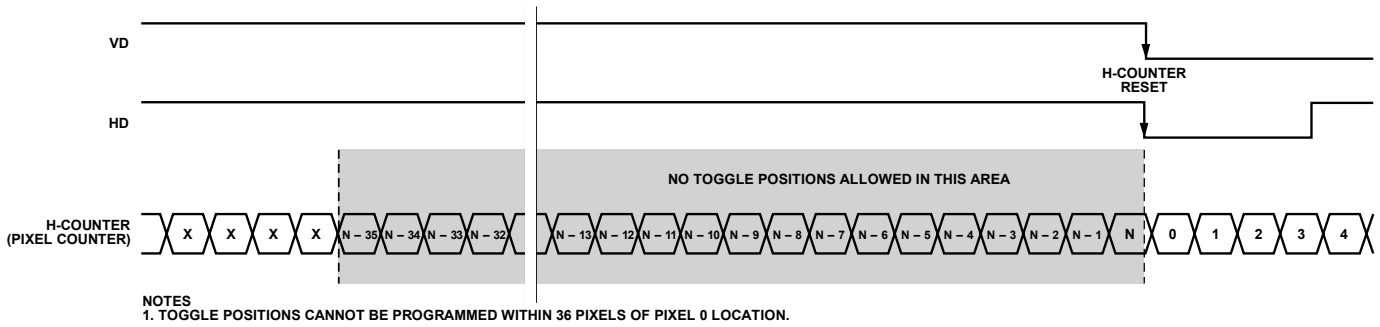


Figure 77. Toggle Position Inhibited Area—Master Mode

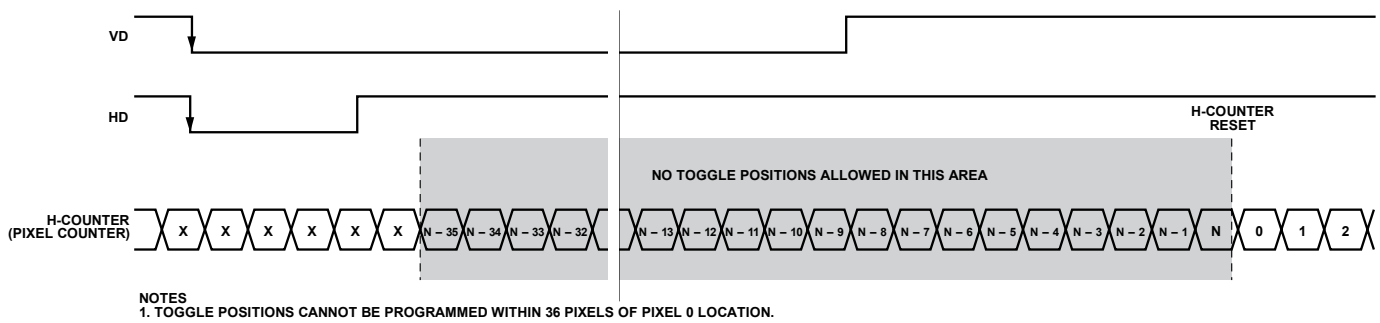


Figure 78. Toggle Position Inhibited Area—Slave Mode

STANDBY MODE OPERATION

The AD9992 contains three standby modes to optimize the overall power dissipation in a particular application. Bits [1:0] of Address 0x00 control the power-down state of the device:

- STANDBY [1:0] = 0 = normal operation (full power)
- STANDBY [1:0] = 1 = Standby1 mode
- STANDBY [1:0] = 2 = Standby2 mode
- STANDBY [1:0] = 3 = Standby3 mode (lowest power)

Table 26 summarizes the operation of each power-down mode. The OUTCONTROL register takes priority over the Standby1 and Standby2 modes in determining the digital output states, but Standby3 mode takes priority over OUTCONTROL. Standby3 has the lowest power consumption and even shuts down the crystal oscillator circuit between CLI and CLO. Therefore, if CLI and CLO are being used with a crystal to generate the master clock, this circuit is powered down and there is no clock signal. When returning from Standby3 mode to normal operation, the timing core must be reset at least 500 μ s after the STANDBY register is written to. This allows sufficient time for the crystal circuit to settle.

The vertical outputs can also be programmed to hold a specific value during the Standby3 mode by using Address 0x26. This register is useful during power-up if different polarities are required by the V-driver and CCD to prevent damage when VH and VL areas are applied. The polarities for Standby1 mode and Standby2 mode are also programmable, using Address 0x25. OUTCONTROL = low also uses the same polarities programmed for Standby1 and Standby2 modes in Address 0x25. The GPO polarities are programmable using Address 0x27.

Note that the GPO outputs are High-Z by default at power-up until Address 0x78 is used to select them as outputs.

CLI FREQUENCY CHANGE

If the input clock CLI is interrupted or changed to a different frequency, the timing core must be reset for proper operation. After the CLI clock has settled to the new frequency, or the previous frequency is resumed, write 0 and then 1 to the TGCORE_RSTB register (Address 0x14). This guarantees that the timing core operates properly.

Table 26. Standby Mode Operation (Standby Polarities for XV, XSUBCK, GPO Outputs are Programmable)

| I/O Block | Standby3 (Default) ^{1, 2} | OUTCONTROL = Low ² | Standby2 ^{3, 4} | Standby1 ^{3, 4} |
|----------------|------------------------------------|-----------------------------------|-----------------------------------|--------------------------|
| AFE | Off | No change | Off | Only REFT, REFB on |
| Timing Core | Off | No change | Off | On |
| CLO Oscillator | Off | No change | Off | On |
| CLO | Low | No change | Low | Running |
| H1 | High-Z | Low | Low (4.3 mA) | Low (4.3 mA) |
| H2 | High-Z | High | High (4.3 mA) | High (4.3 mA) |
| H3 | High-Z | Low | Low (4.3 mA) | Low (4.3 mA) |
| H4 | High-Z | High | High (4.3 mA) | High (4.3 mA) |
| H5 | High-Z | Low | Low (4.3 mA) | Low (4.3 mA) |
| H6 | High-Z | High | High (4.3 mA) | High (4.3 mA) |
| H7 | High-Z | Low | Low (4.3 mA) | Low (4.3 mA) |
| H8 | High-Z | High | High (4.3 mA) | High (4.3 mA) |
| HL | High-Z | Low | Low (4.3 mA) | Low (4.3 mA) |
| RG | High-Z | Low | Low (4.3 mA) | Low (4.3 mA) |
| VD | Low | $\overline{\text{VDHDPOL}}$ value | $\overline{\text{VDHDPOL}}$ value | Running |
| HD | Low | $\overline{\text{VDHDPOL}}$ value | $\overline{\text{VDHDPOL}}$ value | Running |
| DCLK | Low | Running | Low | Running |
| DOUT | Low | Low | Low | Low |
| XV1 to XV24 | Low | Low | Low | Low |
| XSUBCK | Low | Low | Low | Low |
| GPO1 to GPO8 | Low | Low | Low | Low |

¹ To exit Standby3, write 00 to STANDBY (Address 0x00, Bits [1:0]), and then reset the timing core after 500 μ s to guarantee proper settling of the oscillator and external crystal.

² Standby3 mode takes priority over OUTCONTROL for determining the output polarities.

³ These polarities assume OUTCONTROL = high because OUTCONTROL = low takes priority over Standby1 and Standby2.

⁴ Standby1 and Standby2 set H and RG drive strength to minimum value (4.3 mA).

CIRCUIT LAYOUT INFORMATION

The PCB layout is critical in achieving good image quality from the AD9992. All of the supply pins, particularly the AVDD, TCVD, RGVDD, and HVDD supplies, must be decoupled to ground with good quality high frequency chip capacitors. The decoupling capacitors should be located as close as possible to the supply pins and should have a very low impedance path to a continuous ground plane. If possible, there should be a 4.7 μF or larger value bypass capacitor for each main supply—AVDD, HVDD, and DRVDD—although this is not necessary for each individual pin. In most applications, the supply for RGVDD and HVDD is shared, which can be done as long as the individual supply pins are separately bypassed with 0.1 μF capacitors. A separate 3 V supply can also be used for DRVDD, but this supply pin should still be decoupled to the same ground plane as the rest of the chip. A separate ground for DRVSS is not recommended.

The analog bypass pins (REFT and REFB) should be carefully decoupled to ground as close as possible to their respective pins. The analog input (CCDIN) capacitor should be located close to the pin.

The H1 to H8, HL, and RG traces should be designed to have low inductance to minimize distortion of the signals. The complementary signals, H1/H3/H5/H7 and H2/H4/H6/H8, should be routed as close together and as symmetrically as possible to minimize mutual inductance. Heavier PCB traces are recommended because of the large transient current demand on H1 to H8 by the CCD. If possible, physically locating the AD9992 closer to the CCD reduces the inductance on these lines. As always, the routing path should be as direct as possible from the AD9992 to the CCD.

Note that it is recommended that all H1 to H8 outputs on the AD9992 be used together for maximum flexibility in drive strength settings. A typical CCD with H1 and H2 inputs only should have the AD9992's H1, H3, H5, and H7 outputs connected together to drive the CCD's H1, and H2, H4, H6, and H8 outputs connected together to drive the CCD's H2. Similarly, a CCD with H1, H2, H3, and H4 inputs should have the following:

- H1 and H3 connected to the CCD's H1.
- H2 and H4 connected to the CCD's H2.
- H5 and H7 connected to the CCD's H3.
- H6 and H8 connected to the CCD's H4.

Typical 3 V System

The AD9992 typical circuit connections for a 3 V system are shown in Figure 79. This application uses an external 3.3 V supply, which is connected to the AD9992's LDO input. The LDO is configured to output 1.8 V for the AD9992's core supply by connecting the LDO1P8EN pin to 3.3 V and the LDO3P2EN pin to ground. The LDOOUT and SENSE pins are shorted together and used to supply 1.8 V to the AVDD, TCVD, and DVDD pins.

Typical 1.8 V System

The internal LDO can be disabled by tying the LDO pins to ground (LDOIN, LDO1P8EN, LDO3P2EN, LDOOUT, and SENSE). In this case, an external 1.8 V regulator is required to supply 1.8 V to the AVDD, TCVD, and DVDD pins.

All of the AD9992's remaining supplies can be directly supplied with 1.8 V. The internal charge pump (CP) can be used to generate 3.3 V for the H and RG supplies.

The AD9992 typical circuit connections for a 1.8 V system are shown in Figure 80.

External Crystal Application

The AD9992 contains an on-chip oscillator for driving an external crystal. Figure 81 shows an example application using a typical 27 MHz crystal. For the exact values of the external resistors and capacitors, it is best to consult the crystal manufacturer's data sheet.

Note that a 2 \times crystal is not recommended for use with the CLO oscillator circuit. The crystal frequency should not exceed 40 MHz.

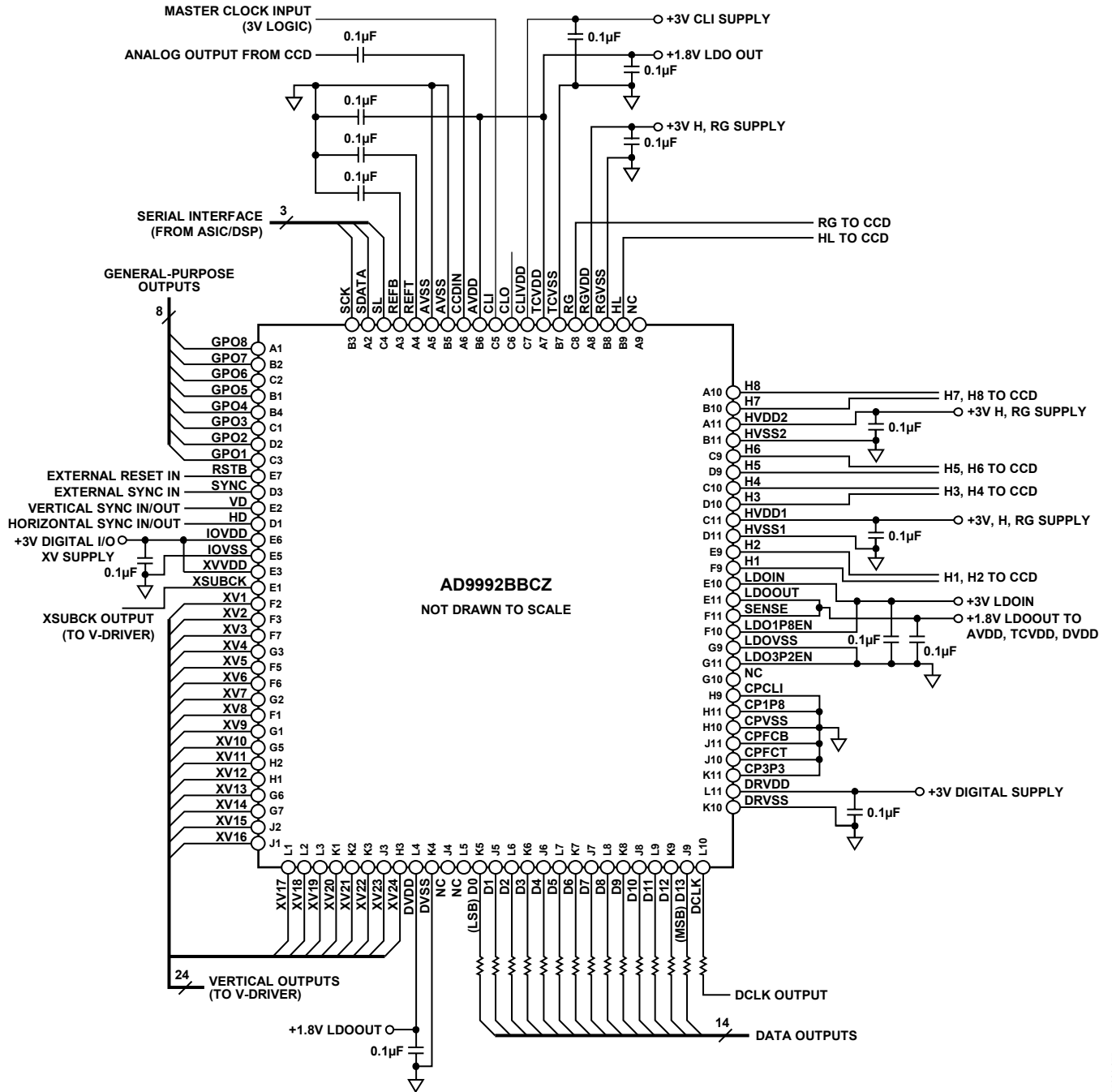


Figure 79. Typical 3 V Circuit Configuration

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AD9992

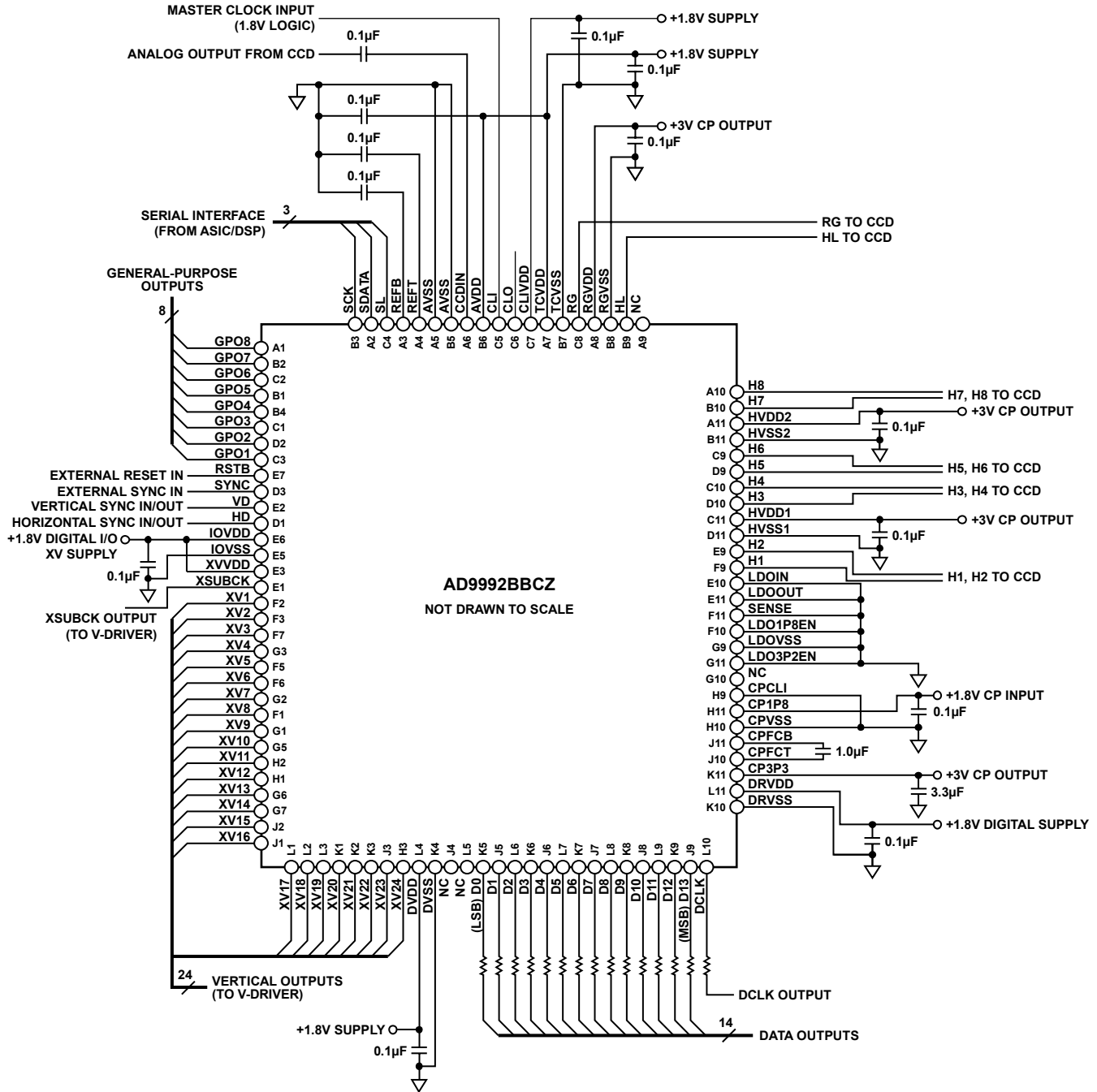


Figure 80. Typical 1.8 V Circuit Configuration Using Charge Pump for HVDD and RGVD

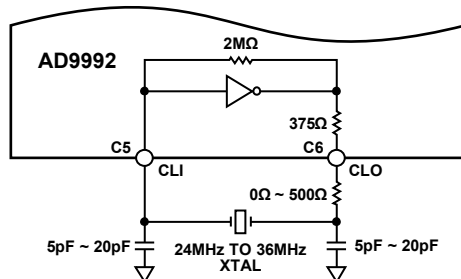
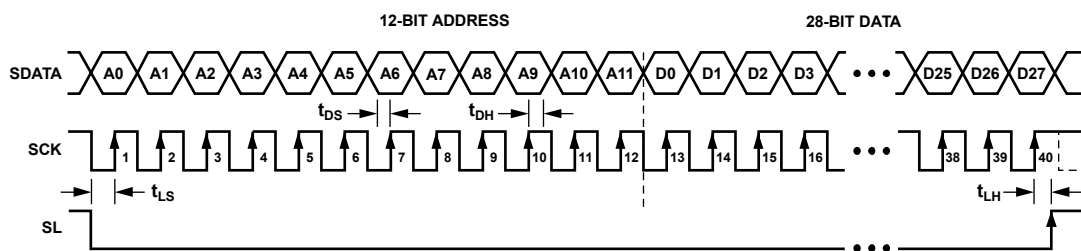


Figure 81. Crystal Application Using CLI/CLO (Consult Crystal Data Sheet for Component Values)

SERIAL INTERFACE TIMING

The internal registers of the AD9992 are accessed through a 3-wire serial interface. Each register consists of a 12-bit address and a 28-bit data-word. Both the 12-bit address and 28-bit data-word are written starting with the LSB. To write to each register, a 40-bit operation is required, as shown in Figure 82. Although many registers are fewer than 28 bits wide, all 28 bits must be written for each register. For example, if the register is only 20 bits wide, the upper eight bits are don't cares and must be filled with 0s during the serial write operation. If fewer than 28 data bits are written, the register is not updated with new data.

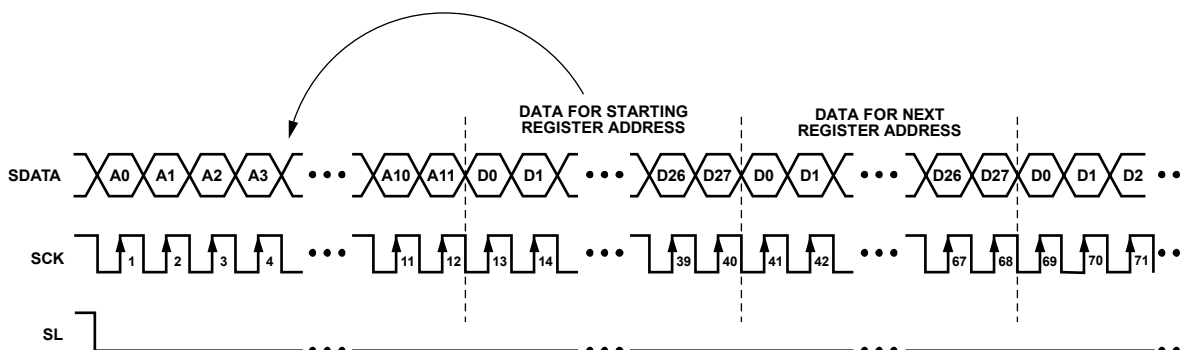
Figure 83 shows a more efficient way to write to the registers, using the AD9992's address autoincrement capability. Using this method, the lowest desired address is written first, followed by multiple 28-bit data-words. Each new 28-bit data-word is automatically written to the next highest register address. By eliminating the need to write each 12-bit address, faster register loading is achieved. Continuous write operations can be used starting with any register location.



NOTES

- SDATA BITS ARE LATCHED ON SCK RISING EDGES. SCK CAN IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
- ALL 40 BITS MUST BE WRITTEN: 12 BITS FOR ADDRESS AND 28 BITS FOR DATA.
- IF THE REGISTER LENGTH IS <28 BITS, 0s MUST BE USED TO COMPLETE THE 28-BIT DATA LENGTH.
- NEW DATA VALUES ARE UPDATED IN THE SPECIFIED REGISTER LOCATION AT DIFFERENT TIMES, DEPENDING ON THE PARTICULAR REGISTER WRITTEN TO. SEE THE UPDATING OF NEW REGISTER VALUES SECTION FOR MORE INFORMATION.

Figure 82. Serial Write Operation



NOTES

- MULTIPLE SEQUENTIAL REGISTERS MAY BE LOADED CONTINUOUSLY.
- THE FIRST (LOWEST) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 28-BIT DATA-WORDS.
- THE ADDRESS AUTOMATICALLY INCREMENTS WITH EACH 28-BIT DATA-WORD (ALL 28 BITS MUST BE WRITTEN).
- SL IS HELD LOW UNTIL THE LAST DESIRED REGISTER HAS BEEN LOADED.

Figure 83. Continuous Serial Write Operation

LAYOUT OF INTERNAL REGISTERS

The AD9992 address space is divided into two register areas, as illustrated in Figure 84. In the first address space, Address 0x00 to Address 0xFF contain the registers for the AFE, miscellaneous, VD/HD, I/O and CP, timing core, shutter and GPO, and update control functions. The second address space, beginning at Address 0x800, consists of the V-pattern groups, V-sequences, and field registers. This is a configurable set of registers; the user can decide how many V-pattern groups, V-sequences, and fields are used in a particular design. Therefore, the addresses for these registers vary, depending on the number of V-patterns and V-sequences chosen.

Address 0x28 specifies the total number of V-pattern groups and V-sequences used. The starting address for the V-pattern groups is always 0x800. The starting address for the V-sequences is based on the number of V-pattern groups used, with each V-pattern group occupying 48 register addresses. The starting address for the field registers depends on both the number of V-pattern groups and the number of V-sequences. Each V-sequence occupies 40 register addresses, and each field occupies 16 register addresses.

The starting address for the V-sequences is equal to 0x800 plus the number of V-pattern groups times 48. The starting address for the fields is equal to the starting address of the V-sequences plus the number of V-sequences times 40. The V-pattern, V-sequence, and field registers must always occupy a continuous block of addresses.

Figure 85 shows an example in which three V-pattern groups, four V-sequences, and two fields are used. The starting address for the V-pattern groups is always 0x800. Since $VPATNUM = 3$, the V-pattern groups occupies 144 address locations. The start of the V-sequence registers is 0x890 (that is, $0x800 + 144$). With $VSEQNUM = 4$, the V-sequences occupy 160 address locations. Therefore, the field registers begin at 0x930 (that is, $0x890 + 160$).

The AD9992 address space contains many unused addresses. Undefined addresses between Address 0x00 and Address 0xFF should not be written to; otherwise, the AD9992 may operate incorrectly. Continuous register writes should be performed carefully so that undefined registers are not written to.

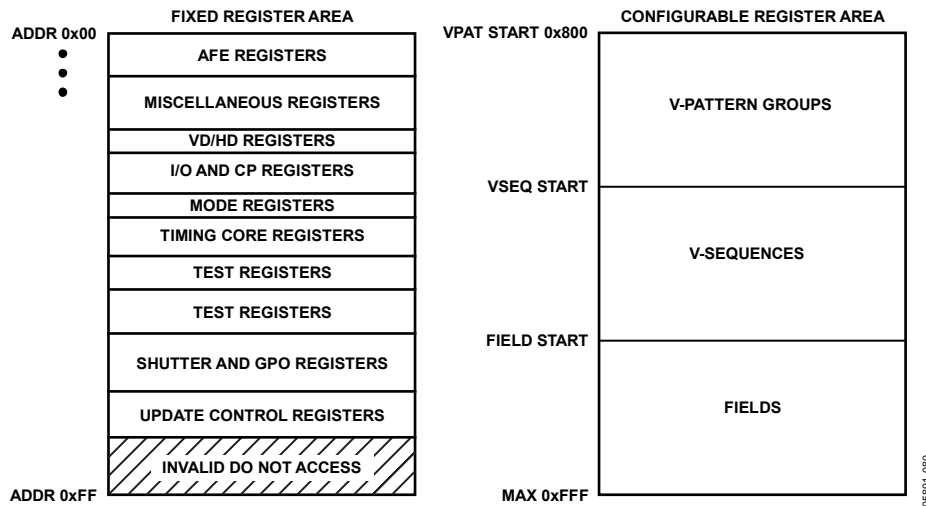


Figure 84. Layout of AD9992 Registers

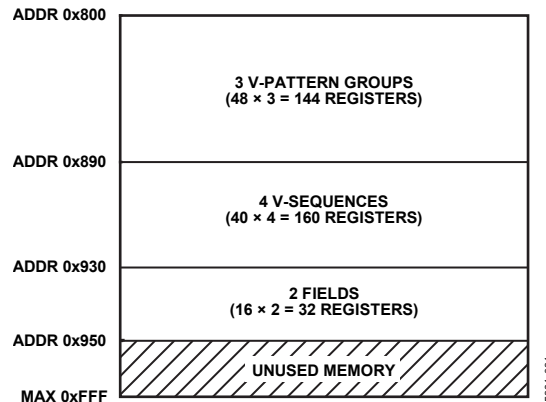


Figure 85. Example Register Configuration

UPDATING NEW REGISTER VALUES

The AD9992's internal registers are updated at different times, depending on the particular register. Table 27 summarizes the four register update types: SCK, VD, SG-Line, and SCP. Tables in the Complete Register Listing section also contain an Update Type column that identifies when each register is updated.

- **SCK Updated**—As soon as the 28th data bit (D27) is clocked in, some registers are immediately updated. These registers are used for functions that do not require gating with the next VD boundary, such as power-up and reset functions.
- **VD Updated**—More registers are updated at the next VD falling edge. By updating these values at the next VD edge, the current field is not corrupted and the new register values are applied to the next field. The VD update can be further delayed past the VD falling edge by using the UPDATE register (Address 0x17). This delays the VD-updated register updates to any HD line in the field. Note that the field registers are not affected by the UPDATE register.
- **SG-Line Updated**—A few of the shutter registers are updated at the HD falling edge at the start of the SG active line. These registers control the SUBCK signal so that the SUBCK output is not updated until the SG line occurs.

- **SCP Updated**—At the next SCP where they are used, the V-pattern group and V-sequence registers are updated. For example, in Figure 86 this field has selected Region 1 to use VSEQ3 for the vertical outputs. This means that a write to any of the VSEQ3 registers, or any of the V-pattern group registers, which are referenced by VSEQ3, updates at SCP1. If multiple writes are done to the same register, the last one done before SCP1 is the one that is updated. Likewise, register writes to any VSEQ5 registers are updated at SCP2, and register writes to any VSEQ8 registers are updated at SCP3.

Caution

It is recommended that the registers in the configurable address area not be written within 36 pixels of any HD falling edge where a sequence change position (SCP) occurs. See Figure 77 and Figure 78 for an example of what this inhibit area looks like in master and slave modes. This restriction applies to the V-pattern, V-sequence, and field registers. As shown in Figure 86, writing to these registers before the VD falling edge typically avoids loading these registers during SCP locations.

Table 27. Register Update Locations

| Update Type | Description |
|-------------|--|
| SCK | When the 28th data bit (D27) is clocked in, the register is immediately updated. |
| VD | Register is updated at the VD falling edge. VD-updated registers can be delayed further by using the UPDATE register at Address 0x17. FIELD registers are not affected by the UPDATE register. |
| SG-Line | Register is updated at the HD falling edge at the start of the SG-active line. |
| SCP | Register is updated at the next SCP when the register is used. |

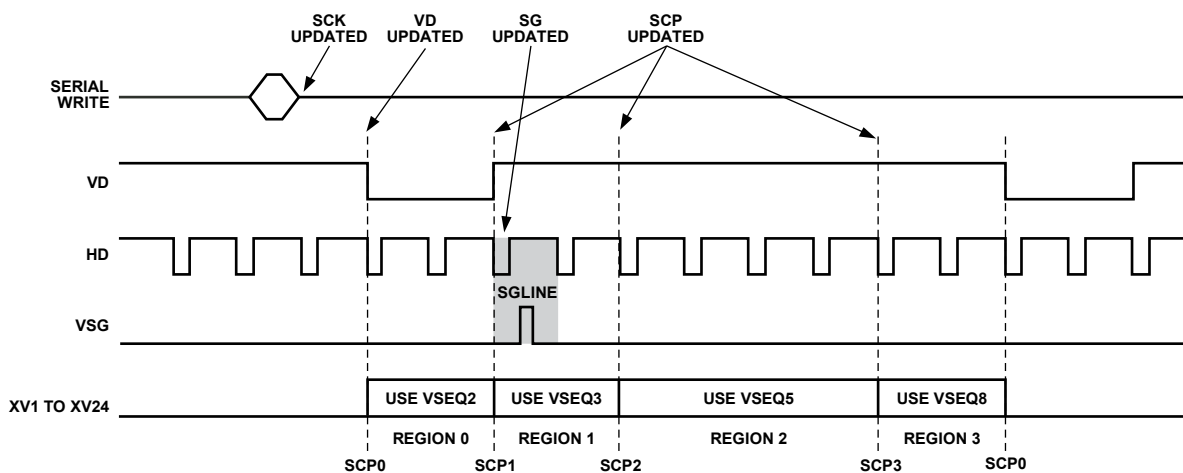


Figure 86. Register Update Locations (See Table 27 for Definitions)

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COMPLETE REGISTER LISTING

When an address contains less than 28 data bits, all remaining bits must be written as 0s.

Table 28. AFE Registers

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|-------------|--|
| 00 | [1:0] | 3 | SCK | STANDBY | Standby modes. 0: normal operation; 1: Standby1 mode; 2: Standby2 mode; 3: Standby3 mode. |
| | [2] | 1 | | CLPENABLE | 0: disable OB clamp; 1: enable OB clamp. |
| | [3] | 0 | | CLPSPEED | 0: select normal OB clamp settling; 1: select fast OB clamp settling. |
| | [4] | 0 | | FASTUPDATE | 0: ignore CDS gain; 1: very fast clamping when CDS gain is updated. |
| | [5] | 0 | | PBLK_LVL | 0: blank data outputs to 0 during PBLK; 1: blank data outputs to programmed clamp level during PBLK. |
| | [6] | 0 | | DCBYP | 0: enable input dc restore circuit during PBLK; 1: disable input dc restore circuit during PBLK. |
| 01 | [0] | 0 | SCK | DOUTDISABLE | 0: data outputs are driven; 1: data outputs are three-stated. |
| | [1] | 0 | | DOUTLATCH | 0: latch data outputs using the rising edge of DOUTPHASEP (DOUTPHASEP register setting); 1: output latch is transparent. |
| | [2] | 0 | | GRAY_EN | 1: enable gray encoding of the digital data outputs. |
| | [3] | 1 | | TEST | Set to 0. |
| 02 | [0] | 0 | SCK | TEST | Do not access, or set to 0. |
| 03 | [23:0] | FFFFFF | SCK | TEST | Do not access, or set to 0xFFFFFF. |
| 04 | [2:0] | 0 | VD | CDSGAIN | CDS gain setting. 0: -3 dB; 4: 0 dB; 6: +3 dB; 7: +6 dB. All other values are invalid. |
| 05 | [9:0] | F | VD | VGAGAIN | VGA gain, 6 dB to 42 dB (0.035 dB per step). |
| 06 | [9:0] | 1EC | VD | CLAMPLEVEL | Optical black clamp level, 0 to 1023 LSB (1 LSB per step). |
| 0D | [0] | 0 | VD | CLIDIVIDE | 0: no division of CLI; 1: divide CLI input frequency by 2. |

Table 29. Miscellaneous Registers

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|---------------|--|
| 10 | [0] | 0 | SCK | SW_RST | Software reset. Bit self-clears to 0 when a reset occurs. 1: reset Address 0x00 to Address 0xFF to default values. |
| 11 | [0] | 0 | VD | OUTCONTROL | 0: make all outputs dc inactive; 1: enable outputs at next VD edge. |
| 12 | [0] | 0 | SCK | RSTB_EN | 1: configure SYNC pin as RSTB input signal. |
| | [4:1] | 0 | | TEST | Test mode only. Must be set to 0. |
| 13 | [0] | 1 | SCK | SYNCENABLE | 1: external synchronization enable (configures Pin D3 as an input). |
| | [1] | 0 | | SYNCPOL | SYNC active polarity. |
| | [2] | 0 | | SYNCSUSPEND | Suspend clocks during SYNC active pulse. 0: don't suspend; 1: suspend. |
| | [3] | 0 | | ENH_SYNC_EN | 1: enable enhanced sync/shutter operations. |
| | [4] | 0 | | SYNC_MASK_HD | 1: mask HD during SYNCSUSPEND. |
| | [5] | 1 | | SYNC_MASK_VD | 1: mask VD during SYNCSUSPEND. |
| | [6] | 1 | | SYNC_MASK_V | 1: mask XV outputs during SYNCSUSPEND. |
| | [7] | 0 | | SHADOW_EN | 1: enable use of shadow registers. |
| | [12:8] | 0 | | TEST | Test mode only. Must be set to 0. |
| | [13] | 0 | | UPDATE_SHADOW | 1: writes to shadow bits affect shadow registers, not primary. |
| 14 | [14] | 0 | SCK | SWSYNC | 1: initiate software SYNC event (self-clears to 0 after SYNC). |
| | [0] | 0 | | TGCORE_RSTB | Timing core reset bar. 0: reset TG core; 1: resume operation. |

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|-----------------|--|
| 15 | [0] | 0 | SCK | OSC_RSTB | CLO oscillator reset bar. 0: oscillator in power-down state; 1: resume oscillator operation. |
| 16 | [27:0] | 0 | SCK | TEST | Test mode only. Must be set to 0. |
| 17 | [12:0] | 0 | SCK | UPDATE | Serial update line. Sets the line (HD) within the field to update the VD-updated registers. |
| | [13] | 0 | | PREVENTUP | Prevents the update of the VD-updated registers. 0: normal update; 1: prevent update of VD-updated registers. |
| | [14] | 0 | | SYNC_RST_SHUTEN | 1: enable reset of the shutter control after SYNC operation occurs. |
| | [15] | 0 | | REG_RST_SHUT | 1: forces shutter control to reset. |
| | [16] | 0 | | GPO_RST_SYNC | 1: reset shutter and GPO control at SYNC operation. |
| 18 | [27:0] | 0 | SCK | TEST | Test mode only. Must be set to 0. |
| 19 | [27:0] | 0 | SCK | TEST | Test mode only. Must be set to 0. |
| 1A | [27:0] | 0 | SCK | TEST | Test mode only. Must be set to 0. |
| 1B | [27:0] | A | SCK | TEST | Test mode only. Must be set to 0xA. |
| 1C | [23:0] | FF0000 | SCK | VSGSELECT | Each bit selects XV pulses for use as VSG pulses. |
| 1D | [23:0] | 0 | SCK | VSGMASK_CTL | VSG masking. Overrides settings in field registers when enabled. |
| | [24] | 0 | | VSGMASK_CTL_EN | 0: disable VSGMAK_CTL bits. VSG masking is controlled by field registers. 1: enable VSGMASK_CTL bits to control VSG masking |
| 1F | [0] | 1 | SCK | HCNT14_EN | 1: enable 14-bit H-counter. |
| | [1] | 1 | | PBLK_MASK_EN | 1: disable clamp operation if PBLK is active at the same time as CLPOB. |

Table 30. VD/HD Registers

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|---------|--|
| 20 | [0] | 0 | SCK | MASTER | VD/HD master or slave mode. 0: slave mode; 1: master mode. |
| 21 | [0] | 0 | VD | VDHDPOL | VD/HD active polarity. 0 = low, 1 = high. |
| 22 | [12:0] | 0 | VD | HDRISE | Rising edge location for HD. Minimum value is 36 pixels. |
| | [25:13] | 0 | | VDRISE | Rising edge location for VD. |

Table 31. I/O and Charge Pump Registers

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|-----------|---|
| 23 | [0] | 0 | SCK | OSC_NVR | Oscillator normal voltage range. Set to match CLIVDD supply voltage. 0 = 1.8 V, 1 = 3.3 V |
| | [1] | 0 | | XV_NVR | XV output normal voltage range. Set to match XVVDD supply voltage. 0 = 1.8 V, 1 = 3.3 V |
| | [2] | 0 | | IO_NVR | I/O normal voltage range. Set the match IOVDD supply voltage. 0 = 1.8 V, 1 = 3.3 V |
| | [3] | 0 | | DATA_NVR | Data pin normal voltage range. Set to match DRVDD supply voltage. 0 = 1.8 V I/O, 1 = 3.3 V I/O. |
| | [4] | 0 | | TEST | Test use only. Set to 0. |
| | [5] | 0 | | TEST | Test use only. Set to 0. |
| | [6] | 0 | | LDO_32_EN | 1: internal regulator enable for 3.2 V output. |
| | [9:7] | 1 | | HCLKMODE | Selects HCLK output configuration. Should be written to desired value. 001 = Mode 1, 010 = Mode 2, 100 = Mode 3. All other values are invalid. |

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| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|------------|--|
| 24 | [0] | 0 | SCK | SEL_VCO | 1: internal CP clock select VCO. |
| | [1] | 1 | | SEL_DIV | 1: internal CP clock select divided-down version of CLI (default). |
| | [2] | 0 | | SEL_CLI | 1: internal CP clock select CLI. |
| | [3] | 0 | | O31V | 1: CP output voltage is 3.1 V. |
| | [4] | 0 | | O32V | 1: CP output voltage is 3.2 V. |
| | [5] | 1 | | O33V | 1: CP output voltage is 3.3 V. |
| | [6] | 0 | | O34V | 1: CP output voltage is 3.4 V. |
| | [7] | 1 | | TEST | Test use only. Use default values only. |
| | [8] | 1 | | TEST | Test use only. Use default values only. |
| | [9] | 1 | | TEST | Test use only. Use default values only. |
| | [10] | 1 | | TEST | Test use only. Use default values only. |
| | [11] | 0 | | TEST | Test use only. Use default values only. |
| | [12] | 0 | | TEST | Test use only. Use default values only. |
| | [13] | 0 | | TEST | Test use only. Use default values only. |
| | [14] | 1 | | CP_PDN | Charge pump power-down. 1: power-down; 0: CP is running. |
| 25 | [24:0] | 0 | SCK | VT_STBY12 | [23:0] Standby1 and Standby2 polarity for XV[23:0]. [24] Standby1 and Standby2 polarity for XSUBCK. Settings also apply when OUTCONTROL = low. |
| 26 | [24:0] | 0 | SCK | VT_STBY3 | [23:0] Standby3 polarity for XV [23:0]. [24] Standby3 polarity for XSUBCK. |
| 27 | [7:0] | 0 | SCK | GP_STDBY12 | Standby1 and Standby2 polarity for GPO [7:0]. Settings also apply when OUTCONTROL = low. |
| | [15:8] | | | GP_STDBY3 | |

Table 32. Memory Configuration and MODE Registers

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|---------|-----------------------------------|
| 28 | [4:0] | 0 | SCK | VPATNUM | Total number of V-pattern groups. |
| | [9:5] | 0 | | SEQNUM | Total number of V-sequences. |
| 2A | [2:0] | 0 | SCK | MODE | Total number of fields in MODE. |
| 2B | [4:0] | 0 | SCK | FIELD0 | Selected first field in MODE. |
| | [9:5] | 0 | | FIELD1 | Selected second field in MODE. |
| | [14:10] | 0 | | FIELD2 | Selected third field in MODE. |
| | [19:15] | 0 | | FIELD3 | Selected fourth field in MODE. |
| | [24:20] | 0 | | FIELD4 | Selected fifth field in MODE. |
| 2C | [4:0] | 0 | SCK | FIELD5 | Selected sixth field in MODE. |
| | [9:5] | 0 | | FIELD6 | Selected seventh field in MODE. |

Table 33. Timing Core Registers

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|----------|--|
| 30 | [5:0] | 0 | SCK | H1POSLOC | H1 rising edge location. |
| | [13:8] | 20 | | H1NEGLOC | H1 falling edge location. |
| | [16] | 1 | | H1POL | H1 polarity control. 0: inverse of Figure 18; 1: no inversion. |
| 31 | [5:0] | 0 | SCK | H2POSLOC | H2 rising edge location (H5 in HCLK Mode 3). |
| | [13:8] | 20 | | H2NEGLOC | H2 falling edge location (H5 in HCLK Mode 3). |
| | [16] | 1 | | H2POL | H2 polarity (H5 in HCLK Mode 3). 0: inverse of Figure 18; 1: no inversion. |
| 32 | [5:0] | 0 | SCK | HLPOSLOC | HL rising edge location. |
| | [13:8] | 20 | | HLNEGLOC | HL falling edge location. |
| | [16] | 1 | | HLPOL | HL polarity control. 0: inverse of Figure 18; 1: no inversion. |

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|--------------|--|
| 33 | [5:0] | 0 | SCK | RGPOSLOC | RG rising edge location. |
| | [13:8] | 10 | | RGNEGLOC | RG falling edge location. |
| | [16] | 1 | | RGH2POL | RG polarity control. 0: inverse of Figure 18, 1: no inversion. |
| 34 | [0] | 0 | SCK | H1HBLKRETIME | Retime H1, H2, HL HBLK to the internal clock. 0: no retime; 1: retime. |
| | [1] | 0 | | H2HBLKRETIME | Recommended setting is retime enabled (1). Setting to 1 adds one cycle delay to programmed HBLK positions. |
| | [2] | 0 | | HLHBLKRETIME | |
| | [3] | 0 | | HL_HBLK_EN | Enable HBLK for HL output. 0: disable; 1: enable. |
| | [7:4] | 4 | | HCLK_WIDTH | Enables wide H-clocks during HBLK interval. Set to 0 to disable. |
| 35 | [2:0] | 1 | SCK | H1DRV | H1 drive strength. 0: off; 1: 4.3 mA; 2: 8.6 mA; 3: 12.9 mA; 4: 4.3 mA; 5: 8.6 mA; 6: 12.9 mA; 7: 17.2 mA. |
| | [6:4] | 1 | | H2DRV | H2 drive strength (same range as H1DRV). |
| | [10:8] | 1 | | H3DRV | H3 drive strength (same range as H1DRV). |
| | [14:12] | 1 | | H4DRV | H4 drive strength (same range as H1DRV). |
| | [18:16] | 1 | | HLDRV | HL drive strength (same range as H1DRV). |
| | [22:20] | 1 | | RGDRV | RG drive strength (same range as H1DRV). |
| 36 | [2:0] | 1 | SCK | H5DRV | H5 drive strength (same range as H1DRV). |
| | [6:4] | 1 | | H6DRV | H6 drive strength (same range as H1DRV). |
| | [10:8] | 1 | | H7DRV | H7 drive strength (same range as H1DRV). |
| | [14:12] | 1 | | H8DRV | H8 drive strength (same range as H1DRV). |
| 37 | [5:0] | 0 | SCK | SHDLOC | SHD sampling edge location. |
| | [11:6] | 20 | | SHPLOC | SHP sampling edge location. |
| | [17:12] | 10 | | SHPWIDTH | SHP width (controls input dc restore switch active time). |
| 38 | [5:0] | 0 | SCK | DOUTPHASEP | DOUT phase control, positive edge. Specifies location of DOUT. |
| | [11:6] | 20 | | DOUTPHASEN | DOUT phase control, negative edge. Always set to DOUTPHASEP plus 32 edges to maintain 50% duty cycle of internal DOUTPHASE clocking. |
| | [12] | 0 | | DCLKMODE | DCLK mode. 0: DCLK tracks DOUT; 1: DCLK phase is fixed. |
| | [14:13] | 0 | | DOUTDELAY | Data output delay (t_{OD}) with respect to DCLK rising edge. 0: no delay; 1: ~3 ns; 2: ~6 ns; 3: ~9 ns |
| 39 | [15] | 0 | SCK | DCLKINV | Invert DCLK output. 0: no inversion, 1: inversion of DCLK. |
| | [2:0] | 7 | | CPHMASK | Enable H-masking during CP operation. |

Table 34. Test Registers—Do Not Access

| Address | Data Bits | Default Value | Update | Name | Description |
|---------|-----------|---------------|--------|------|-------------------------------------|
| 3E ~ 4F | | | | | Test registers only. Do not access. |

Table 35. Test Registers—Do Not Access

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|------|-------------------------------------|
| 50 ~ 6F | | | | | Test registers only. Do not access. |

Table 36. Shutter and GPO Registers

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|----------------|--|
| 70 | [2:0] | 0 | VD | PRIMARY_ACTION | Selects action for primary and secondary counters. |
| | [5:3] | 0 | | SECOND_ACTION | 0: idle (do nothing) autoreset on VD. 1: activate counter (primary: auto exposure/readout). 2: RapidShot: wrap/repeat counter. 3: ShotTimer: delay start of count. 4: ShotTimer with RapidShot. 5: SLR exposure (manual). |

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| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|--|---|-------------|---|--|
| | [13:6] | 0 | | MANUAL_TRIG | 6: SLR read (manual). 7: force to idle. 1: manual trigger for GP signals, when Protocol 1 is selected. Bit [6] : GP1 manual trigger ... Bit [13] : GP8 manual trigger |
| 71 | [12:0] [24:13] [27:25] | 0 0 0 | VD | PRIMARY_MAX SECOND_MAX VDHD_MASK | Primary counter maximum value. Secondary counter maximum value. Mask VD/HD during counter operation. |
| 72 | [12:0] [13] [26:14] [27] | 0 0 0 0 | VD | PRIMARY_DELAY PRIMARY_SKIP SECOND_DELAY SECOND_SKIP | Number of fields to delay before the next count (exposure) starts. ShotTimer with RapidShot, skip delay before first count (exposure). Number of fields to delay before the next count starts. ShotTimer with RapidShot, skip delay before first count. |
| 73 | [2:0] [5:3] [8:6] [11:9] [14:12] [17:15] [20:18] [23:21] | 0 0 0 0 0 0 0 0 | VD | GP1_PROTOCOL GP2_PROTOCOL GP3_PROTOCOL GP4_PROTOCOL GP5_PROTOCOL GP6_PROTOCOL GP7_PROTOCOL GP8_PROTOCOL | Selects protocol for each general-purpose signal. Idle = 0. No counter association = 1. Link to primary = 2. Link to secondary = 3. Link to mode = 4. Primary repeat = 5. Secondary repeat = 6. Keep on = 7. |
| 74 | [12:0] [25:13] [26] [27] | 0 0 1 0 | VD | SGMASK_NUM SUBCKMASK_NUM SUBCKTOG_UPDATE SUBCKMASK_SKIP1 | Exposure: number of fields to mask SGs. Exposure plus readout: number of fields to mask SUBCK. 0: SUBCK toggles (Register 0x77) updated on SG line. 1: SUBCK toggles (Register 0x77) updated on UPDATE line (VD-updated) Skip the SUBCK mask for the first exposure field only. Typically set to 1. |
| 75 | [0] [13:1] [26:14] [27] | 0 0 0 0 | SG | TEST SUBCKSTARTLINE SUBCKNUM SG_SUPPRESS | Reserved for test purpose. Must be set to 0. Line location after VSG line to begin SUBCK pulses. Must not be set to 1. Number of SUBCK pulses per field. Must be set less than VDLEN. Suppress the SG and allow SUBCK to finish at SUBCKNUM. |
| 76 | [12:0] [25:13] [26] | 1FFF 1FFF 0 | VD | SUBCK_TOG1 SUBCK_TOG2 SUBCK_POL | SUBCK Toggle Position 1. SUBCK Toggle Position 2. SUBCK start polarity. |
| 77 | [12:0] [25:13] | 1FFF 1FFF | VD/SG | SUBCKHP_TOG1 SUBCKHP_TOG2 | Hi-Precision SUBCK Toggle Position 1. Hi-Precision SUBCK Toggle Position 2. |
| 78 | [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] | 0 0 0 0 0 0 0 0 1 1 1 1 1 | VD | GP1_POL GP2_POL GP3_POL GP4_POL GP5_POL GP6_POL GP7_POL GP8_POL SEL_GP1 SEL_GP2 SEL_GP3 SEL_GP4 SEL_GP5 | GP1 low/high start polarity. GP2 low/high start polarity. GP3 low/high start polarity. GP4 low/high start polarity. GP5 low/high start polarity. GP6 low/high start polarity. GP7 low/high start polarity. GP8 low/high start polarity. 1 = GP1 signal is selected for GPO1 output. 1 = GP2 signal is selected for GPO2 output. 1 = GP3 signal is selected for GPO3 output. 1 = GP4 signal is selected for GPO4 output. 0 = SUBCK is selected. 1 = GP5 signal is selected for GPO5 output. 0 = XV21 is selected. |

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|---------------|---|
| | [13] | 1 | | SEL_GP6 | 1 = GP6 signal is selected for GPO6 output. 0 = XV22 is selected. |
| | [14] | 1 | | SEL_GP7 | 1 = GP7 signal is selected for GPO7 output. 0 = XV23 is selected. |
| | [15] | 1 | | SEL_GP8 | 1 = GP8 signal is selected for GPO8 output. 0 = XV24 is selected. |
| | [23:16] | 0 | | GPO_OUTPUT_EN | 1 = GPO outputs enabled. 0 = GPO is input high-Z state (default). |
| | [24] | 0 | | GPO5_OVERRIDE | 1 = when GPO5 configured as input, overrides internal OUT_CONT. |
| | [25] | 0 | | GPO6_OVERRIDE | 1 = when GPO6 configured as input, overrides internal HBLK. |
| | [26] | 0 | | GPO7_OVERRIDE | 1 = when GPO7 configured as input, overrides internal CLPOB. |
| | [27] | 0 | | GPO8_OVERRIDE | 1 = when GPO8 configured as input, overrides internal PBLK. |
| 79 | [7:0] | 0 | VD | GP[*]_USE_LUT | Use result from LUT, or else GP* is unaltered. |
| | [11:8] | {0, 0, 0, 0} | | LUT_FOR_GP12 | Two-input look-up table results. |
| | [15:12] | {0, 0, 0, 0} | | LUT_FOR_GP34 | Examples: {LUT_FOR_GP12} ← {GP2:GP1}. |
| | [19:16] | {0, 0, 0, 0} | | LUT_FOR_GP56 | {0, 1, 1, 0} = GP2 XOR GP1; {1, 1, 1, 0} = GP2 OR GP1. |
| | [23:20] | {0, 0, 0, 0} | | LUT_FOR_GP78 | {0, 1, 1, 1} = GP2 NAND GP1; {1, 0, 0, 0} = GP2 AND GP1. |
| 7A | [12:0] | 0 | VD | GP1_TOG1_FD | General-Purpose Signal 1, first toggle position, field location. |
| | [25:13] | 0 | | GP1_TOG1_LN | General-Purpose Signal 1, first toggle position, line location. |
| 7B | [12:0] | 0 | VD | GP1_TOG1_PX | General-Purpose Signal 1, first toggle position, pixel location. |
| | [25:13] | 0 | | GP1_TOG2_FD | General-Purpose Signal 1, second toggle position, field location. |
| 7C | [12:0] | 0 | VD | GP1_TOG2_LN | General-Purpose Signal 1, second toggle position, line location. |
| | [25:13] | 0 | | GP1_TOG2_PX | General-Purpose Signal 1, second toggle position, pixel location. |
| 7D | [12:0] | 0 | VD | GP1_TOG3_FD | General-Purpose Signal 1, third toggle position, field location. |
| | [25:13] | 0 | | GP1_TOG3_LN | General-Purpose Signal 1, third toggle position, line location. |
| 7E | [12:0] | 0 | VD | GP1_TOG3_PX | General-Purpose Signal 1, third toggle position, pixel location. |
| | [25:13] | 0 | | GP1_TOG4_FD | General-Purpose Signal 1, fourth toggle position, field location. |
| 7F | [12:0] | 0 | VD | GP1_TOG4_LN | General-Purpose Signal 1, fourth toggle position, line location. |
| | [25:13] | 0 | | GP1_TOG4_PX | General-Purpose Signal 1, fourth toggle position, pixel location. |
| 80 | [12:0] | 0 | VD | GP2_TOG1_FD | General-Purpose Signal 2, first toggle position, field location. |
| | [25:13] | 0 | | GP2_TOG1_LN | General-Purpose Signal 2, first toggle position, line location. |
| 81 | [12:0] | 0 | VD | GP2_TOG1_PX | General-Purpose Signal 2, first toggle position, pixel location. |
| | [25:13] | 0 | | GP2_TOG2_FD | General-Purpose Signal 2, second toggle position, field location. |
| 82 | [12:0] | 0 | VD | GP2_TOG2_LN | General-Purpose Signal 2, second toggle position, line location. |
| | [25:13] | 0 | | GP2_TOG2_PX | General-Purpose Signal 2, second toggle position, pixel location. |
| 83 | [12:0] | 0 | VD | GP2_TOG3_FD | General-Purpose Signal 2, third toggle position, field location. |
| | [25:13] | 0 | | GP2_TOG3_LN | General-Purpose Signal 2, third toggle position, line location. |
| 84 | [12:0] | 0 | VD | GP2_TOG3_PX | General-Purpose Signal 2, third toggle position, pixel location. |
| | [25:13] | 0 | | GP2_TOG4_FD | General-Purpose Signal 2, fourth toggle position, field location. |
| 85 | [12:0] | 0 | VD | GP2_TOG4_LN | General-Purpose Signal 2, fourth toggle position, line location. |
| | [25:13] | 0 | | GP2_TOG4_PX | General-Purpose Signal 2, fourth toggle position, pixel location. |
| 86 | [12:0] | 0 | VD | GP3_TOG1_FD | General-Purpose Signal 3, first toggle position, field location. |
| | [25:13] | 0 | | GP3_TOG1_LN | General-Purpose Signal 3, first toggle position, line location. |
| 87 | [12:0] | 0 | VD | GP3_TOG1_PX | General-Purpose Signal 3, first toggle position, pixel location. |
| | [25:13] | 0 | | GP3_TOG2_FD | General-Purpose Signal 3, second toggle position, field location. |
| 88 | [12:0] | 0 | VD | GP3_TOG2_LN | General-Purpose Signal 3, second toggle position, line location. |
| | [25:13] | 0 | | GP3_TOG2_PX | General-Purpose Signal 3, second toggle position, pixel location. |
| 89 | [12:0] | 0 | VD | GP3_TOG3_FD | General-Purpose Signal 3, third toggle position, field location. |
| | [25:13] | 0 | | GP3_TOG3_LN | General-Purpose Signal 3, third toggle position, line location. |
| 8A | [12:0] | 0 | VD | GP3_TOG3_PX | General-Purpose Signal 3, third toggle position, pixel location. |
| | [25:13] | 0 | | GP3_TOG4_FD | General-Purpose Signal 3, fourth toggle position, field location. |
| 8B | [12:0] | 0 | VD | GP3_TOG4_LN | General-Purpose Signal 4, fourth toggle position, line location. |
| | [25:13] | 0 | | GP3_TOG4_PX | General-Purpose Signal 4, fourth toggle position, pixel location. |
| 8C | [12:0] | 0 | VD | GP4_TOG1_FD | General-Purpose Signal 4, first toggle position, field location. |
| | [25:13] | 0 | | GP4_TOG1_LN | General-Purpose Signal 4, first toggle position, line location. |

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| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|-------------|---|
| 8D | [12:0] | 0 | VD | GP4_TOG1_PX | General-Purpose Signal 4, first toggle position, pixel location. |
| | [25:13] | 0 | | GP4_TOG2_FD | General-Purpose Signal 4, second toggle position, field location. |
| 8E | [12:0] | 0 | VD | GP4_TOG2_LN | General-Purpose Signal 4, second toggle position, line location. |
| | [25:13] | 0 | | GP4_TOG2_PX | General-Purpose Signal 4, second toggle position, pixel location. |
| 8F | [12:0] | 0 | VD | GP4_TOG3_FD | General-Purpose Signal 4, third toggle position, field location. |
| | [25:13] | 0 | | GP4_TOG3_LN | General-Purpose Signal 4, third toggle position, line location. |
| 90 | [12:0] | 0 | VD | GP4_TOG3_PX | General-Purpose Signal 4, third toggle position, pixel location. |
| | [25:13] | 0 | | GP4_TOG4_FD | General-Purpose Signal 4, fourth toggle position, field location. |
| 91 | [12:0] | 0 | VD | GP4_TOG4_LN | General-Purpose Signal 4, fourth toggle position, line location. |
| | [25:13] | 0 | | GP4_TOG4_PX | General-Purpose Signal 4, fourth toggle position, pixel location. |
| 92 | [12:0] | 0 | VD | GP5_TOG1_FD | General-Purpose Signal 5, first toggle position, field location. |
| | [25:13] | 0 | | GP5_TOG1_LN | General-Purpose Signal 5, first toggle position, line location. |
| 93 | [12:0] | 0 | VD | GP5_TOG1_PX | General-Purpose Signal 5, first toggle position, pixel location. |
| | [25:13] | 0 | | GP5_TOG2_FD | General-Purpose Signal 5, second toggle position, field location. |
| 94 | [12:0] | 0 | VD | GP5_TOG2_LN | General-Purpose Signal 5, second toggle position, line location. |
| | [25:13] | 0 | | GP5_TOG2_PX | General-Purpose Signal 5, second toggle position, pixel location. |
| 95 | [12:0] | 0 | VD | GP5_TOG3_FD | General-Purpose Signal 5, third toggle position, field location. |
| | [25:13] | 0 | | GP5_TOG3_LN | General-Purpose Signal 5, third toggle position, line location. |
| 96 | [12:0] | 0 | VD | GP5_TOG3_PX | General-Purpose Signal 5, third toggle position, pixel location. |
| | [25:13] | 0 | | GP5_TOG4_FD | General-Purpose Signal 5, fourth toggle position, field location. |
| 97 | [12:0] | 0 | VD | GP5_TOG4_LN | General-Purpose Signal 5, fourth toggle position, line location. |
| | [25:13] | 0 | | GP5_TOG4_PX | General-Purpose Signal 5, fourth toggle position, pixel location. |
| 98 | [12:0] | 0 | VD | GP6_TOG1_FD | General-Purpose Signal 6, first toggle position, field location. |
| | [25:13] | 0 | | GP6_TOG1_LN | General-Purpose Signal 6, first toggle position, line location. |
| 99 | [12:0] | 0 | VD | GP6_TOG1_PX | General-Purpose Signal 6, first toggle position, pixel location. |
| | [25:13] | 0 | | GP6_TOG2_FD | General-Purpose Signal 6, second toggle position, field location. |
| 9A | [12:0] | 0 | VD | GP6_TOG2_LN | General-Purpose Signal 6, second toggle position, line location. |
| | [25:13] | 0 | | GP6_TOG2_PX | General-Purpose Signal 6, second toggle position, pixel location. |
| 9B | [12:0] | 0 | VD | GP6_TOG3_FD | General-Purpose Signal 6, third toggle position, field location. |
| | [25:13] | 0 | | GP6_TOG3_LN | General-Purpose Signal 6, third toggle position, line location. |
| 9C | [12:0] | 0 | VD | GP6_TOG3_PX | General-Purpose Signal 6, third toggle position, pixel location. |
| | [25:13] | 0 | | GP6_TOG4_FD | General-Purpose Signal 6, fourth toggle position, field location. |
| 9D | [12:0] | 0 | VD | GP6_TOG4_LN | General-Purpose Signal 6, fourth toggle position, line location. |
| | [25:13] | 0 | | GP6_TOG4_PX | General-Purpose Signal 6, fourth toggle position, pixel location. |
| 9E | [12:0] | 0 | VD | GP7_TOG1_FD | General-Purpose Signal 7, first toggle position, field location. |
| | [25:13] | 0 | | GP7_TOG1_LN | General-Purpose Signal 7, first toggle position, line location. |
| 9F | [12:0] | 0 | VD | GP7_TOG1_PX | General-Purpose Signal 7, first toggle position, pixel location. |
| | [25:13] | 0 | | GP7_TOG2_FD | General-Purpose Signal 7, second toggle position, field location. |
| A0 | [12:0] | 0 | VD | GP7_TOG2_LN | General-Purpose Signal 7, second toggle position, line location. |
| | [25:13] | 0 | | GP7_TOG2_PX | General-Purpose Signal 7, second toggle position, pixel location. |
| A1 | [12:0] | 0 | VD | GP7_TOG3_FD | General-Purpose Signal 7, third toggle position, field location. |
| | [25:13] | 0 | | GP7_TOG3_LN | General-Purpose Signal 7, third toggle position, line location. |
| A2 | [12:0] | 0 | VD | GP7_TOG3_PX | General-Purpose Signal 7, third toggle position, pixel location. |
| | [25:13] | 0 | | GP7_TOG4_FD | General-Purpose Signal 7, fourth toggle position, field location. |
| A3 | [12:0] | 0 | VD | GP7_TOG4_LN | General-Purpose Signal 7, fourth toggle position, line location. |
| | [25:13] | 0 | | GP7_TOG4_PX | General-Purpose Signal 7, fourth toggle position, pixel location. |
| A4 | [12:0] | 0 | VD | GP8_TOG1_FD | General-Purpose Signal 8, first toggle position, field location. |
| | [25:13] | 0 | | GP8_TOG1_LN | General-Purpose Signal 8, first toggle position, line location. |
| A5 | [12:0] | 0 | VD | GP8_TOG1_PX | General-Purpose Signal 8, first toggle position, pixel location. |
| | [25:13] | 0 | | GP8_TOG2_FD | General-Purpose Signal 8, second toggle position, field location. |

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|-----------------|---|
| A6 | [12:0] | 0 | VD | GP8_TOG2_LN | General-Purpose Signal 8, second toggle position, line location. |
| | [25:13] | 0 | | GP8_TOG2_PX | General-Purpose Signal 8, second toggle position, pixel location. |
| A7 | [12:0] | 0 | VD | GP8_TOG3_FD | General-Purpose Signal 8, third toggle position, field location. |
| | [25:13] | 0 | | GP8_TOG3_LN | General-Purpose Signal 8, third toggle position, line location. |
| A8 | [12:0] | 0 | VD | GP8_TOG3_PX | General-Purpose Signal 8, third toggle position, pixel location. |
| | [25:13] | 0 | | GP8_TOG4_FD | General-Purpose Signal 8, fourth toggle position, field location. |
| A9 | [12:0] | 0 | VD | GP8_TOG4_LN | General-Purpose Signal 8, fourth toggle position, line location. |
| | [25:13] | 0 | | GP8_TOG4_PX | General-Purpose Signal 8, fourth toggle position, pixel location. |
| AA | [0] | 0 | VD | SUBCK_TOG1_13 | Bit [13] for SUBCK Toggle Position 1. For 14-bit H-counter mode. |
| | [1] | 0 | VD | SUBCK_TOG2_13 | Bit [13] for SUBCK Toggle Position 2. For 14-bit H-counter mode. |
| | [2] | 0 | VD/SG | SUBCKHP_TOG1_13 | Bit [13] for SUBCK HP Toggle 1. For 14-bit H-counter mode. |
| | [3] | 0 | VD/SG | SUBCKHP_TOG2_13 | Bit [13] for SUBCK HP Toggle 2. For 14-bit H-counter mode. |

Table 37. Update Control Registers

| Address | Data Bits | Default Value | Update | Name | Description |
|---------|-----------|---------------|--------|---------------|---|
| B0 | [15:0] | 1803 | SCK | AFE_UPDT_SCK | Each bit corresponds to one address location. AFE_UPDT_SCK [0] = 1, update Address 0x00 on SL rising edge. AFE_UPDT_SCK [1] = 1, update Address 0x01 on SL rising edge. ... AFE_UPDT_SCK [15] = 1, update Address 0x0F on SL rising edge. |
| B1 | [15:0] | E7FC | SCK | AFE_UPDT_VD | Each bit corresponds to one address location. AFE_UPDT_VD [0] = 1, update Address 0x00 on VD rising edge. AFE_UPDT_VD [1] = 1, update Address 0x01 on VD rising edge. ... AFE_UPDT_VD [15] = 1, update Address 0x0F on VD rising edge. |
| B2 | [15:0] | F8FD | SCK | MISC_UPDT_SCK | Enable SCK update of miscellaneous registers, Address 0x10 to Address 0x1F. |
| B3 | [15:0] | 0702 | SCK | MISC_UPDT_VD | Enable VD update of miscellaneous registers, Address 0x10 to Address 0x1F. |
| B4 | [15:0] | FFF9 | SCK | VDHD_UPDT_SCK | Enable SCK update of VDHD registers, Address 0x20 to Address 0x2F. |
| B5 | [15:0] | 0006 | SCK | VDHD_UPDT_VD | Enable VD update of VDHD registers, Address 0x20 to Address 0x2F. |

Table 38. Extra Registers

| Address | Data Bits | Default Value | Update | Name | Description |
|---------|-----------|---------------|--------|------------|--|
| D4 | [0] | 0 | SCK | TEST | Test use only. Set to 0. |
| | [1] | 0 | | GPO_INT_EN | Allow observation of internal signals at GPO5 to GPO8 outputs. GPO5: OUTCONTROL. GPO6: HBLK. GPO7: CLPOB. GPO8: PBLK. |
| | [9:2] | 0 | | TEST | Test use only. Set to 0. |
| D7 | [0] | 0 | SCK | TEST | Test use only. Set to 0. |
| | [1] | 0 | | XV24_SWAP | Set to 1 to change the V-driver output configuration so that XV15 is output on the XV24 output pin. Useful with special vertical sequence alternation mode when the XV24 register is reserved for pattern selection. |
| D8 | [27:0] | 0 | SCK | START | Recommended start-up register. Should be set to 0x888. |

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Table 39. V-Pattern Group (VPAT) Register Map

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|---------|------------------------|
| 00 | [12:0] | X | SCP | V1TOG1 | V1 Toggle Position 1. |
| | [25:13] | X | | V1TOG2 | V1 Toggle Position 2. |
| 01 | [12:0] | X | SCP | V1TOG3 | V1 Toggle Position 3. |
| | [25:13] | X | | V1TOG4 | V1 Toggle Position 4. |
| 02 | [12:0] | X | SCP | V2TOG1 | V2 Toggle Position 1. |
| | [25:13] | X | | V2TOG2 | V2 Toggle Position 2. |
| 03 | [12:0] | X | SCP | V2TOG3 | V2 Toggle Position 3. |
| | [25:13] | X | | V2TOG4 | V2 Toggle Position 4. |
| 04 | [12:0] | X | SCP | V3TOG1 | V3 Toggle Position 1. |
| | [25:13] | X | | V3TOG2 | V3 Toggle Position 2. |
| 05 | [12:0] | X | SCP | V3TOG3 | V3 Toggle Position 3. |
| | [25:13] | X | | V3TOG4 | V3 Toggle Position 4. |
| 06 | [12:0] | X | SCP | V4TOG1 | V4 Toggle Position 1. |
| | [25:13] | X | | V4TOG2 | V4 Toggle Position 2. |
| 07 | [12:0] | X | SCP | V4TOG3 | V4 Toggle Position 3. |
| | [25:13] | X | | V4TOG4 | V4 Toggle Position 4. |
| 08 | [12:0] | X | SCP | V5TOG1 | V5 Toggle Position 1. |
| | [25:13] | X | | V5TOG2 | V5 Toggle Position 2. |
| 09 | [12:0] | X | SCP | V5TOG3 | V5 Toggle Position 3. |
| | [25:13] | X | | V5TOG4 | V5 Toggle Position 4. |
| 0A | [12:0] | X | SCP | V6TOG1 | V6 Toggle Position 1. |
| | [25:13] | X | | V6TOG2 | V6 Toggle Position 2. |
| 0B | [12:0] | X | SCP | V6TOG3 | V6 Toggle Position 3. |
| | [25:13] | X | | V6TOG4 | V6 Toggle Position 4. |
| 0C | [12:0] | X | SCP | V7TOG1 | V7 Toggle Position 1. |
| | [25:13] | X | | V7TOG2 | V7 Toggle Position 2. |
| 0D | [12:0] | X | SCP | V7TOG3 | V7 Toggle Position 3. |
| | [25:13] | X | | V7TOG4 | V7 Toggle Position 4. |
| 0E | [12:0] | X | SCP | V8TOG1 | V8 Toggle Position 1. |
| | [25:13] | X | | V8TOG2 | V8 Toggle Position 2. |
| 0F | [12:0] | X | SCP | V8TOG3 | V8 Toggle Position 3. |
| | [25:13] | X | | V8TOG4 | V8 Toggle Position 4. |
| 10 | [12:0] | X | SCP | V9TOG1 | V9 Toggle Position 1. |
| | [25:13] | X | | V9TOG2 | V9 Toggle Position 2. |
| 11 | [12:0] | X | SCP | V9TOG3 | V9 Toggle Position 3. |
| | [25:13] | X | | V9TOG4 | V9 Toggle Position 4. |
| 12 | [12:0] | X | SCP | V10TOG1 | V10 Toggle Position 1. |
| | [25:13] | X | | V10TOG2 | V10 Toggle Position 2. |
| 13 | [12:0] | X | SCP | V10TOG3 | V10 Toggle Position 3. |
| | [25:13] | X | | V10TOG4 | V10 Toggle Position 4. |
| 14 | [12:0] | X | SCP | V11TOG1 | V11 Toggle Position 1. |
| | [25:13] | X | | V11TOG2 | V11 Toggle Position 2. |
| 15 | [12:0] | X | SCP | V11TOG3 | V11 Toggle Position 3. |
| | [25:13] | X | | V11TOG4 | V11 Toggle Position 4. |
| 16 | [12:0] | X | SCP | V12TOG1 | V12 Toggle Position 1. |
| | [25:13] | X | | V12TOG2 | V12 Toggle Position 2. |
| 17 | [12:0] | X | SCP | V12TOG3 | V12 Toggle Position 3. |
| | [25:13] | X | | V12TOG4 | V12 Toggle Position 4. |
| 18 | [12:0] | X | SCP | V13TOG1 | V13 Toggle Position 1. |
| | [25:13] | X | | V13TOG2 | V13 Toggle Position 2. |

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|---------|------------------------|
| 19 | [12:0] | X | SCP | V13TOG3 | V13 Toggle Position 3. |
| | [25:13] | X | | V13TOG4 | V13 Toggle Position 4. |
| 1A | [12:0] | X | SCP | V14TOG1 | V14 Toggle Position 1. |
| | [25:13] | X | | V14TOG2 | V14 Toggle Position 2. |
| 1B | [12:0] | X | SCP | V14TOG3 | V14 Toggle Position 3. |
| | [25:13] | X | | V14TOG4 | V14 Toggle Position 4. |
| 1C | [12:0] | X | SCP | V15TOG1 | V15 Toggle Position 1. |
| | [25:13] | X | | V15TOG2 | V15 Toggle Position 2. |
| 1D | [12:0] | X | SCP | V15TOG3 | V15 Toggle Position 3. |
| | [25:13] | X | | V15TOG4 | V15 Toggle Position 4. |
| 1E | [12:0] | X | SCP | V16TOG1 | V16 Toggle Position 1. |
| | [25:13] | X | | V16TOG2 | V16 Toggle Position 2. |
| 1F | [12:0] | X | SCP | V16TOG3 | V16 Toggle Position 3. |
| | [25:13] | X | | V16TOG4 | V16 Toggle Position 4. |
| 20 | [12:0] | X | SCP | V17TOG1 | V17 Toggle Position 1. |
| | [25:13] | X | | V17TOG2 | V17 Toggle Position 2. |
| 21 | [12:0] | X | SCP | V17TOG3 | V17 Toggle Position 3. |
| | [25:13] | X | | V17TOG4 | V17 Toggle Position 4. |
| 22 | [12:0] | X | SCP | V18TOG1 | V18 Toggle Position 1. |
| | [25:13] | X | | V18TOG2 | V18 Toggle Position 2. |
| 23 | [12:0] | X | SCP | V18TOG3 | V18 Toggle Position 3. |
| | [25:13] | X | | V18TOG4 | V18 Toggle Position 4. |
| 24 | [12:0] | X | SCP | V19TOG1 | V19 Toggle Position 1. |
| | [25:13] | X | | V19TOG2 | V19 Toggle Position 2. |
| 25 | [12:0] | X | SCP | V19TOG3 | V19 Toggle Position 3. |
| | [25:13] | X | | V19TOG4 | V19 Toggle Position 4. |
| 26 | [12:0] | X | SCP | V20TOG1 | V20 Toggle Position 1. |
| | [25:13] | X | | V20TOG2 | V20 Toggle Position 2. |
| 27 | [12:0] | X | SCP | V20TOG3 | V20 Toggle Position 3. |
| | [25:13] | X | | V20TOG4 | V20 Toggle Position 4. |
| 28 | [12:0] | X | SCP | V21TOG1 | V21 Toggle Position 1. |
| | [25:13] | X | | V21TOG2 | V21 Toggle Position 2. |
| 29 | [12:0] | X | SCP | V21TOG3 | V21 Toggle Position 3. |
| | [25:13] | X | | V21TOG4 | V21 Toggle Position 4. |
| 2A | [12:0] | X | SCP | V22TOG1 | V22 Toggle Position 1. |
| | [25:13] | X | | V22TOG2 | V22 Toggle Position 2. |
| 2B | [12:0] | X | SCP | V22TOG3 | V22 Toggle Position 3. |
| | [25:13] | X | | V22TOG4 | V22 Toggle Position 4. |
| 2C | [12:0] | X | SCP | V23TOG1 | V23 Toggle Position 1. |
| | [25:13] | X | | V23TOG2 | V23 Toggle Position 2. |
| 2D | [12:0] | X | SCP | V23TOG3 | V23 Toggle Position 3. |
| | [25:13] | X | | V23TOG4 | V23 Toggle Position 4. |
| 2E | [12:0] | X | SCP | V24TOG1 | V24 Toggle Position 1. |
| | [25:13] | X | | V24TOG2 | V24 Toggle Position 2. |
| 2F | [12:0] | X | SCP | V24TOG3 | V24 Toggle Position 3. |
| | [25:13] | X | | V24TOG4 | V24 Toggle Position 4. |

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Table 40. V-Sequence (VSEQ) Registers

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|---|---------------|---|
| 00 | [0] | X | SCP | CLPOBPOL | CLPOB start polarity. |
| | [1] | X | | PBLKPOL | PBLK start polarity. |
| | [5:2] | X | | HOLD | 1 = enable HOLD function for each VPAT group (A, B, C, D). |
| | [9:6] | X | | VMASK_EN | 1 = enable FREEZE/RESUME for each VPAT group (A, B, C, D). |
| | [13:10] | X | | CONCAT_GRP | Combine multiple VPAT groups together in one sequence. Set register equal to 0x01 to enable. |
| | [15:14] | X | | VREP_MODE | Defines V-alternation repetition mode. 00 = single pattern alternation for all groups. 01 = two pattern alternation for all groups. 10 = three-pattern alternation for Group A. Groups B, C, and D follow pattern {0, 1, 1, 0, 1, 1...}. 11 = four-pattern alternation for Group A. Two-pattern alternation for Groups B, C, and D. |
| | [19:16] | X | | LASTREPLEN_EN | Enable use of last repetition counter for last repetition length of each group. |
| [23:20] | X | LASTTOG_EN | Enable the fifth toggle position for all V-signals in each group. | | |
| [25:24] | X | HBLK_MODE | Selection of HBLK modes. 00 = HBLK Mode 0 (normal six-toggle operation). 01 = HBLK Mode 1. 10 = HBLK Mode 2. (Address 0x19 to Address 0x1E operate differently.) 11 = test only, do not access. | | |
| 01 | [12:0] | X | SCP | HDLENE | HD line length for even lines. |
| | [25:13] | X | | HDLENO | HD line length for odd lines. |
| 02 | [23:0] | X | SCP | VSGPATSEL | Selects which two toggle positions are used by each V-output when they are configured as VSG pulses (Miscellaneous Register Address 0x1C, fixed register area). 0 = use Toggles 1, 2; 1 = use Toggles 3, 4. |
| | [24] | | | HDLENE_13 | HD length Bit [13] for even lines when 14-bit H-counter is enabled. |
| | [25] | | | HDLENO_13 | HD length Bit [13] for odd lines when 14-bit H-counter is enabled. |
| 03 | [23:0] | X | SCP | VPOL_A | Starting polarities for each V-output signal (Group A). |
| 04 | [23:0] | X | SCP | VPOL_B | Starting polarities for each V-output signal (Group B). |
| 05 | [23:0] | X | SCP | VPOL_C | Starting polarities for each V-output signal (Group C). |
| 06 | [23:0] | X | SCP | VPOL_D | Starting polarities for each V-output signal (Group D). |
| 07 | [23:0] | X | SCP | GROUPSEL_0 | Select which group each V1 ~ V12 signal is assigned to. 00 = Group A, 01 = Group B, 10 = Group C, 11 = Group D. [1:0]: V1; [3:2]: V2 ... [23:22]: V12. |
| 08 | [23:0] | X | SCP | GROUPSEL_1 | Select which group each V13 ~ V24 signal is assigned to. 00 = Group A, 01 = Group B, 10 = Group C, 11 = Group D. [1:0]: V13; [3:2]: V14 ... [23:22]: V24. |
| 09 | [4:0] | X | SCP | VPATSELA | Selected VPAT group for Group A, from VPAT Group 0 ~ 31. |
| | [9:5] | X | | VPATSELB | Selected VPAT group for Group B, from VPAT Group 0 ~ 31. |
| | [14:10] | X | | VPATSELC | Selected VPAT group for Group C, from VPAT Group 0 ~ 31. |
| | [19:15] | X | | VPATSELD | Selected VPAT group for Group D, from VPAT Group 0 ~ 31. |
| 0A | [12:0] | X | SCP | VSTARTA | Start position of selected V-Pattern Group A. |
| | [25:13] | X | | VLENA | Length of selected V-Pattern Group A. |
| 0B | [12:0] | X | SCP | VREPA_1 | Number of repetitions for V-Pattern Group A for first lines. |
| | [25:13] | X | | VREPA_2 | Number of repetitions for V-Pattern Group A for second lines. |
| 0C | [12:0] | X | SCP | VREPA_3 | Number of repetitions for V-Pattern Group A for third lines. |
| | [25:13] | X | | VREPA_4 | Number of repetitions for V-Pattern Group A for fourth lines. |
| 0D | [12:0] | X | SCP | VSTARTB | Start position of selected V-Pattern Group B. |
| | [25:13] | X | | VLENB | Length of selected V-Pattern Group B. |
| 0E | [12:0] | X | SCP | VREP_B_ODD | Number of repetitions for V-Pattern Group B for odd lines. |
| | [25:13] | X | | VREP_B_EVEN | Number of repetitions for V-Pattern Group B for even lines. |

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|-------------|--|
| 0F | [12:0] | X | SCP | VSTARTC | Start position of selected V-Pattern Group C. |
| | [25:13] | X | | VLENC | Length of selected V-Pattern Group C. |
| 10 | [12:0] | X | SCP | VREPC_ODD | Number of repetitions for V-Pattern Group C for odd lines. |
| | [25:13] | X | | VREPC_EVEN | Number of repetitions for V-Pattern Group C for even lines. |
| 11 | [12:0] | X | SCP | VSTARTD | Start position of selected V-Pattern Group D. |
| | [25:13] | X | | VLEND | Length of selected V-Pattern Group D. |
| 12 | [12:0] | X | SCP | VREPD_ODD | Number of repetitions for V-Pattern Group D for odd lines. |
| | [25:13] | X | | VREPD_EVEN | Number of repetitions for V-Pattern Group D for even lines. |
| 13 | [12:0] | X | SCP | FREEZE1 | Holds the V-outputs at their current levels. |
| | [25:13] | X | | RESUME1 | Resumes the operation of V-outputs to finish the pattern. |
| 14 | [12:0] | X | SCP | FREEZE2 | Holds the V-outputs at their current levels. |
| | [25:13] | X | | RESUME2 | Resumes the operation of V-outputs to finish the pattern. |
| 15 | [12:0] | X | SCP | FREEZE3 | Holds the V-outputs at their current levels. |
| | [25:13] | X | | RESUME3 | Resumes the operation of V-outputs to finish the pattern. |
| 16 | [12:0] | X | SCP | FREEZE4 | Holds the V-outputs at their current levels. |
| | [25:13] | X | | RESUME4 | Resumes the operation of V-outputs to finish the pattern. |
| 17 | [12:0] | X | SCP | HBLKSTART | Start location for HBLK in HBLK Modes 1 and 2. |
| | [25:13] | X | | HBLKEND | End location for HBLK in HBLK Modes 1 and 2. |
| 18 | [12:0] | X | SCP | HBLKLEN | HBLK length in HBLK Modes 1 and 2. |
| | [20:13] | X | | HBLKREP | Number of HBLK repetitions in HBLK Modes 1 and 2. |
| | [21] | X | | HBLKMASK_H1 | Masking polarity for H1/H3/H5/H7 during HBLK. |
| | [22] | X | | HBLKMASK_H2 | Masking polarity for H2/H4/H6/H8 during HBLK. |
| | [23] | X | | HBLKMASK_HL | Masking polarity for HL during HBLK. |
| | [25:24] | X | | TEST | Test use only. Set to 0. |
| 19 | [12:0] | X | SCP | HBLKTOGO1 | First HBLK toggle position for odd lines, or RA0H1REPABC in HBLK Mode 2 (see HBLK Mode 2 Operation for more information). |
| | [25:13] | X | | HBLKTOGO2 | Second HBLK toggle position for odd lines, or RA1H1REPABC. |
| 1A | [12:0] | X | SCP | HBLKTOGO3 | Third HBLK toggle position for odd lines, or RA2H1REPABC. |
| | [25:13] | X | | HBLKTOGO4 | Fourth HBLK toggle position for odd lines, or RA3H1REPABC. |
| 1B | [12:0] | X | SCP | HBLKTOGO5 | Fifth HBLK toggle position for odd lines, or RA4H1REPABC. |
| | [25:13] | X | | HBLKTOGO6 | Sixth HBLK toggle position for odd lines, or RA5H1REPABC. |
| 1C | [12:0] | X | SCP | HBLKTOGE1 | First HBLK toggle position for even lines, or RA0H2REPABC. |
| | [25:13] | X | | HBLKTOGE2 | Second HBLK toggle position for even lines, or RA1H2REPABC. |
| 1D | [12:0] | X | SCP | HBLKTOGE3 | Third HBLK toggle position for even lines, or RA2H2REPABC. |
| | [25:13] | X | | HBLKTOGE4 | Fourth HBLK toggle position for even lines, or RA3H2REPABC. |
| 1E | [12:0] | X | SCP | HBLKTOGE5 | Fifth HBLK toggle position for even lines, or RA4H2REPABC. |
| | [25:13] | X | | HBLKTOGE6 | Sixth HBLK toggle position for even lines, or RA5H2REPABC. |
| 1F | [12:0] | X | SCP | HBLKSTARTA | HBLK Repeat Area Start Position A for HBLK Mode 2. Set to 8191 if not used. |
| | [25:13] | X | | HBLKSTARTB | HBLK Repeat Area Start Position B for HBLK Mode 2. Set to 8191 if not used. |
| 20 | [12:0] | X | SCP | HBLKSTARTC | HBLK Repeat Area Start Position C for HBLK Mode 2. Set to 8191 if not used. |
| | [13] | X | | VSEQALT_EN | Special V-sequence alternation enable. |
| | [14] | X | | VALT_MAP | 1 = enables operation of VALTSEL0_EVEN/ODD, VALTSEL1_EVEN/ODD registers in FREEZE/RESUME registers. Must be enabled if special VALT mode is used. |
| | [17:15] | X | | SPC_PAT_EN | 1 = enables use of special vertical pattern insertion into VPATA sequence. [0]: use VPATB as the special pattern. [1]: use VPATC as the special pattern. [2]: use VPATD as the special pattern. |

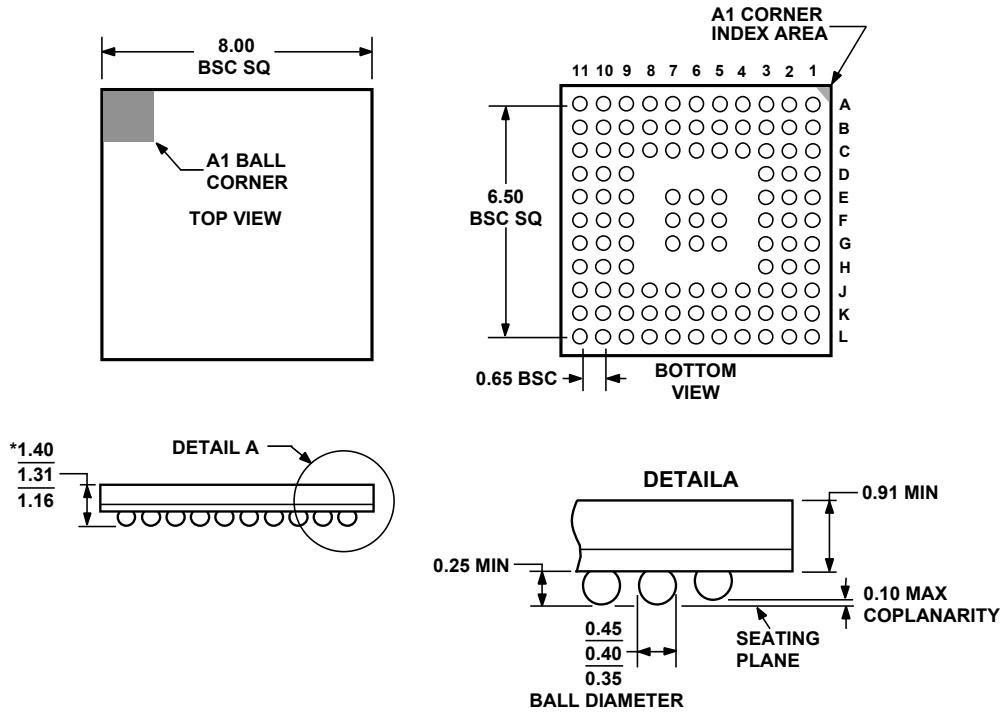
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| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|-----------|---------------|-------------|--------------|---|
| 21 | [2:0] | X | SCP | HBLKALT_PAT1 | HBLK Mode 2, Repeat Area 0 pattern for odd lines. |
| | [6:4] | X | | HBLKALT_PAT2 | HBLK Mode 2, Repeat Area 0 pattern for odd lines. |
| | [10:8] | X | | HBLKALT_PAT3 | HBLK Mode 2, Repeat Area 0 pattern for odd lines. |
| | [14:12] | X | | HBLKALT_PAT4 | HBLK Mode 2, Repeat Area 0 pattern for odd lines. |
| | [18:16] | X | | HBLKALT_PAT5 | HBLK Mode 2, Repeat Area 0 pattern for odd lines. |
| | [22:20] | X | | HBLKALT_PAT6 | HBLK Mode 2, Repeat Area 0 pattern for odd lines. |
| 22 | [12:0] | X | SCP | CLPOBTOG1 | CLPOB Toggle Position 1. |
| | [25:13] | X | | CLPOBTOG2 | CLPOB Toggle Position 2. |
| 23 | [12:0] | X | SCP | PBLKTOG1 | PBLK Toggle Position 1. |
| | [25:13] | X | | PBLKTOG2 | PBLK Toggle Position 2. |
| 24 | [12:0] | X | SCP | LASTREPLEN_A | Last repetition length for Group A. Set equal to VLENA. |
| | [25:13] | X | | LASTREPLEN_B | Last repetition length for Group B. Set equal to VLENB. |
| 25 | [12:0] | X | SCP | LASTREPLEN_C | Last repetition length for Group C. Set equal to VLENC. |
| | [25:13] | X | | LASTREPLEN_D | Last repetition length for Group D. Set equal to VLEND. |
| 26 | [12:0] | X | SCP | LASTTOG_A | Optional fifth toggle position for Group A. |
| | [25:13] | X | | LASTTOG_B | Optional fifth toggle position for Group B. |
| 27 | [12:0] | X | SCP | LASTTOG_C | Optional fifth toggle position for Group C. |
| | [25:13] | X | | LASTTOG_D | Optional fifth toggle position for Group D. |

Table 41. Field Registers

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|--------------------|---------------|-------------|-------------------------------|---|
| 00 | [4:0] | X | VD | SEQ0 | Selected V-sequence for first region in the field. |
| | [9:5] | X | | SEQ1 | Selected V-sequence for second region in the field. |
| | [14:10] | X | | SEQ2 | Selected V-sequence for third region in the field. |
| | [19:15] | X | | SEQ3 | Selected V-sequence for fourth region in the field. |
| | [24:20] | X | | SEQ4 | Selected V-sequence for fifth region in the field. |
| 01 | [4:0] | X | VD | SEQ5 | Selected V-sequence for sixth region in the field. |
| | [9:5] | X | | SEQ6 | Selected V-sequence for seventh region in the field. |
| | [14:10] | X | | SEQ7 | Selected V-sequence for eighth region in the field. |
| | [19:15] | X | | SEQ8 | Selected V-sequence for ninth region in the field. |
| | [21:20] | | | MULT_SWEEP0 | Enables multiplier mode and/or sweep mode for Region 0. 0: multiplier off/sweep off; 1: multiplier off/sweep on; 2: multiplier on/sweep off; 3: multiplier on/sweep on. |
| | [23:22] [25:24] | | | MULT_SWEEP1 MULT_SWEEP2 | Enables multiplier mode and/or sweep mode for Region 2. Enables multiplier mode and/or sweep mode for Region 1. |
| 02 | [12:0] | X | VD | HDLASTLEN | HD last line length. Line length of last line in the field. |
| | [14:13] | X | | MULT_SWEEP3 | Enables multiplier mode and/or sweep mode for Region 3. |
| | [16:15] | X | | MULT_SWEEP4 | Enables multiplier mode and/or sweep mode for Region 4. |
| | [18:17] | X | | MULT_SWEEP5 | Enables multiplier mode and/or sweep mode for Region 5. |
| | [20:19] | X | | MULT_SWEEP6 | Enables multiplier mode and/or sweep mode for Region 6. |
| | [22:21] | X | | MULT_SWEEP7 | Enables multiplier mode and/or sweep mode for Region 7. |
| | [24:23] | X | | MULT_SWEEP8 | Enables multiplier mode and/or sweep mode for Region 8. |
| | [25] | | | HDLASTLEN_13 | HD last line length Bit [13] when 14-bit H-counter is enabled. |
| | 03 | [12:0] | | X | VD |
| [25:13] | | X | SCP1 | V-Sequence Change Position 1. | |
| 04 | [12:0] | X | VD | SCP2 | V-Sequence Change Position 2. |
| | [25:13] | X | | SCP3 | V-Sequence Change Position 3. |
| 05 | [12:0] | X | VD | SCP4 | V-Sequence Change Position 4. |
| | [25:13] | X | | SCP5 | V-Sequence Change Position 5. |
| 06 | [12:0] | X | VD | SCP6 | V-Sequence Change Position 6. |
| | [25:13] | X | | SCP7 | V-Sequence Change Position 7. |
| 07 | [12:0] | X | VD | SCP8 | V-Sequence Change Position 8. |
| | [25:13] | | | VDLEN | VD field length (number of lines in the field). |
| 08 | [12:0] | X | VD | SGACTLINE1 | SG Active Line 1. |
| | [25:13] | X | | SGACTLINE2 | SG Active Line 2 (set to SG Active Line 1 or maximum if not used). |
| 09 | [23:0] | X | VD | SGMASK | Masking of VSG outputs during SG active line. |
| 0A | [12:0] | X | VD | CLPMASKSTART1 | CLPOB Mask Region 1 start position. Set to 8191 to disable. |
| | [25:13] | X | | CLPMASKEND1 | CLPOB Mask Region 1 end position. Set to 0 to disable. |
| 0B | [12:0] | X | VD | CLPMASKSTART2 | CLPOB Mask Region 2 start position. Set to 8191 to disable. |
| | [25:13] | X | | CLPMASKEND2 | CLPOB Mask Region 2 end position. Set to 0 to disable. |
| 0C | [12:0] | X | VD | CLPMASKSTART3 | CLPOB Mask Region 3 start position. Set to 8191 to disable. |
| | [25:13] | X | | CLPMASKEND3 | CLPOB Mask Region 3 end position. Set to 0 to disable. |
| 0D | [12:0] | X | VD | PBLKMASKSTART1 | PBLK Mask Region 1 start position. Set to 8191 to disable. |
| | [25:13] | X | | PBLKMASKEND1 | PBLK Mask Region 1 end position. Set to 0 to disable. |
| 0E | [12:0] | X | VD | PBLKMASKSTART2 | PBLK Mask Region 2 start position. Set to 8191 to disable. |
| | [25:13] | X | | PBLKMASKEND2 | PBLK Mask Region 2 end position. Set to 0 to disable. |
| 0F | [12:0] | X | VD | PBLKMASKSTART3 | PBLK Mask Region 3 start position. Set to 8191 to disable. |
| | [25:13] | X | | PBLKMASKEND3 | PBLK Mask Region 3 end position. Set to 0 to disable. |

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-225
WITH THE EXCEPTION TO PACKAGE HEIGHT.

Figure 87. 105-Lead Chip Scale Package Ball Grid Array [CSP_BGA]
8 mm × 8 mm Body
(BC-105)
Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---------------------------|-------------------|---------------------|----------------|
| AD9992BBCZ ¹ | -25°C to +85°C | 105-Lead CSP_BGA | BC-105 |
| AD9992BBCZRL ¹ | -25°C to +85°C | 105-Lead CSP_BGA | BC-105 |

¹ Z = Pb-free part.

NOTES

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NOTES