

**NOTES:**

1.0 DESIGNED TO PROTECT AGAINST GR1089 INTRABUILDING AND ESD SURGES.

2.0 PINS WITHOUT ELECTRICAL CONNECTION ARE OMITTED.

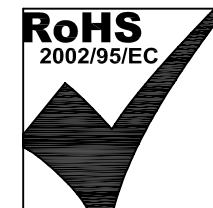
3.0 ALL RESISTORS ARE ±5% TOLERANCE.

ELECTRICAL SPECIFICATIONS:

1.0 TURNS RATIO: (P4-P5-P6) : (J3-J6) : 1CT : 1CT ± 3%  
 (P3-P2-P1) : (J1-J2) : 1CT : 1CT ± 3%

2.0 INDUCTANCE: (P4-P6) : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias  
 (P3-P1) : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias

3.0 DC RESISTANCE: (J6-J3)=(J2-J1) : 2.0 ohms Max.



Bel Stewart Connector  
 11118 Susquehanna Trail, South  
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SHEET 1 OF 4

DRAWING NO. SI-53024-F

REV. 05

RECEIVE

4.0 RETURN LOSS: APPLY 100 OHMS LOAD EACH TO (P4-P6) AND (P1-P3)

1MHz TO 30MHz  
31MHz TO 80MHz

: 18dB MIN.  
: 12dB MIN.

NOTE: SOURCE APPLIED TO (J2-J1) OR (J3-J6).

5.0 INSERTION LOSS: RSource=RLoad=100 OHMS

100KHz TO 100MHz

: 1.1 dB TYP

6.0 CROSS TALK: 1-100 MHz

: 30 dB TYP

7.0 COMMON TO COMMON MODE ATTENUATION: 1MHz TO 100MHz

: 35dB TYP

8.0 RISE TIME: RS=100 OHMS AND RL = 100 OHMS

OUTPUT VOLTAGE = 1 V peak  
PULSE WIDTH= 112nS

: 3.0 nS MAX  
: 3.0 nS MAX

9.0 DIELECTRIC WITHSTAND: (J1, J2) TO (P1, P3)

(J3, J6) TO (P4,P6)

: 1500 VAC  
: 1500 VAC

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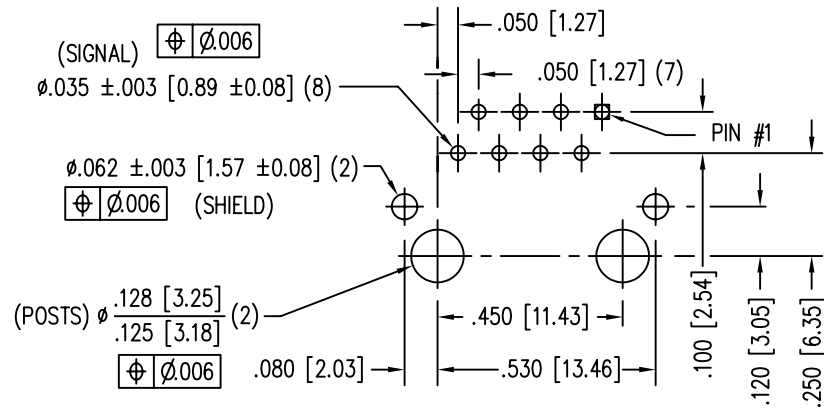
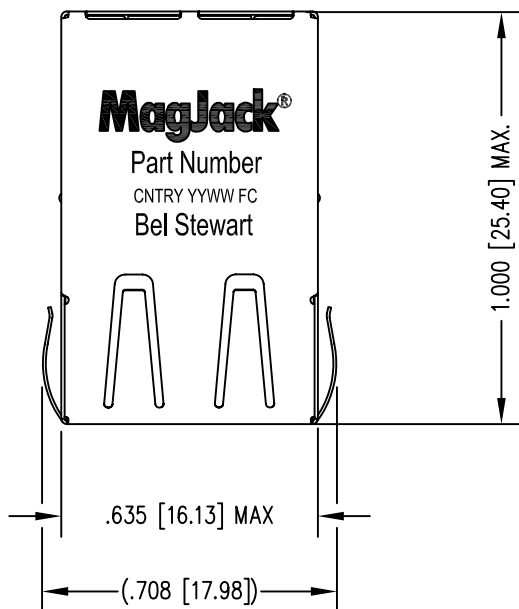
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SHEET  
2 OF 4

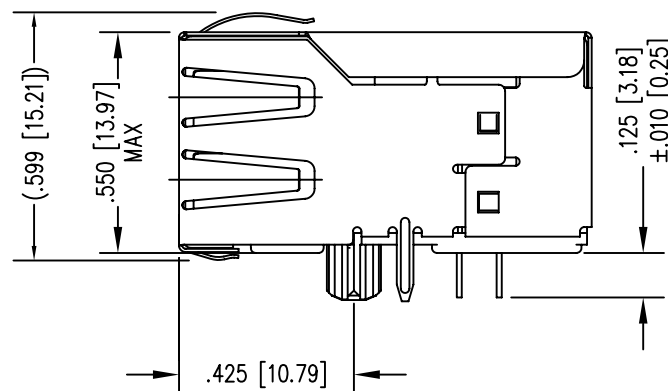
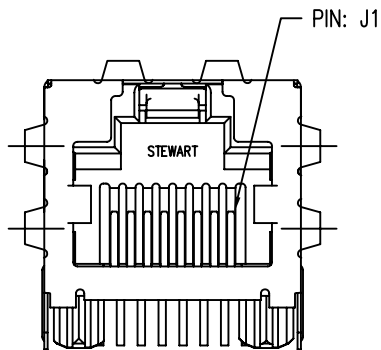
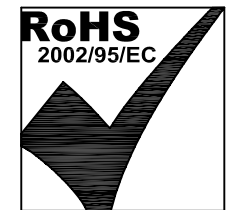
DRAWING NO.  
SI-53024-F

REV.  
05



P.C.B. RECOMMENDED HOLE LAYOUT  
SEEN FROM COMPONENT SIDE

ALL CENTERLINE DIMENSIONS ARE BASIC.



NOTES:

- CONNECTOR MATERIALS:  
HOUSING: THERMOPLASTIC UL94 V-0  
CONTACT/SHIELD: COPPER ALLOY  
SHIELD PLATING: NICKEL OR TIN  
CONTACT PLATING: SELECTIVE GOLD,  
50 MICRO-INCHES MIN. IN CONTACT AREA.
- PIN NOT ELECTRICALLY CONNECTED MAYBE OMITTED.  
SEE ELECTRICAL DRAWING FOR OMITTED PINS.
- TOLERANCES COMPLY WITH F.C.C. DIMENSION REQUIREMENTS.
- ALL TOLERANCES NOT OTHERWISE SPECIFIED TO BE  $\pm 0.005 [0.13]$
- WAVE SOLDER COMPATIBLE - PREHEAT 125°C/90SECS.

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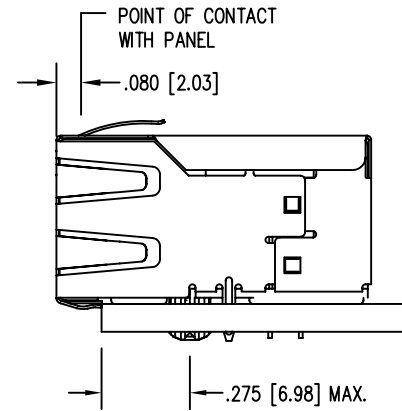
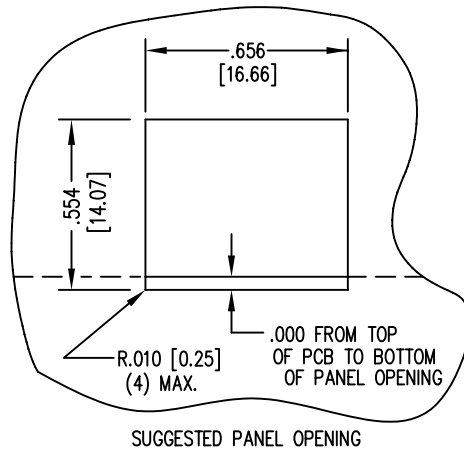
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SHEET  
3 OF 4

DRAWING NO.  
SI-53024-F

REV.  
07



1. THE SUGGESTED PANEL OPENING IS INTENDED TO GIVE THE USER THE ABILITY TO HAVE REASONABLE JACK / PANEL CLEARANCES YET MAINTAIN RELIABLE GROUNDING CAPABILITY.
2. ALL TOLERANCES NOT OTHERWISE SPECIFIED TO BE  $\pm .005$  [0.13]

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SHEET  
4 OF 4

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