DOCUMENT NUMBER AND REVISION

VL-PS-PDA320240D-02 REV. A

(PDA320240D-02)

DOCUMENT TITLE:

PRELIMINARY SPECIFICATION
OF
LCD MODULE TYPE

MODEL NUMBER: PDA320240D-02

DEPARTMENT	NAME	SIGNATURE	DATE
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DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2005.06.24	First Release. Based on a.) Test Specification: VL-TS-PDA320240D-02 REV. A 2005.06.10 b.) VL-QUA-012B, REV. W, 2004.03.20 According to VL-QUA-012B, LCD size is middle because Unit Per Laminate=6 which is in the range of 2pcs/Laminate to 6pcs /Laminate.	ZHANG YAN FANG	LIU ZHI QIANG

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VARITRONIX LIMITED

Preliminary Specification
of
LCD Module Type
PDA320240D-02

1. General Description

- 320 X 240 dots.
- FSTN Positive Black & White Transflective LCD Graphic Module.
- Viewing Angle: 6 O'clock direction.
- Driving scheme: 1/240 Duty, 1/13 bias.
- 'NOVATEK' NT7701 (TCP form) 160 Output LCD Segment/Common Drivers or equivalent.
- 'NOVATEK' NT7702 (TCP form) 240 Output LCD Segment/Common Drivers or equivalent.
- DC/DC Converters.
- White LED05 backlight.
- FFC connection.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1(a) and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	95.4(W) x 128.88(H) x 7.8 (D) (Include FFC & backlight terminals, exclude TAB)	mm
Viewing area	79.78(W) x 60.58(H)	mm
Active area	76.785(W) x 57.585(H)	mm
Display format	320 (H) dots x 240 (V) dots	-
Dot size	0.225(W) x 0.225(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.24(W) x 0.24(H)	mm
Overall Weight	TBD	gram

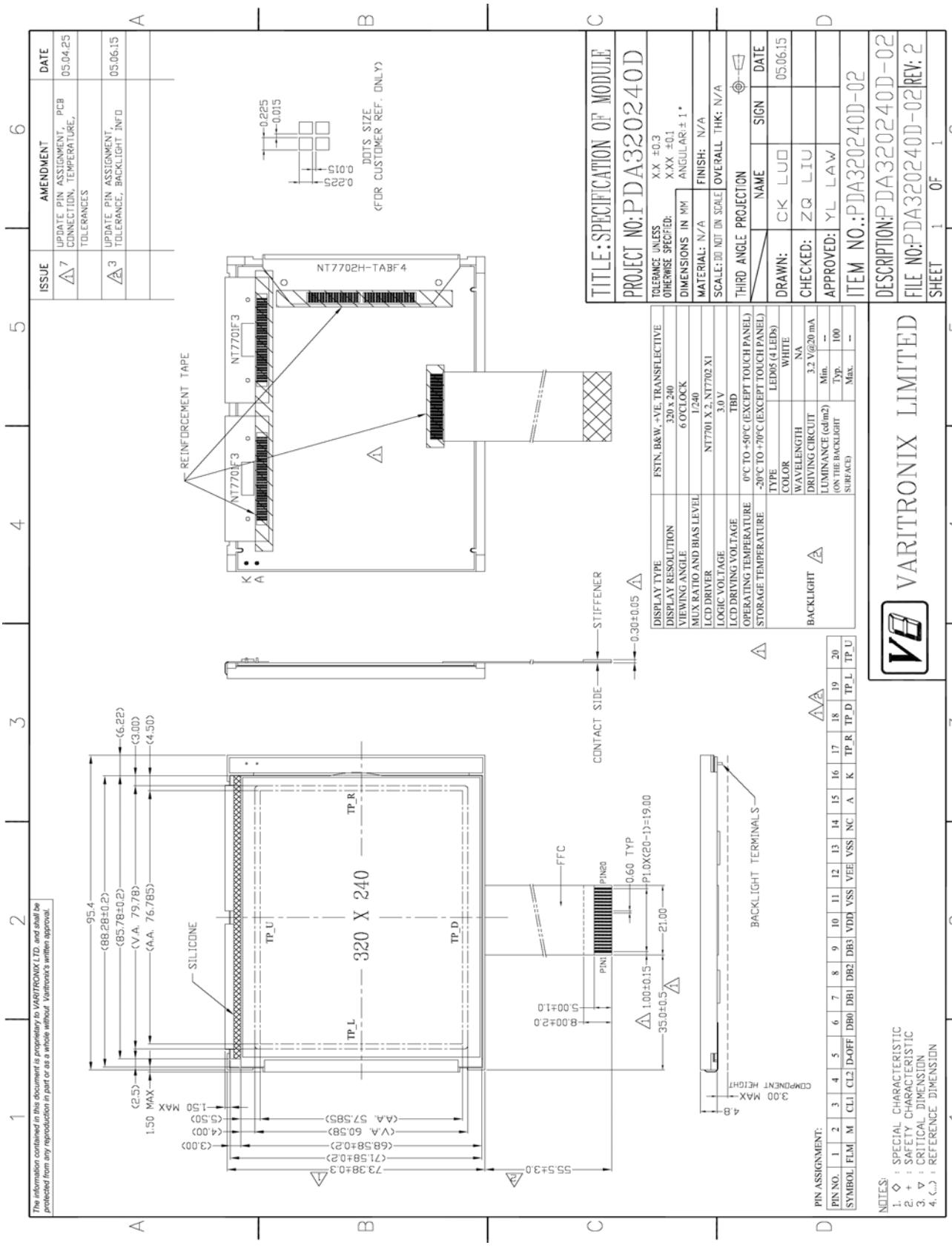

Figure 1(a): Module specification

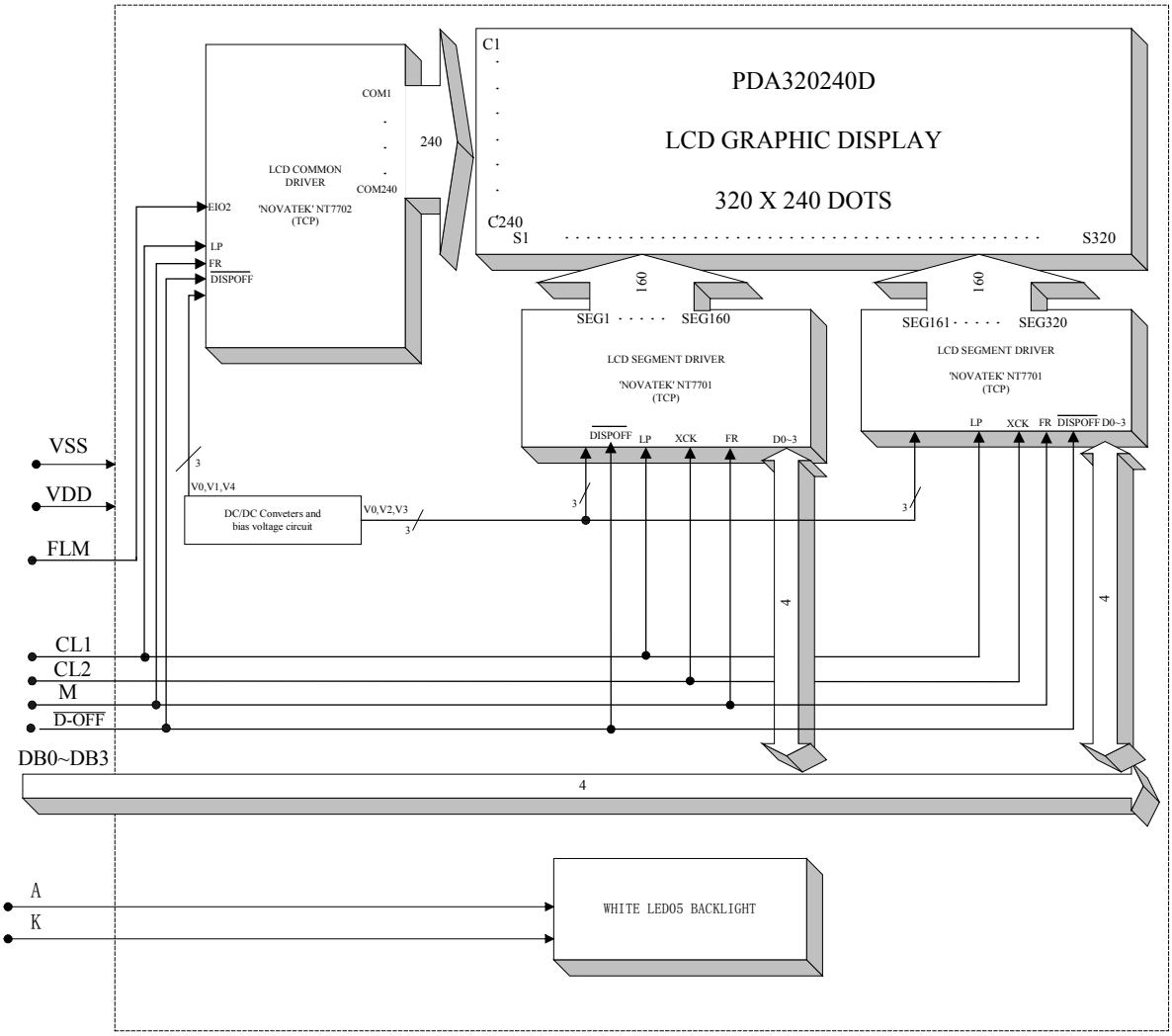

Figure 1(b): Block Diagram of the module.

3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings – for IC Only

Table 2

Parameter	Symbol	Min.	Max.	Unit
Supply voltage range (Logic)	VDD - VSS	-0.3	+7.0	V
Supply voltage (LCD)	V0	-0.3	+30.0	V
Input voltage range	VIN	-0.3	VDD+0.3	V

Note: 1.) The module may be destroyed if they are used beyond the absolute maximum ratings.
2.) All voltage values are referenced to VSS= 0V.

3.2 Environmental Conditions

Table 3

Item	Operating Temperature (Topr)		Storage Temperature (Tstg) (Note1)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature (Except Touch Panel)	0°C	+50°C	-20°C	+70°C	Dry
Humidity	90% max. RH for Ta ≤ 40°C				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100 g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note 1: Product cannot sustain in extreme storage conditions for a long time.

4. Electrical Specifications

4.1 Interface signals

Table 4: Pin description (LCD Driver)

Pin No.	Symbol	Description
1	FLM	Input/output for chip select or data of the shift register.
2	M	AC signal input for LCD driving waveform -The input signal is level-shifted from logic voltage level to the LCD driver voltage level, and it controls the LCD driver circuit -Normally, inputs a frame inversion signal. The LCD driver output pin's output voltage level can be set using the shift register output signal and the FR signal.
3	CL1	Latch pulse input/shift clock input for the shift register.
4	CL2	Display data shift clock input for segment mode.
5	$\overline{\text{D-OFF}}$	Control input for deselect output level.
6	DB0	Input pin for display data.
7	DB1	
8	DB2	
9	DB3	
10	VDD	Power supply for logic.
11	VSS	Ground (0V)
12	VEE *	Positive power supply for LCD driving voltage. *
13	VSS	Ground (0V)
14	NC	No connection
15	A	Anode of backlight
16	K	Cathode of backlight.
17	TP_R	RIGHT Input Position
18	TP_D	BOTTOM Input Position
19	TP_L	LEFT Input Position
20	TP_U	TOP Input Position

* This pin should be NC (No Connection) when Built-in DC/DC converter is used

4.2 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 3.0V±5%, VSS = 0V. Ta=25°C

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		2.85	3.0	3.15	V
Supply voltage (LCD) (Build-in)	VLCD	VDD=3.0V, Ta=25°C, Note 1	16.3	16.5	16.7	V
Input signal voltage	VIH	"High" level, Note 2	0.8 VDD	-	-	V
	VIL	"Low" level, Note 2	-	-	0.2 VDD	V
Supply Current (Logic & LCD)	IDD	Character mode, VDD = 3.0V. Ta=25°C, Note (1)	-	20	30	mA
		Checker board mode, VDD = 3.0V. Ta=25°C, Note (1)	-	30	45	mA
Supply voltage of White LED05 backlight	VLED	Forward current =20mA	3.0	3.2	3.4	V
Luminance (on the backlight surface)		Number of LED chips=1x4=4	70	100	-	cd/m^2

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Note 2: Apply to pins DB0~DB3 (or D0~D3), FLM (or EIO2), CL1 (or LP), CL2 (or XCK), DISPOFF M (or FR), and $\overline{\text{D-OFF}}$ (or $\overline{\text{DISPOFF}}$).

4.3 Timing Specifications

Refer to Fig. 2, Segment mode characteristics (NT7701)

At Ta = 0 °C to +50 °C, VDD = 3.0V±5%, VSS = 0V.

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	125	-		ns	tr, tf ≦ 11ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	51	-		ns	
Shift clock "L" pulse width	t_{WCKL}	51	-		ns	
Data setup time	t_{DS}	30	-		ns	
Data hole time	t_{DH}	40	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	51	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	51	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	51	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	51	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	36	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	78	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL = 15pF

Note

1. Take the cascade connection into consideration.
2. (t_{CK} - t_{WCKII} - t_{WCKL})/2 is the maximum in the case of high speed operation.

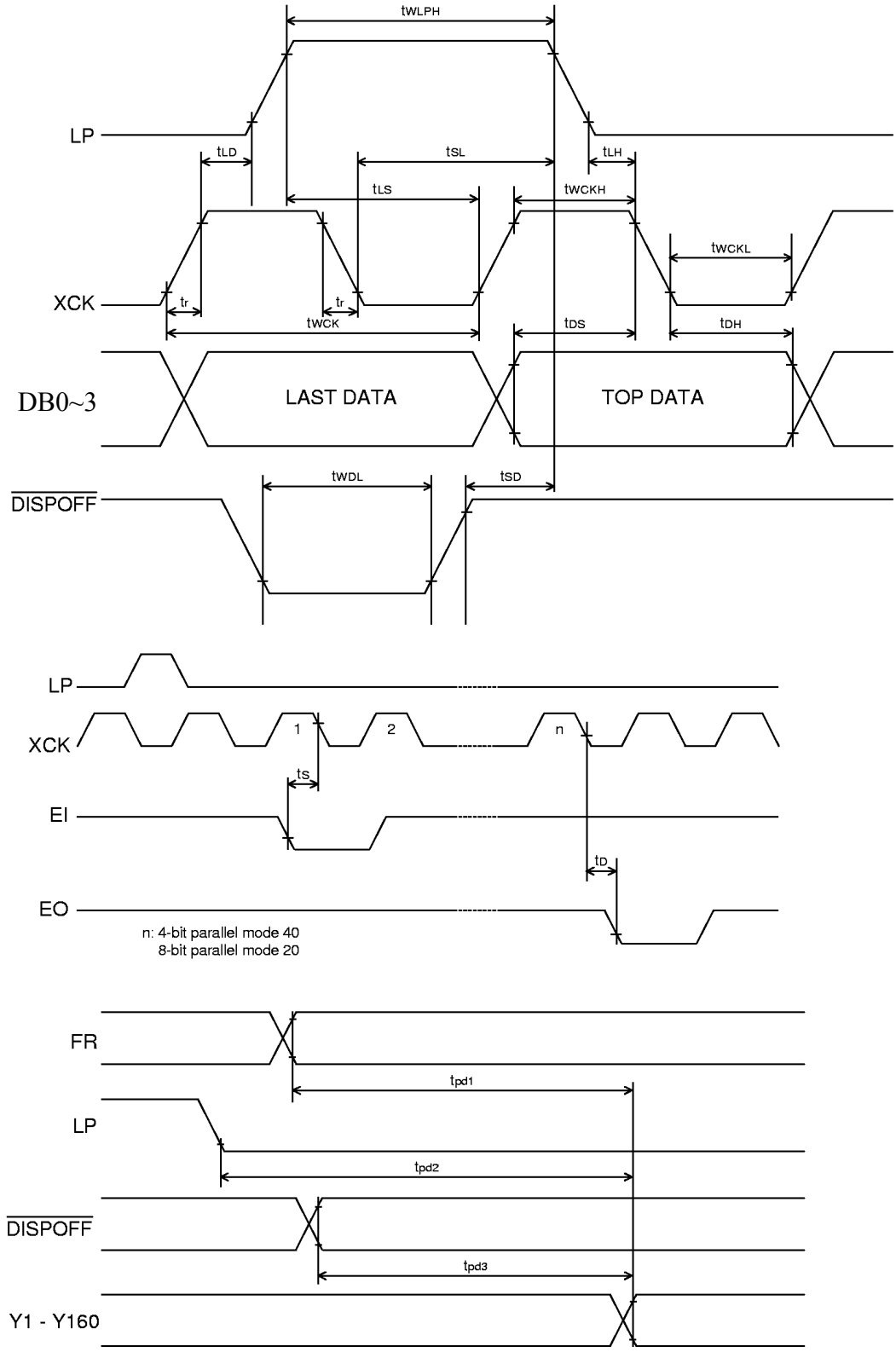

Figure 2: Timing waveform of the segment mode (NT7701)

Refer to Fig. 3, Common mode characteristics (NT7702).
At Ta = 0 °C to +50 °C, VDD = 3.0V±5%, VSS = 0V.

Table 7

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WLP}	250	-	-	ns	t_r, $t_f \leqq$ 20ns
Shift clock "H" pulse width	t_{WLPH}	15	-	-	ns	V_{DD} = +5.0V ± 10%
		30	-	-	ns	V_{DD} = +2.5 - +4.5V
Data setup time	t_{SU}	30	-	-	ns	
Data hole time	t_H	50	-	-	ns	
Input signal rise time	t_r		-	50	ns	
Input signal fall time	t_f		-	50	ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-	-	ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-	-	µs	
Output delay time (1)	t_{DL}	-	-	200	ns	C_L = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}	-	-	1.2	µs	C_L = 15pF
Output delay time (3)	t_{pd3}	-	-	1.2	µs	C_L = 15pF

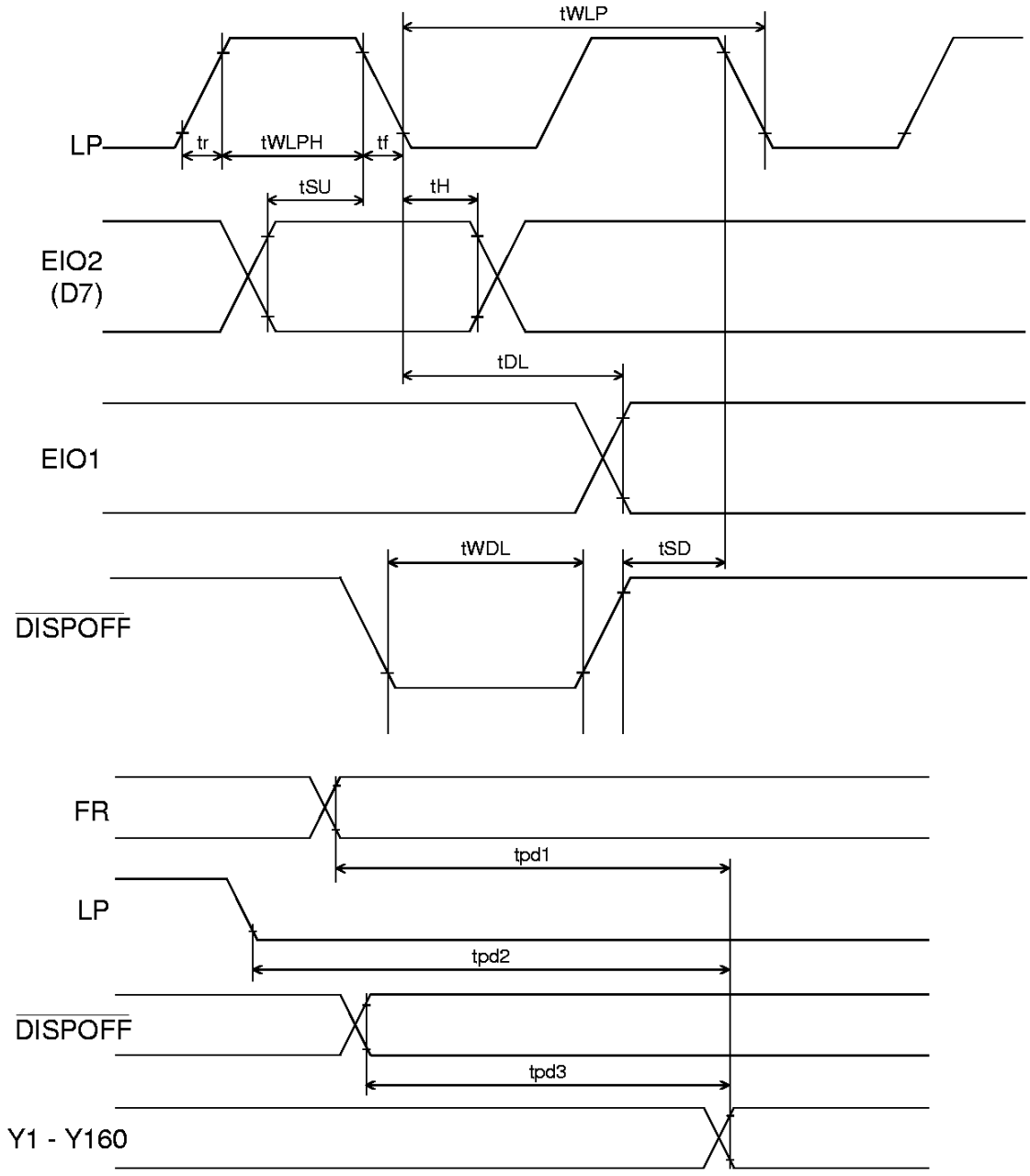

Figure 3: Timing waveform of the common mode (NT7702)

4.4 Precaution when Connecting and Disconnecting the Power

Be careful when connecting or disconnecting the power.
This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current, which may occur, if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating.
The details are as follows:

- When connecting the power supply, connect the LCD driver power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.

- We recommend that you connect a serial resistor (50-100 Ω) or fuse to the LCD driver power V0 of the system as a current limiting device. Also, set a suitable value of the resistor in consideration of LCD display grade.

  In addition, when connecting the logic power supply, the logic condition of this LSI inside is insecure. Therefore connect the LCD driver power supply after resetting the logic condition of this LSI inside on /DOFF function. After that, the /DOFF cancel the function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD driver output pins to level VSS on the /DOFF function. After that, disconnect the logic system power after disconnecting the LCD driver power.

  When connecting the power supply, follow the recommended sequence shown.

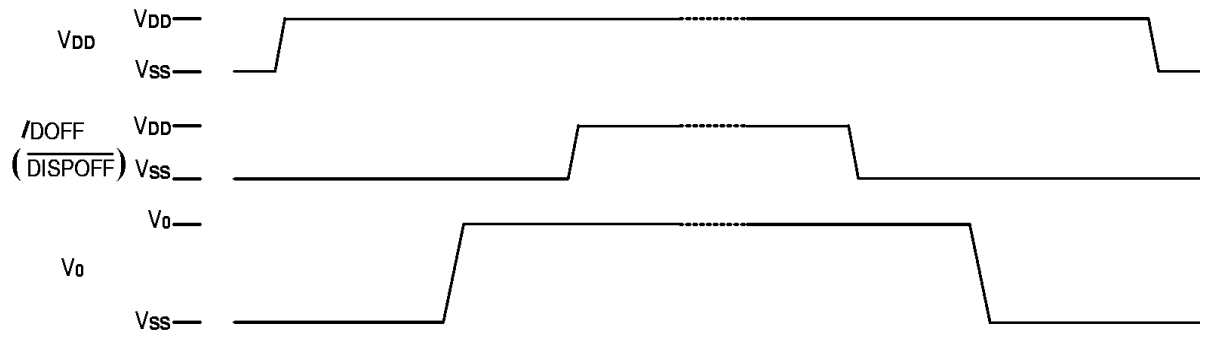

Figure 4: Power sequence

5. Remark

HANDLING LCD AND LCD MODULES

1. Liquid Crystal Display (LCD)

LCD is made up of glass, organic sealant, organic fluid and polymer based polarizers. The following precautions should be taken when handling:

(1) Keep the temperature within range for use and storage. Excessive temperature and humidity could cause polarization degredation, polarizer peel-off or bubble generation. When storage for a long period over 40° C is required, the relative humidity should be kept below 60%.
(2) Do not contact the exposed polarizers with anything harder than an HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin. Never scrub hard.
(3) Varitronix does not responsible for any polarizer defect after the protective film has been removed from the display
(4) Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or color fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.
(5) PETROLEUM BENZIN is recommended to remove adhesives used to attach front/rear polarizers and reflectors, while chemicals like acetone, toluene, ethanol and isopropyl alcohol will cause damage to the polarizer. Avoid oil and fats. Avoid lacquer and epoxies which might contain solvents and hardeners to cause electrode errosion. Some solvents will also soften the epoxy covering the DIL pins and thereby weakening the adhesion of the epoxy on glass. This will cause the exposed electrodes to erode electrochemically when operating in high humidity and condensing environment.
(6) Glass can be easily chipped or cracked from rough handling, especially at corners and edges.
(7) Do not drive LCD with DC voltage.
(8) When soldering DIL pins, avoid excessive heat and keep soldering temperature between 260°C to 300°C for no more than 5 seconds. Never use wave or reflow soldering.

2. Liquid Crystal Display Modules (MDL)

2.1 Mechanical Considerations

MDL's are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.
(1) Do not tamper in any way with the tabs on the metal frame.
(2) Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.
(3) Do not touch the elastomer connector (conductive rubber), especially when inserting an EL panel.
(4) When mounting a MDL make sure that the PCB is not under any stress such as bending or twisting. Elas / delicate and missing pixels could result from slight dislocation of any of the elements.
(5) Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.
(6) If FPCA need to be bent, please refer the suggested ben con duri FP(
(7) Sha trac

2.2 Static Electricity

MDL contains CMOS LSI's and the same precaution for such devices should apply, namely:

(1) The operator should be grounded whenever he comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any part of the human body.
(2) The modules should be kept in antistatic bags or other containers resistant to static for storage.
(3) Only properly grounded soldering irons should be used.
(4) If an electric screwdriver is used it should be well grounded and shielded from commutator sparks.
(5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.
(6) Since dry air is inducive to statics, a relative humidity of 50 - 60% is recommended.

2.3 Soldering

(1) Solder only to the I/O terminals.
(2) Use only soldering irons with proper grounding and no leakage.
(3) Soldering temperature is 280°C ± 10°C .
(4) Soldering time: 3 to 4 seconds.
(5) Use eutectic solder with resin flux fill.
(6) If flux is used. the LCD surface should be covered to avoid flux spatters. Flux residue should be removed afterwards.
(7) Use proper de-soldering methods (e.g. suction type desoldering irons) to remove lead wires from the I/O terminals when necessary. Do not repeat the soldering/ desoldering process more than three times as the pads and plated through holes may be damaged.

2.4 Label

Identification labels will be stuck on the module without obstructing the viewing area of display.

3. Operation

(1) The viewing angle can be adjusted by varying the LCD driving voltage Vo.
(2) Driving voltage should be kept within specified range, excess voltage shortens display life.
onse time increases with decrease in erature.
ay may turn black or dark Blue at temperatures its operational range; this is however not uctive and the display will return to normal once mperature falls back to range.
(3) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured". They will recover once the display is turned off.
(6) Condensation at terminals will cause malfunction and possible electrochemical reaction. Relative humidity of the environment should therefore be kept below 60%.
(7) Display performance may vary out of viewing area. If there is any special requirement on performance out of viewing area, please consult Varitronix.

4. Storage and Reliability

(1) LCD's should be kept in sealed polyethylene bags while MDL's should use antistatic ones. If properly sealed, there is no need for desiccant.
(2) Store in dark places and do not expose to sunlight or fluorescent light. Keep the temperature between 0°C and 35°C and the relative humidity low. Please consult VARITRONIX for other storage requirements.
(3) Water condensation will affect reliability performance of the display and is not allowed.
(4) Semi-conductor device on the display is sensitive to light and should be protected properly.
(5) Power up/down sequence.
a) Power Up: in general, LCD supply voltage, Vo must be supplied after logic voltage, VDD becomes steady. Please refer to related IC data sheet for details.
b) Power Down: in general, LCD supply voltage, Vo must be removed before logic voltage, VDD turns off. Please refer to related IC data sheet for details.

5. Safety

If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all times.

LIMITED WARRANTY

VARITRONIX LCDs and modules are not consumer products, but may be incorporated by VARITRONIX's customers into consumer products or components thereof. VARITRONIX does not warrant that its LCDs and components are fit for any such particular purpose.

1. The liability of VARITRONIX is limited to repair or replacement on the terms set forth below. VARITRONIX will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user.

   Unless otherwise agreed in writing between VARITRONIX and the customer, VARITRONIX will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with VARITRONIX LCD Acceptance Standards (copies available on request), for a period of one year from the date of shipment. Confirmation of such date shall be based on freight documents.

2. No warranty can be granted if any of the precautions stated in HANDLING LCD and LCD Modules above have been disregarded. Broken glass, scratches on polarizers, mechanical damages as well as defects that are caused by accelerated environmental tests are excluded from warranty.
3. In returning the LCD and Modules, they must be properly packaged and there should be detailed description of the failures or defects.

IMPORTANT NOTICE

The information presented in this document has been carefully checked and is believed to be accurate, however, no responsibility is assumed for inaccuracies. VARITRONIX reserves the right to make changes to any specifications without further notice for performance, reliability, production technique and other considerations, VARITRONIX does not assume any liability arising out of the application or use of products herein. Please see Limited Warranty in the previous section.

6. LCD Cosmetic Conditions

a.) Reference document follow VL-QUA-012B.

b.) LCD size of the product is middle.

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