24 MHz Rail-to-Rail Dual Amplifier

AD8646

FEATURES

Offset voltage: 2.5 mV maximum
Single-supply operation: 2.7 V to 5.5 V
Low noise: 8 nV/√Hz
Wide bandwidth: 24 MHz
Slew rate: 12 V/μs
Short-circuit output current: 150 mA
No phase reversal
Low input bias current: 1 pA
Low supply current: 2 mA maximum
Unity gain stable

APPLICATIONS

Battery-powered instruments
Multipole filters
ADC front ends
Sensors
Barcode scanners
ASIC input or output amplifiers
Audio amplifiers
Photodiode amplifiers
Datapath/mux/switch control

PIN CONFIGURATION

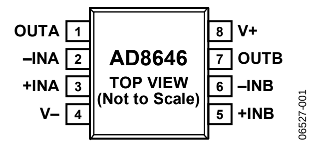

Figure 1.

GENERAL DESCRIPTION

The AD8646 is a dual, rail-to-rail, input and output, single-supply amplifier featuring low offset voltage, wide signal bandwidth, low input voltage, and low current noise.

The combination of 24 MHz bandwidth, low offset, low noise, and very low input bias current makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. AC applications benefit from the wide bandwidth and low distortion. This amplifier offers high output drive capability, which is excellent for audio line drivers and other low impedance applications.

Applications include portable and low powered instrumentation, audio amplification for portable devices, portable phone headsets, barcode scanners, and multipole filters. The ability to swing rail to rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in single-supply systems.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

8/07—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V, V_{CM} = V_{DD}/2, T_A = +25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 2.5 V		0.6	2.5	mV
		−40°C < T_A < +125°C			3.2	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1.8	7.5	μV/°C
Input Bias Current	I_B			0.3	1	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			550	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			250	pA
Input Voltage Range	V_{CM}		0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	67	84		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	104	116		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{OUT} = 1 mA	4.98	4.99		V
		−40°C < T_A < +125°C	4.90			
		I_{OUT} = 10 mA	4.85	4.92		V
		−40°C < T_A < +125°C	4.70			V
Output Voltage Low	V_{OL}	I_{OUT} = 1 mA		8.4	20	mV
		−40°C < T_A < +125°C			40	mV
		I_{OUT} = 10 mA		78	145	mV
		−40°C < T_A < +125°C			200	mV
Output Current	I_{OUT}	Short circuit		±120		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, A_V = 1		5		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.7 V to 5.0 V	63	80		dB
Supply Current per Amplifier	I_{SY}			1.5	1.9	mA
		−40°C < T_A < +125°C			2.25	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		11		V/μs
Gain Bandwidth Product	GBP			27		MHz
Phase Margin	$Ø_m$			77		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	0.1 Hz to 10 Hz		2.3		μV
Voltage Noise Density	e_n	f = 1 kHz		8		nV/√Hz
		f = 10 kHz		6		nV/√Hz
Channel Separation	CS	f = 10 kHz		−129		dB
		f = 100 kHz		−119		dB
Total Harmonic Distortion Plus Noise	THD+N	V p-p = 0.1 V, R_L = 600 Ω, f = 25 kHz, T_A = 25°C				
		A_V = +1		0.010		%
		A_V = −10		0.021		%

V_{DD} = 2.7 V, V_{CM} = V_{DD}/2, T_A = +25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 1.35 V		0.6	2.5	mV
		−40°C < T_A < +125°C			3.2	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1.5	7.0	µV/°C
Input Bias Current	I_B			0.2	1	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			550	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			250	pA
Input Voltage Range	V_{CM}		0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	62	79		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 2.2 V	95	107		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{OUT} = 1 mA	2.65	2.68		V
		−40°C < T_A < +125°C	2.60			V
Output Voltage Low	V_{OL}	I_{OUT} = 1 mA		11	25	mV
		−40°C < T_A < +125°C			30	mV
Output Current	I_{OUT}	Short circuit		±63		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, A_V = 1		5		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.7 V to 5.0 V	63	80		dB
Supply Current per Amplifier	I_{SY}			1.6	1.9	mA
		−40°C < T_A < +125°C			2.25	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		11		V/µs
		R_L = 10 kΩ				
Gain Bandwidth Product	GBP			26		MHz
Phase Margin	$Ø_m$			53		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	0.1 Hz to 10 Hz		2.3		µV
Voltage Noise Density	e_n	f = 1 kHz		8		nV/√Hz
		f = 10 kHz		6		nV/√Hz
Channel Separation	CS	f = 10 kHz		−129		dB
		f = 100 kHz		−121		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_{DD}
Differential Input Voltage	±3 V
Output Short Circuit to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering 60 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

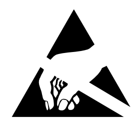
THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	121	43	°C/W
8-Lead MSOP	210	45	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

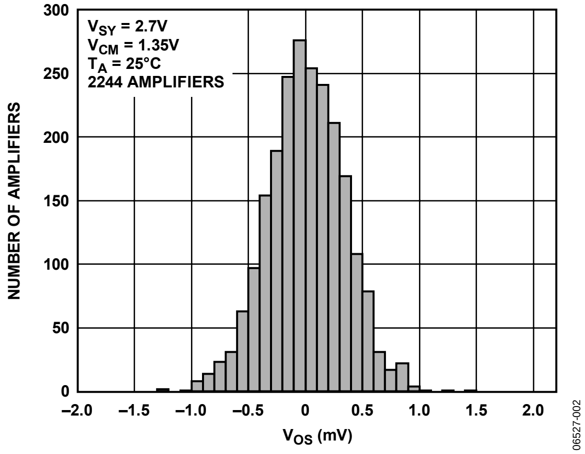


Figure 2. Input Offset Voltage Distribution

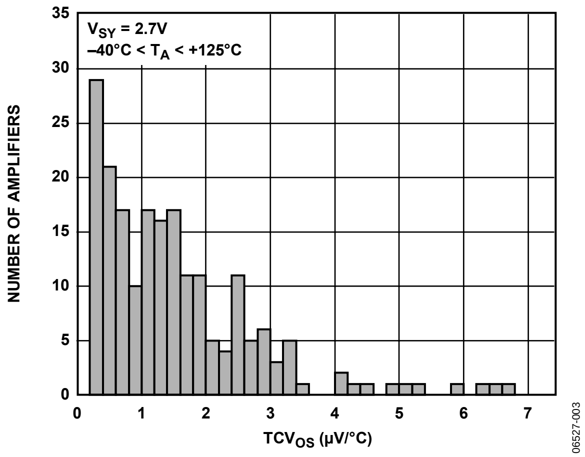


Figure 3. V_{OS} Drift (TCV_{OS}) Distribution

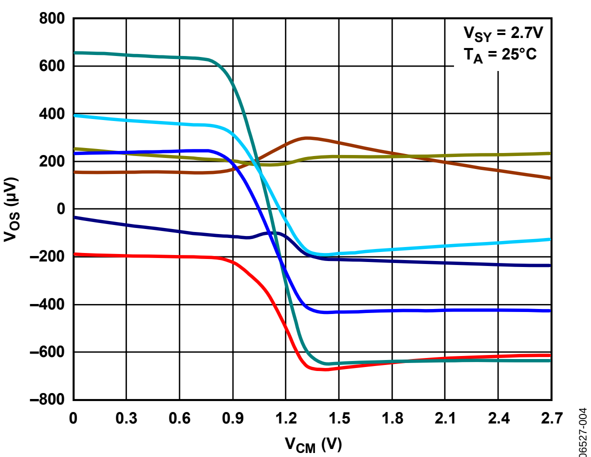


Figure 4. Input Offset Voltage vs. Input Common-Mode Voltage

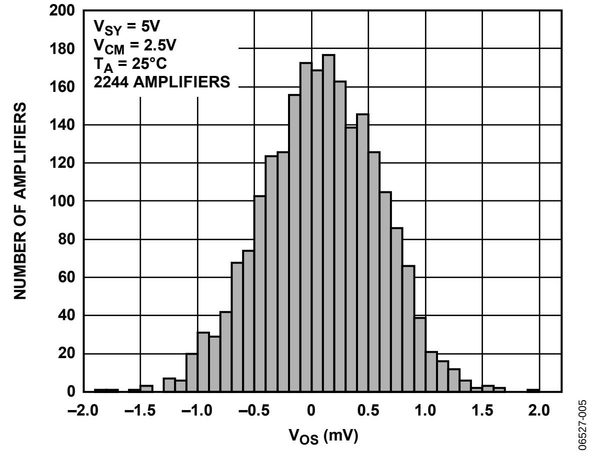


Figure 5. Input Offset Voltage Distribution

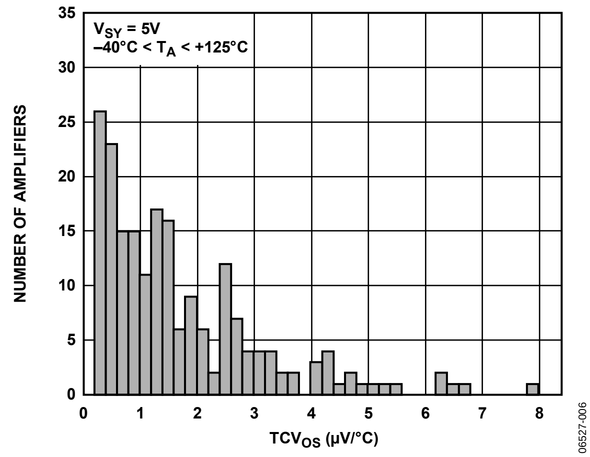


Figure 6. V_{OS} Drift (TCV_{OS}) Distribution

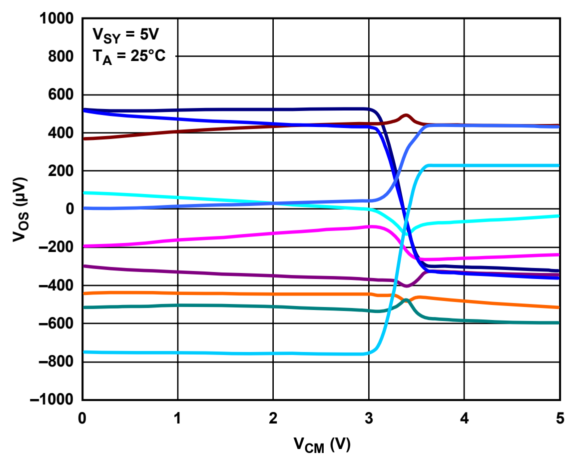


Figure 7. Input Offset Voltage vs. Input Common-Mode Voltage

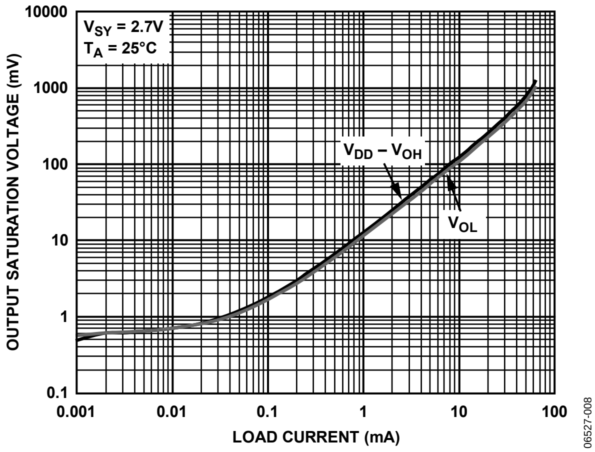


Figure 8. Output Saturation Voltage vs. Load Current

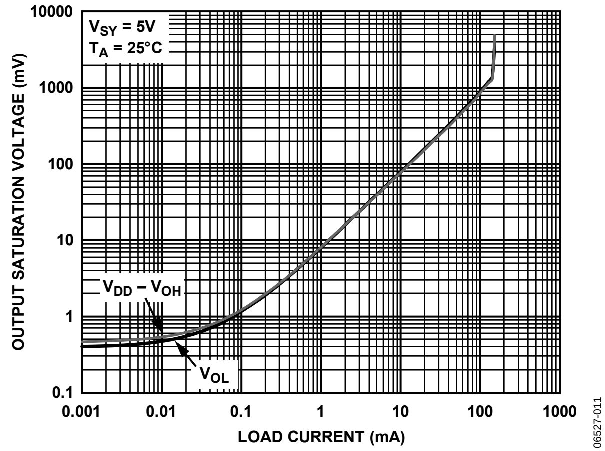


Figure 11. Output Saturation Voltage vs. Load Current

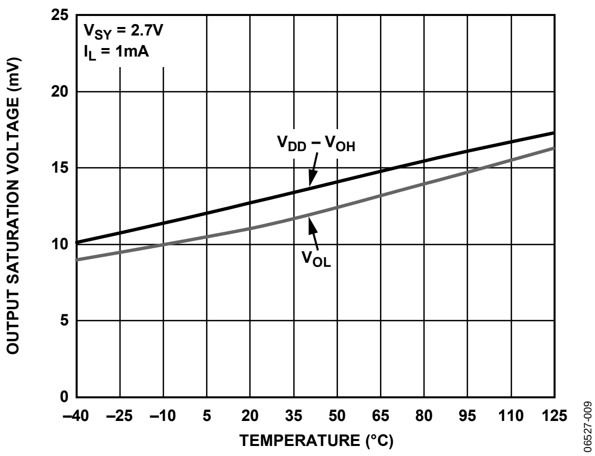


Figure 9. Output Saturation Voltage vs. Temperature

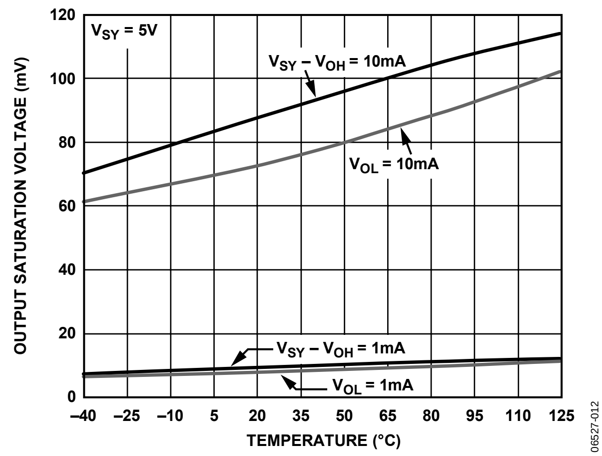


Figure 12. Output Saturation Voltage vs. Temperature

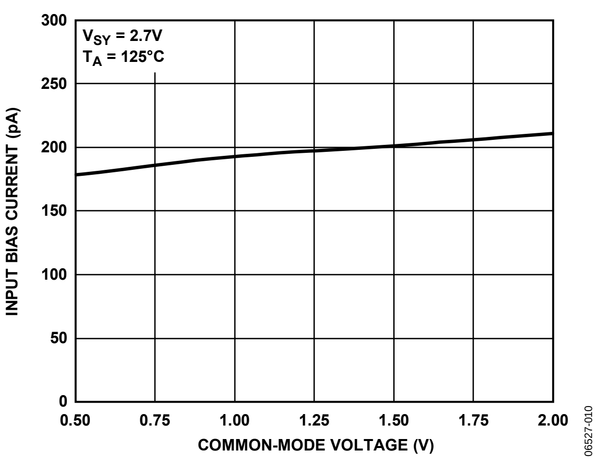


Figure 10. Input Bias Current vs. Common-Mode Voltage

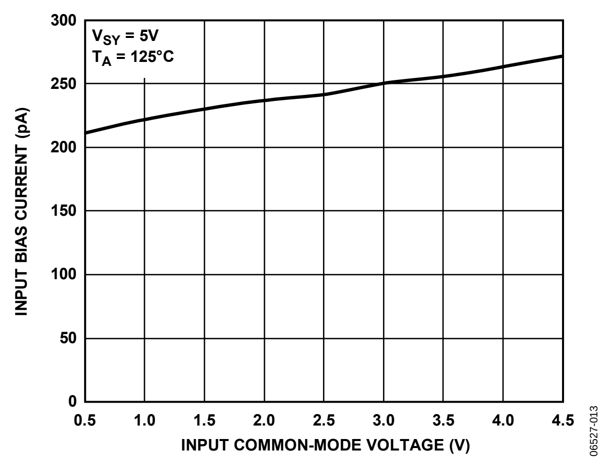


Figure 13. Input Bias Current vs. Common-Mode Voltage

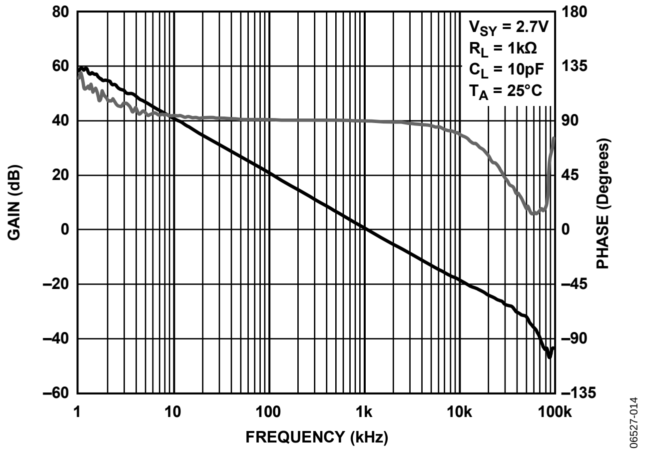


Figure 14. Open-Loop Gain and Phase vs. Frequency

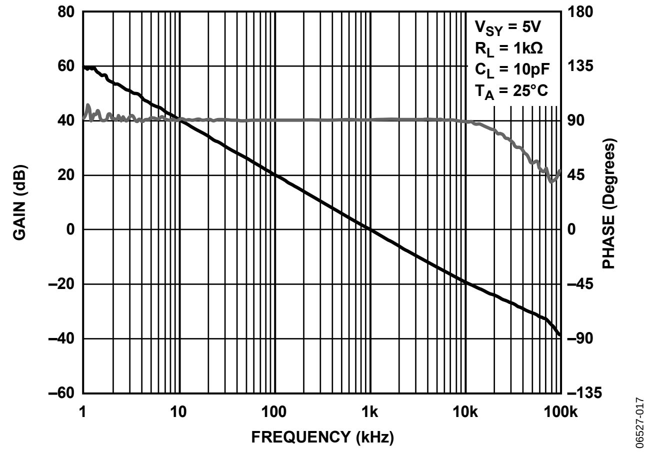


Figure 17. Open-Loop Gain and Phase vs. Frequency

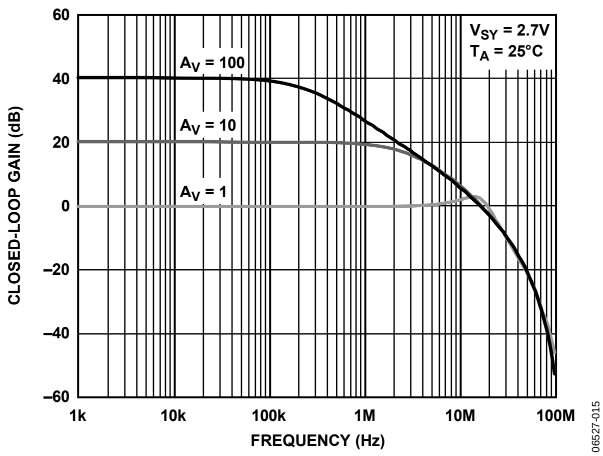


Figure 15. Closed-Loop Gain vs. Frequency

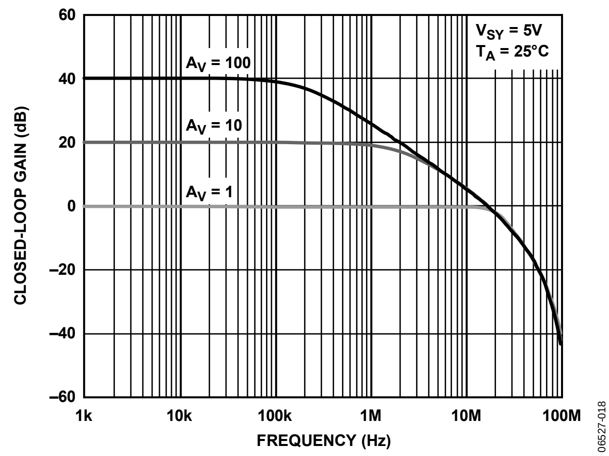


Figure 18. Closed-Loop Gain vs. Frequency

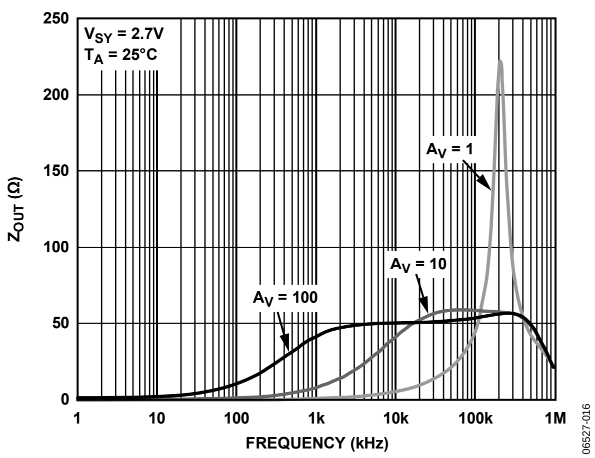


Figure 16. Z_{OUT} vs. Frequency

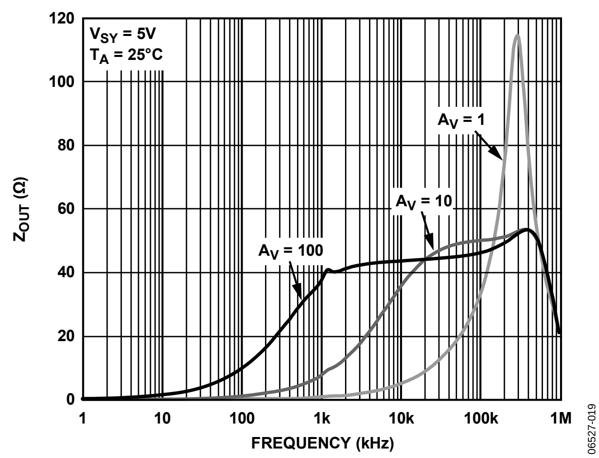


Figure 19. Z_{OUT} vs. Frequency

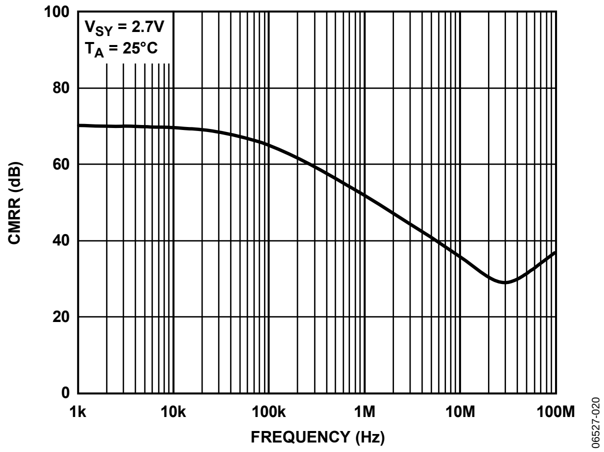


Figure 20. CMRR vs. Frequency

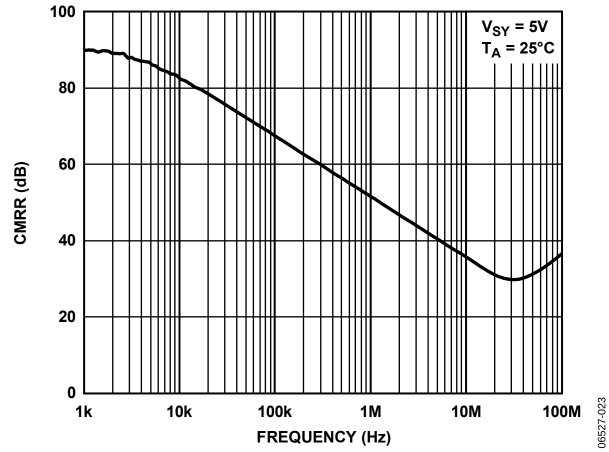


Figure 23. CMRR vs. Frequency

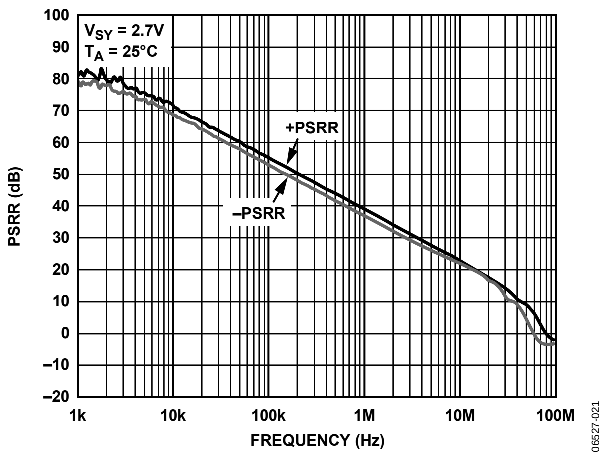


Figure 21. PSRR vs. Frequency

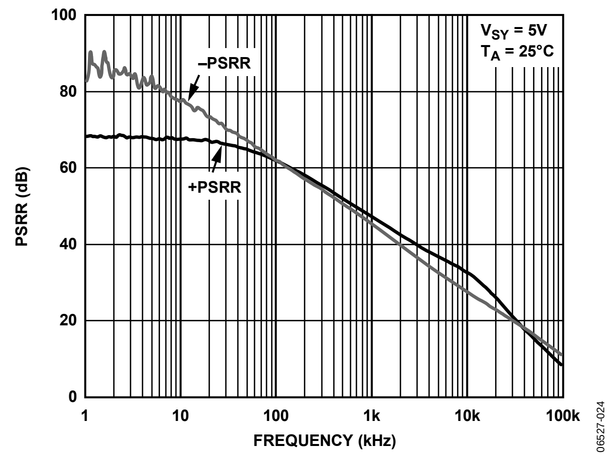


Figure 24. PSRR vs. Frequency

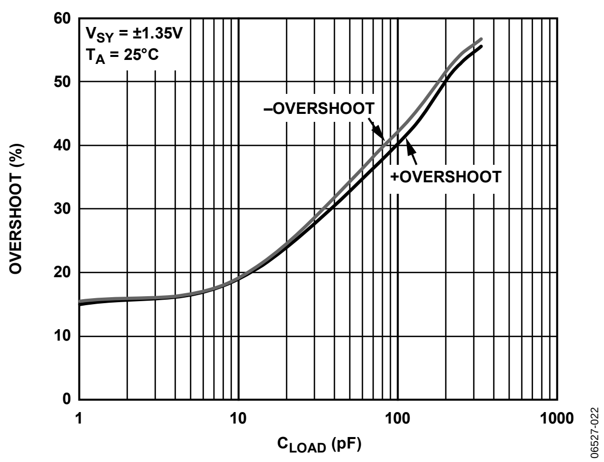


Figure 22. Small Signal Overshoot vs. Load Capacitance

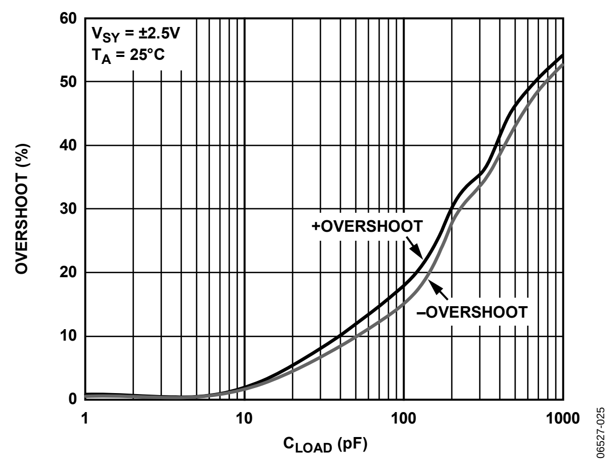


Figure 25. Small Signal Overshoot vs. Load Capacitance

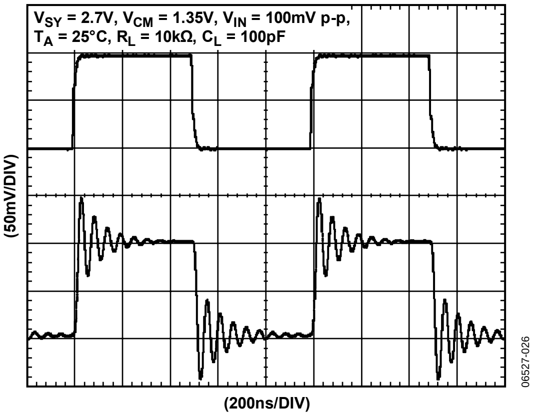


Figure 26. 2.7 V Small Signal Transient Response

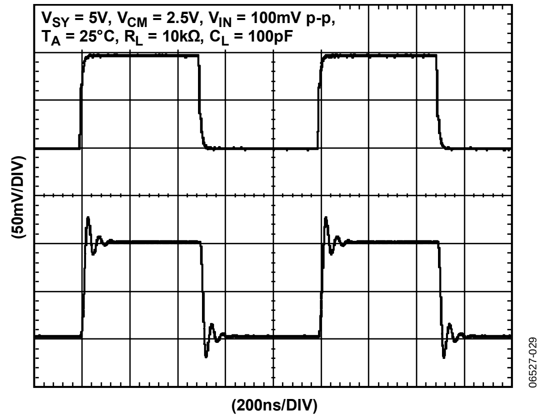


Figure 29. 5 V Small Signal Transient Response

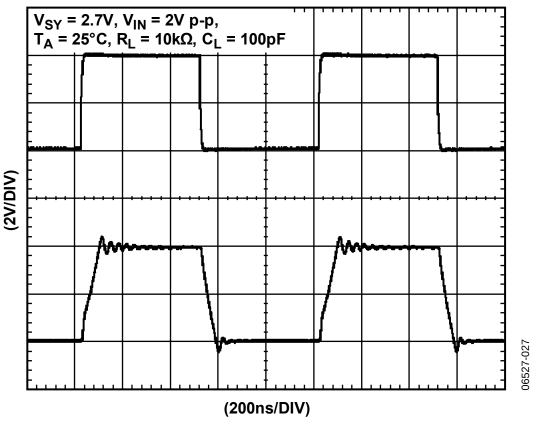


Figure 27. 2.7 V Large Signal Transient Response

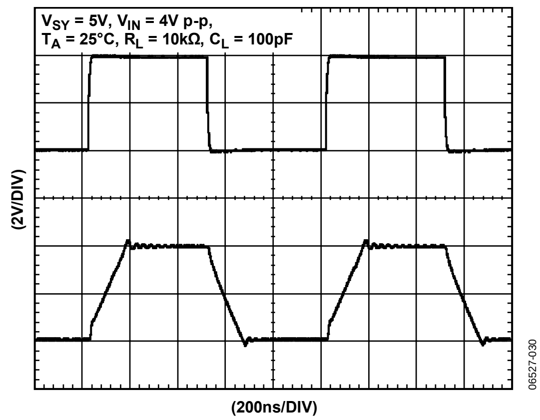


Figure 30. 5 V Large Signal Transient Response

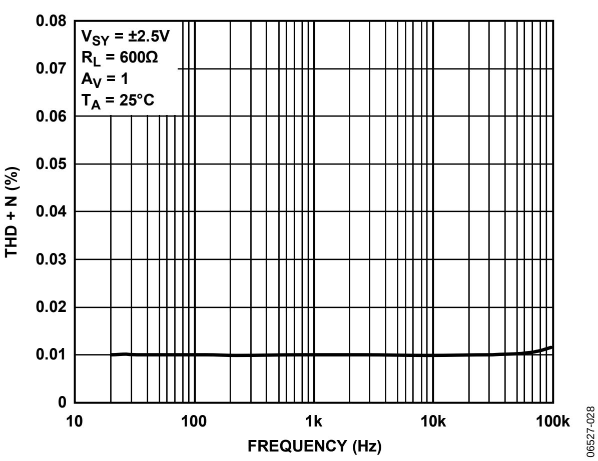


Figure 28. THD + Noise vs. Frequency

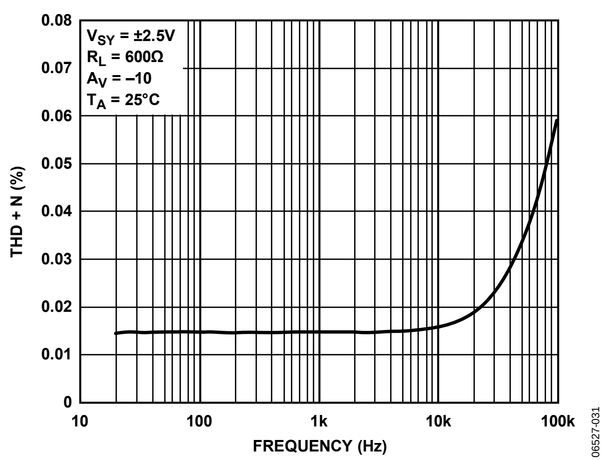


Figure 31. THD + Noise vs. Frequency

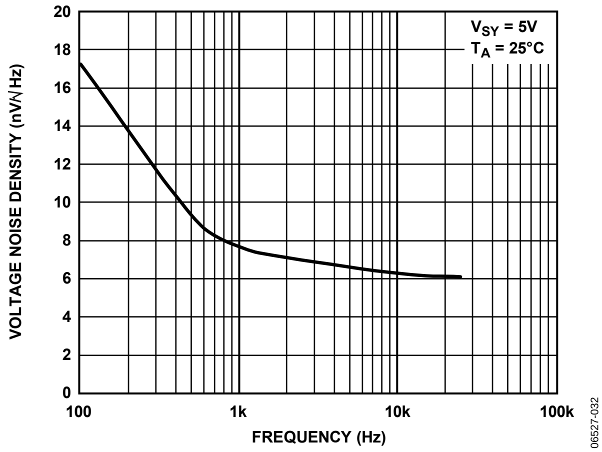


Figure 32. Voltage Noise Density vs. Frequency

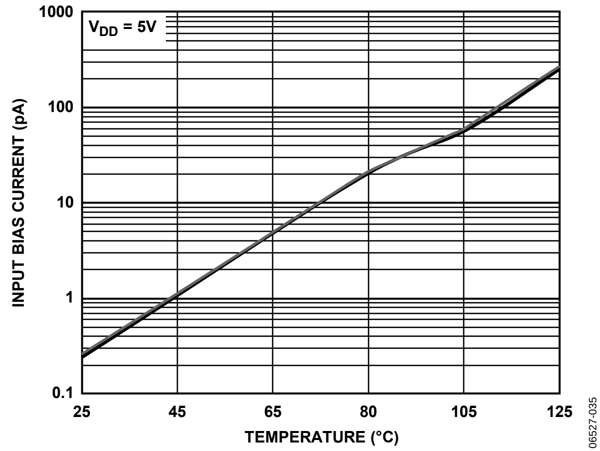


Figure 35. Input Bias Current vs. Temperature

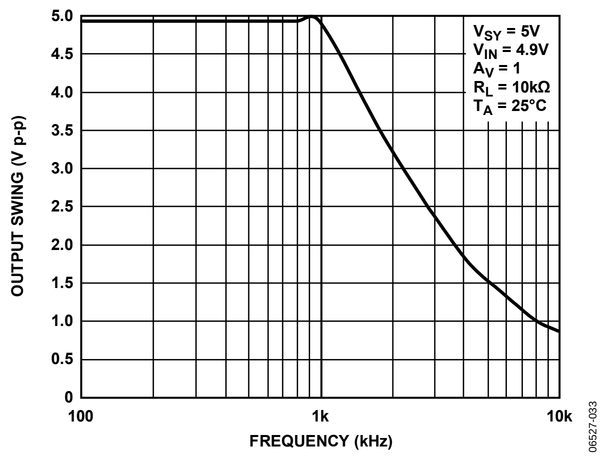


Figure 33. Maximum Output Swing vs. Frequency

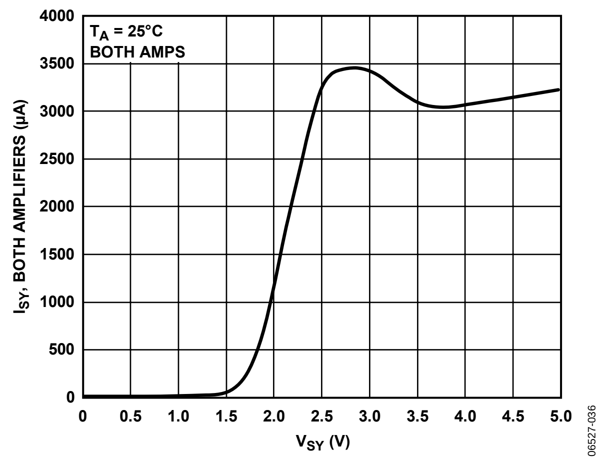


Figure 36. Supply Current vs. Supply Voltage

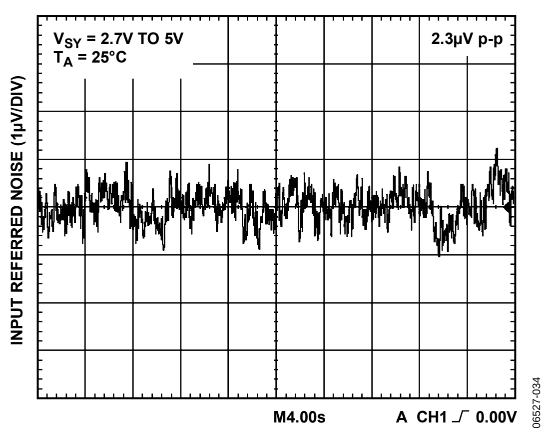


Figure 34. 0.1 Hz to 10 Hz Voltage Noise

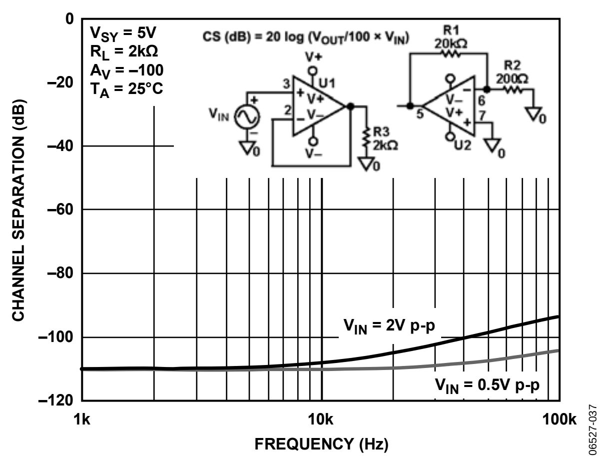


Figure 37. Channel Separation

OUTLINE DIMENSIONS

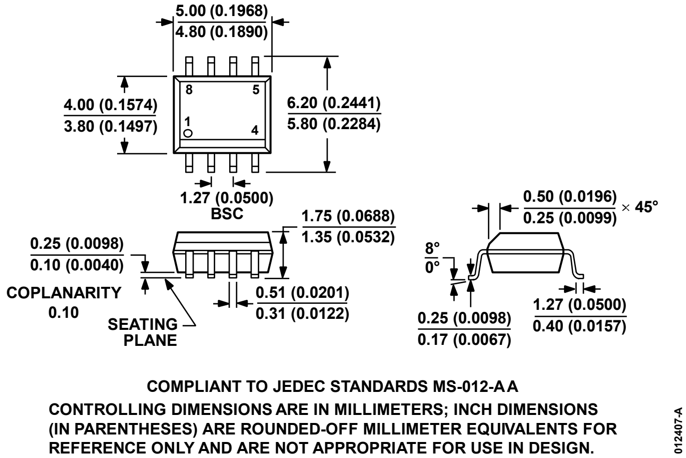


Figure 38. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

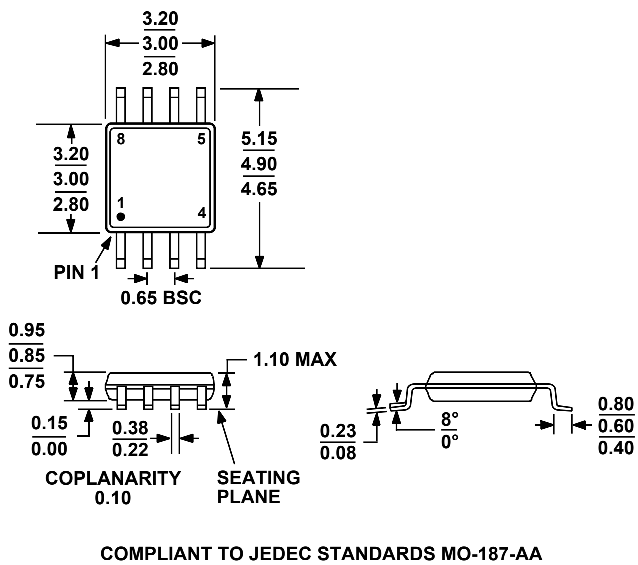


Figure 39. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8646ARZ[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8646ARZ-REEL[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8646ARZ-REEL7[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8646ARMZ-R2[1]	–40°C to +125°C	8-Lead MSOP	RM-8	A1V
AD8646ARMZ-REEL[1]	–40°C to +125°C	8-Lead MSOP	RM-8	A1V

[1] Z = RoHS Compliant Part.

D06527-0-8/07(0)