= Target Spec =

AK4703

AV SCART switch

GENERAL DESCRIPTION

The AK4703 offers the ideal features for digital set-top-box systems. The AK4703 includes the audio switches, video switches, video filters, etc. designed primarily for digital set-top-box systems. The AK4703 is offered in a space saving 64-pin LQFP package.

FEATURES

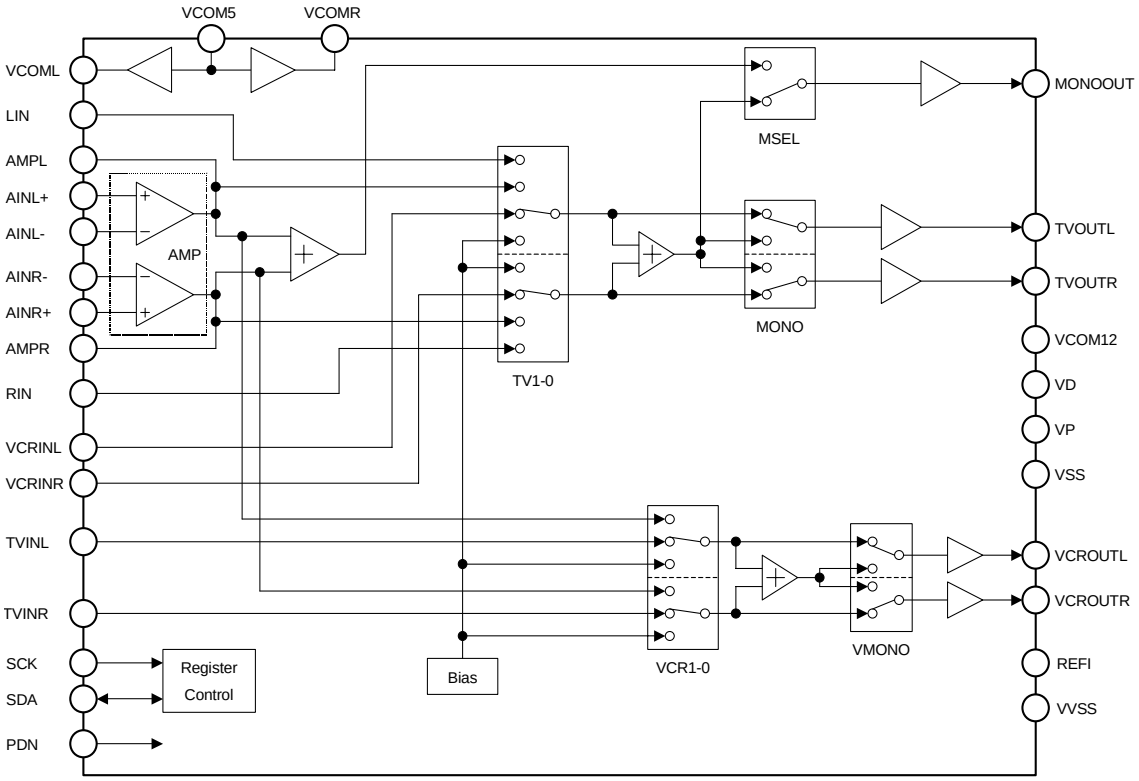
Analog switches for SCART
- **Audio section**
  - ☐ **THD+N: –86dB (@2Vrms)**
  - ☐ **Dynamic Range: 96dB (@2Vrms)**
  - ☐ **Six Analog Inputs**
    - **Full Differential Stereo Input for Decoder DAC**
    - **Two Stereo Input (TV & VCR SCART)**
  - ☐ **Five Analog Outputs**
    - **Two Stereo Outputs (TV & VCR SCART)**
    - **One Mono Output (Modulator)**
  - ☐ **Pop Noise Free Circuit for Power on/off**
- **Video section**
  - ☐ **Integrated LPF: –35dB@27MHz**
  - ☐ **75ohm driver**
  - ☐ **6dB Gain for Outputs**
  - ☐ **Four CVBS/Y inputs (ENCx2, TV, VCR)**
    Three CVBS/Y outputs (RF, TV, VCR)
  - ☐ **Three R/C inputs (ENCx2, VCR), Two R/C output (TV, VCR)**
  - ☐ **Bi-directional control for VCR-Chroma/Red**
  - ☐ **Two G and B inputs (ENC, VCR), One G and B outputs (TV)**
  - ☐ **TV/VCR input monitor**
- **Loop-through Mode for standby**
- **Auto-Startup Mode for power saving**

SCART pin#TBD(Fast Blanking), pin#TBD(Slow Blanking) Control

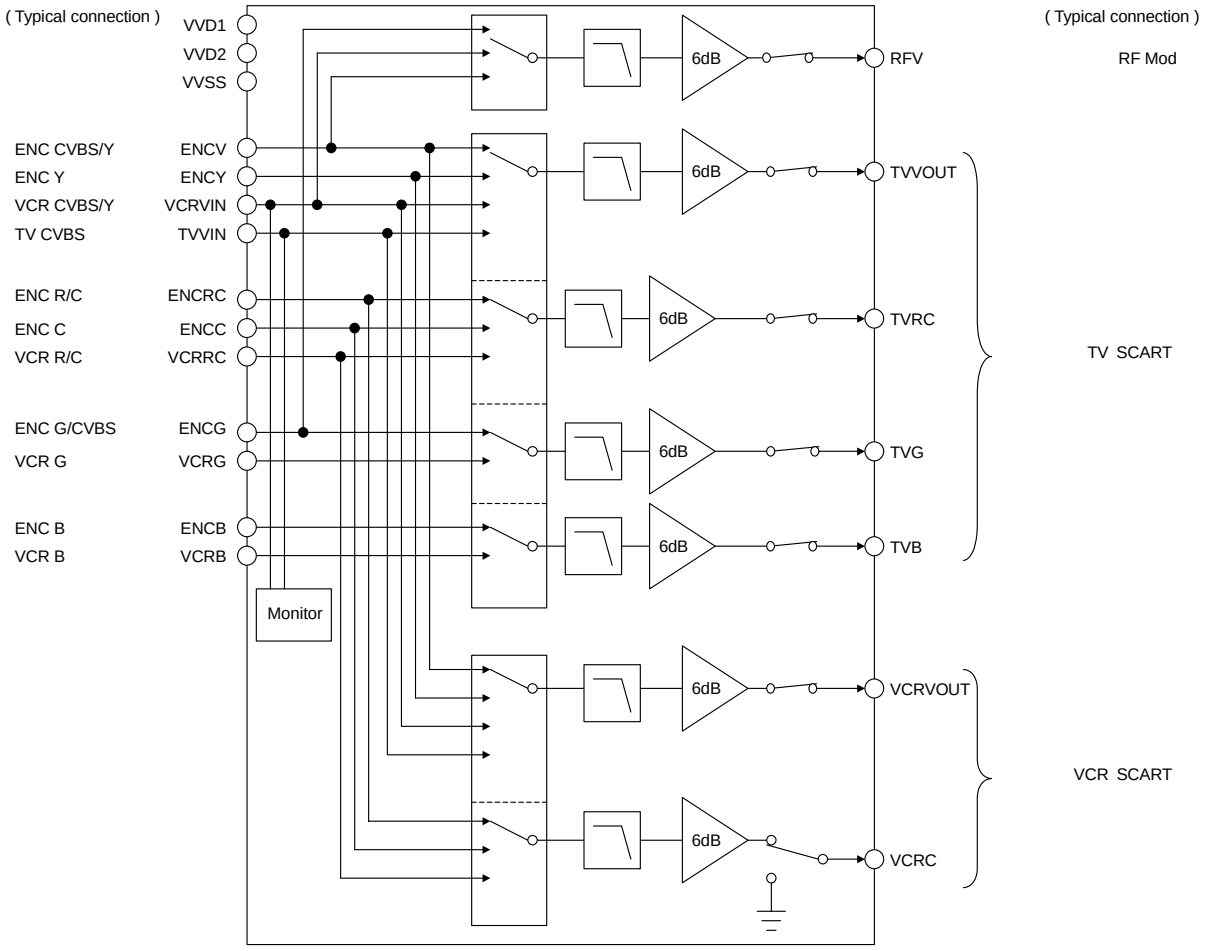
Power supply
- ☐ **5V+/–5% and 12V+/–5%**
- ☐ **Low Power Dissipation / Low Power Standby Mode**

Package
- ☐ **64pin LQFP**

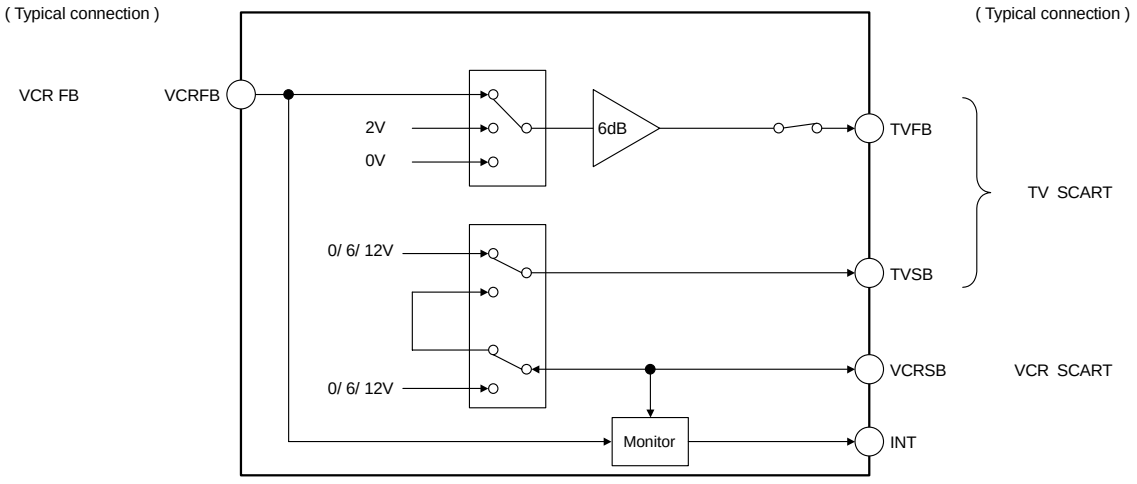
■ Block Diagram



Audio Block



Video Block



Video Blanking Block

■ Ordering Guide

AK4703VQ	–10 ~ +70°C	64pin LQFP (0.5mm pitch)

■ Pin Layout

TBD

PIN/FUNCTION (TBD)

No.	Pin Name	I/O	Function
1	VCRC	O	Chrominance Output Pin for VCR
2	VVSS	-	Video Ground Pin, 0V
3	TVVOUT	O	Composite/Luminance Output Pin for TV
4	VVD2	-	Video Power Supply Pin #2, 5V Normally connected to VVSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
5	TVRC	O	Red/Chrominance Output Pin for TV
6	TVG	O	Green Output Pin for TV
7	TVB	O	Blue Output Pin for TV
8	VVD1	-	Video Power Supply Pin #1, 5V Normally connected to VVSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
9	ENCB	I	Blue Input Pin for Encoder
10	ENCG	I	Green Input Pin for Encoder
11	ENCRC	I	Red/Chrominance Input Pin1 for Encoder
12	ENCC	I	Chrominance Input Pin2 for Encoder
13	ENCV	I	Composite/Luminance Input Pin1 for Encoder
14	ENCY	I	Composite/Luminance Input Pin2 for Encoder
15	TVVIN	I	Composite/Luminance Input Pin for TV
16	VCRVIN	I	Composite/Luminance Input Pin for VCR
17	VCRFB	I	Fast Blanking Input Pin for VCR
18	VCRRC	I	Red/Chrominance Input Pin for VCR
19	VCRG	I	Green Input Pin for VCR
20	VCRB	I	Blue Input Pin for VCR
21	INT	O	Interrupt Pin for Video Blanking
22	VCRSB	I/O	Slow Blanking Input/Output Pin for VCR
23	TVSB	O	Slow Blanking Output Pin for TV
24	VCRINR	I	Rch VCR Audio Input Pin
25	VCRINL	I	Lch VCR Audio Input Pin
26	TVINR	I	Rch TV Audio Input Pin
27	TVINL	I	Lch TV Audio Input Pin
28	TBD		
29	VCROUTR	O	Rch Analog Output Pin1
30	VCROUTL	O	Lch Analog Output Pin1
31	TVOUTR	O	Rch Analog Output Pin2
32	TVOUTL	O	Lch Analog Output Pin2

Pin layout is TBD.

PIN/FUNCTION (TBD, Continued)

No.	Pin Name	I/O	Function
33	VSS	-	Ground Pin, 0V
34	VD	-	Power Supply Pin, 5V Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
35	LIN	I	Lch Input Pin
36	AMPL	O	Lch Feed back Resistor Output Pin
37	AINL+	I	Lch Positive Analog Input Pin
38	AINL–	I	Lch Negative Analog Input Pin
39	RIN	I	Rch Input Pin
40	AMPR	O	Rch Feed back Resistor Output Pin
41	AINR+	I	Rch Positive Analog Input Pin
42	AINR–	I	Rch Negative Analog Input Pin
43	SCL	I	Control Data Clock Pin
44	SDA	I/O	Control Data Pin
45	PDN	I	Power-Down Mode Pin When at “L”, the AK4703 is in the power-down mode and is held in reset. The AK4703 should always be reset upon power-up.
46	RFV	O	Composite Output Pin for RF modulator
47	VCRVOUT	O	Composite/Luminance Output Pin for VCR
48	TVFB	O	Fast Blanking Output Pin for TV
49	MONOOUT	O	MONO Analog Output Pin
50	VP	-	Power Supply Pin, 12V Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
51	VCOM5	O	Common Voltage Pin Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
52	VCOM12	O	Audio Common Voltage Pin Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap. The caps affect the settling time of audio bias level.
53	VCOMO	O	Common Voltage Output Pin
54	REFI	I	TBD
55	TBD		
56	TBD		
57	TBD		
58	TBD		
59	TBD		
60	TBD		
61	TBD		
62	TBD		
63	TBD		
64	TBD		

Note: All input pins should not be left floating.

Pin layout is TBD.

ABSOLUTE MAXIMUM RATINGS

(VSS = VVSS = 0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VD	–0.3	6.0	V
	VVD1	–0.3	6.0	V
	VVD2	–0.3	6.0	V
	VP	–0.3	14	V
	|VSS – VVSS| (Note 2)	-	0.3	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage	VIND	–0.3	VD+0.3	V
Video Input Voltage	VINV	–0.3	VVD1+0.3	V
Audio Input Voltage (except LIN, RIN, AINL+/–, AINR+/– pins)	VINA	–0.3	VP+0.3	V
Audio Input Voltage (except LIN, RIN, AINL+/–, AINR+/– pins)	VINA	–0.3	VD+0.3	V
Ambient Operating Temperature	Ta	–10	70	°C
Storage Temperature	Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. VSS and VVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS = VVSS = 0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VD	4.75	5.0	5.25	V
	VVD1=VVD2	4.75	5.0	5.25	V
	VP	11.4	12	12.6	V

Note 3. Analog output voltage scales with the voltage of VD.
AOUT (typ@0dB) = 2Vrms × VD/5.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C; VP = 12V, VD = 5V; VVD1 = VVD2 = 5V)

Power Supplies	min	typ	max	Units
Power Supply Current				
Normal Operation (PDN = "H") (Note 4)				
VD		TBD	TBD	mA
VVD1+VVD2		TBD	TBD	mA
VP		TBD	TBD	mA
Power-Down Mode (PDN = "L") (Note 5)				
VD		10	100	μA
VVD1+VVD2		10	100	μA
VP		10	100	μA

Note 4. STBY bit = "L", All video outputs active. No signal, no load for A/V switches.
Note 5. All digital inputs are held at VD or VSS.

DIGITAL CHARACTERISTICS

(Ta = 25°C; VD = 4.75 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.0	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
Low-Level Output Voltage (SDA pin: Iout= 3mA, INT pin: Iout= 1mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

ANALOG CHARACTERISTICS (AUDIO)

(Ta = 25°C; VP = 12V, VD = 5V; VVD1 = VVD2 = 5V; Signal Frequency = 1kHz; Measurement frequency = 20Hz ~ 20kHz; R_L ≥4.5kΩ; 0dB=2Vrms output; unless otherwise specified)

Parameter	min	typ	max	Units
Analog Input: (TVINL/TVINR/VCRINL/VCRINR pins)				
Analog Input Characteristics				
Input Voltage			2	Vrms
Input Resistance	100	150	-	kΩ
Analog Input: (LIN/RIN pins)				
Analog Input Characteristics				
Input Voltage			1	Vrms
Input Resistance	40	60	-	kΩ
Stereo/Mono Output: (TVOUTL/TVOUTR/VCROUTL/VCROUTR/MONOOUT pins) (Note 6)				
Analog Output Characteristics				
THD+N (at 2Vrms output) (Note 7)		–86	–80	dB
Dynamic Range (–60dB Output, A-weighted) (Note 7)	92	96		dB
S/N (A-weighted) (Note 7)	92	96		dB
Interchannel Isolation (Note 7, 8)	80	90		dB
Interchannel Gain Mismatch (Note 7, 8)	-	0.3	-	dB
Gain Drift	-	200	-	ppm/°C
Load Resistance (AC-Lord, Note 10) TVOUTL/R, VCROUTL/R, MONOOUT	4.5			kΩ
Output Voltage (Note 9, 10)	1.85	2	2.15	Vrms
Power Supply Rejection (PSR) (Note 11)	-	50		dB

Note 6. Measured by Audio Precision System Two Cascade.
Note 7. Analog In to TVOUT. Path : AINL+/– (AINR+/–) → TVOUTL (TVOUTR)
Note 8. Between TVOUTL and TVOUTR with analog inputs (AINL/R+/–) 1kHz/0dB.
Note 9. THD+N : –80dB(min. at 2Vrns).
Note 10. Analog input voltage by LIN/RIN pins (0dB). Stereo output (typ@0dBFS) = 2Vrms × VD/5.
Do not output signals over 3Vrms.
Note 11. The PSR is applied to VD with 1kHz, 100mV.

FILTER CHARACTERISTICS

(Ta = 25°C; VP = 11.4 ~ 12.6V, VD = 4.75 ~ 5.25V, VVD1 = VVD2 = 4.75 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
LPF					
Frequency Response 0 ~ 20.0kHz	FR	-	± 0.5	-	dB

ANALOG CHARACTERISTICS (VIDEO)

(Ta = 25°C; VP = 12V, VD = 5V; VVD1 = VVD2 = 5V; unless otherwise specified.)

Parameter	Conditions	min	typ	max	Units
Sync Tip Clamp Voltage	at output pin.		0.7		V
Chrominance Bias Voltage	at output pin.		2.2		V
Gain	Input = 0.3Vp-p, 100kHz	5.5	6	6.5	dB
Interchannel Gain Mismatch	TVRC, TVG, TVB. Input = 0.3Vp-p, 100kHz.	–0.3	-	0.3	dB
Frequency Response	Input=0.3Vp-p, C1=C2=0pF. 100kHz to 6MHz. at 12MHz. at 27MHz.	 –1.0	 –3 –35	0.5 TBD	dB dB dB
Group Delay Distortion	At 4.43MHz with respect to 1MHz.			15	ns
Input Impedance	Chrominance input (internally biased)	40	60	-	kΩ
Input Signal	f = 100kHz, maximum with distortion < 1.0%, gain = 6dB.	-	-	1.5	Vpp
Load Resistance	(Note 12)	150	-	-	Ω
Load Capacitance	C1 (Note 12) C2 (Note 12)			400 15	pF pF
Dynamic Output Signal	f = 100kHz, maximum with distortion < 1.0%	-	-	3	Vpp
Y/C Crosstalk	f = 4.43MHz, 1Vp-p input. Among TVVOUT, TVRC, VCRVOUT and VCRC outputs.	-	–50	-	dB
S/N	Reference Level = 0.7Vp-p, CCIR 567 weighting. BW = 15kHz to 5MHz.	-	74	-	dB
Differential Gain	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-	TBD	-	%
Differential Phase	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-	TBD	-	Degree

Note 12. Refer the Figure 1.

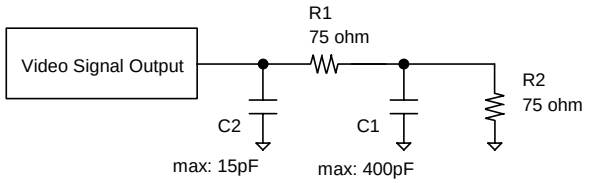


Figure 1. Load Resistance R1+R2 and Load Capacitance C1/C2.

SWITCHING CHARACTERISTICS

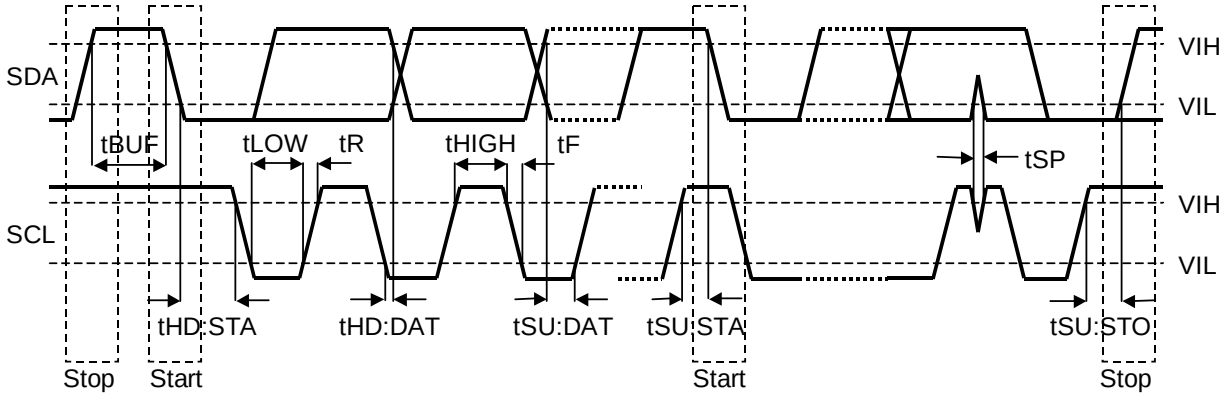
(Ta = 25°C; VP = 11.4 ~ 12.6V, VD = 4.75 ~ 5.25V, VVD1 = VVD2 = 4.75 ~ 5.25V; C_L = 20pF)

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 13)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Reset Timing					
PDN Pulse Width (Note 14)	tPD	150			ns

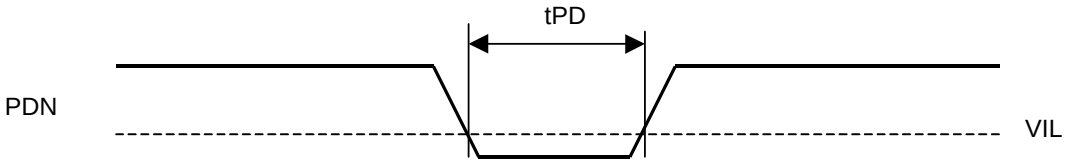
Note 13. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 14. The AK4703 should be reset by PDN pin = "L" upon power up.
Note 15. I^2C is a registered trademark of Philips Semiconductors.

Purchase of Asahi Kasei Microsystems Co., Ltd I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conform to the I^2C specifications defined by Philips.

■ **Timing Diagram**



I^2C Bus mode Timing



Power-down Timing

OPERATION OVERVIEW

1. System Reset and Power-down options

The AK4703 should be reset once by bringing PDN pin = "L" upon power-up. The AK4703 has several operation modes. The PDN pin, AUTO bit, BIAS bit, STBY bit and AMP bit control operation modes as shown in Table 1 and Table 2

Mode	PDN pin	AUTO bit	STBY bit	BIAS bit	AMPPD bit	Mode
0	"L"	*	*	*	*	Full Power-down
1	"H"	1	*	*	*	Auto Startup mode (Power-on Default)
2	"H"	0	1	1	*	Standby & Mute
3	"H"	0	1	0	*	Standby
4	"H"	0	0	1	1	Mute (AMP power down)
5	"H"	0	0	1	0	Mute (AMP operation)
6	"H"	0	0	0	1	Normal operation (AMP power down & Analog input)
7	"H"	0	0	0	0	Normal operation (AMP operation)

Table 1. Operation Mode Settings (*: Don't Care)

Mode			Register Control	Audio Bias Level	Video Output	TVFB, TVSB	VCRSB
0	Full Power-down		Not available	Power down	Hi-Z	Hi-Z	Pull-down (*)
1	Auto Startup mode (Power-on Default)	No video input	Available	Power down	Hi-Z	Hi-Z	Pull-down (*)
		Video input (**)		Active	Active (***)	Active	Active
2	Standby & Mute			Power down	Hi-Z / Active		
3	Standby			Active			
4	Mute (AMP power down)			Power down			
5	Mute (AMP operation)						
6	Normal operation (AMP power down & Analog input)			Active (****)			
7	Normal operation (AMP operation)						

(*): Internally pulled down by 120kΩ (typ) resistor.
(**): Video input to TVVIN or VCRVIN.
(***): VCRC outputs 0V for termination.
(****): TVOUTL/R are muted by Mute bit in the default state.

Table 2. Status of each operation modes

■ Full Power-down Mode

The AK4703 should be reset once by bringing PDN pin = "L" upon power-up.

PDN pin: Power down pin
L: Device power down.
H: Normal operation.

■ Auto Startup Mode

After when the PDN pin is set to "H", the AK4703 is in the auto startup mode. In this mode, all blocks except for the video detection circuit are powered down. Once the video detection circuit detects video signal from TVVIN pin or VCRVIN pin, the AK4703 goes to the stand-by mode automatically and sends "H" pulse via INT pin. To exit the auto startup mode, set the AUTO bit to "0".

AUTO bit (00H D3): Auto startup bit
0: Auto startup disable. (Manual startup)
1: Auto startup enable. (Default)

■ AMP Power-down Mode

The internal AMP block can be powered-down by AMPPD bit. When AMPPD bit ="1", the internal AMP block is powered-down.

AMPPD bit (00H D2): AMP power-down bit
0: Normal operation.
1: AMP power-down. (Default)

■ Bias Mode

When the BIAS bit = "1", the bias voltage on the audio output goes to GND level. Bringing BIAS bit to "0" changes this bias voltage smoothly from GND to VP/2 by 2sec (typ.). This removes the huge click noise related the sudden change of bias voltage at power-on. The change of BIAS bit from "1" to "0" also makes smooth transient from VP/2 to GND by 2sec (typ). This removes the huge click noise related the sudden change of bias voltage at power-off.

BIAS bit (00H D1): Bias-off bit
0: Normal operation.
1: Set the audio bias to GND. (Default)

■ Standby Mode

When the AUTO bit = BIAS bit = "0" and the STBY bit = "1", the AK4703 is forced into TV-VCR loop through mode. In this mode, the sources of TVOUTL/R and MONOOUT pins are fixed to VCRINL/R pins; the sources of VCROUTL/R are fixed to TVINL/R pins respectively. All register values themselves are NOT changed by STBY bit = "1".

STBY bit (00H D0): Standby bit
0: Normal operation.
1: Standby mode. (Default)

■ Normal Operation Mode

To change analog switches, set the AUTO bit, BIAS bit and STBY bit to "0". The AK4703 is in power-down mode until PDN pin = "H". The Figure 2 shows an example of the system timing at the power-down and power-up by PDN pin.

■ Typical Operation Sequence (auto setup mode)

The Figure 2 shows an example of the system timing at auto setup mode.

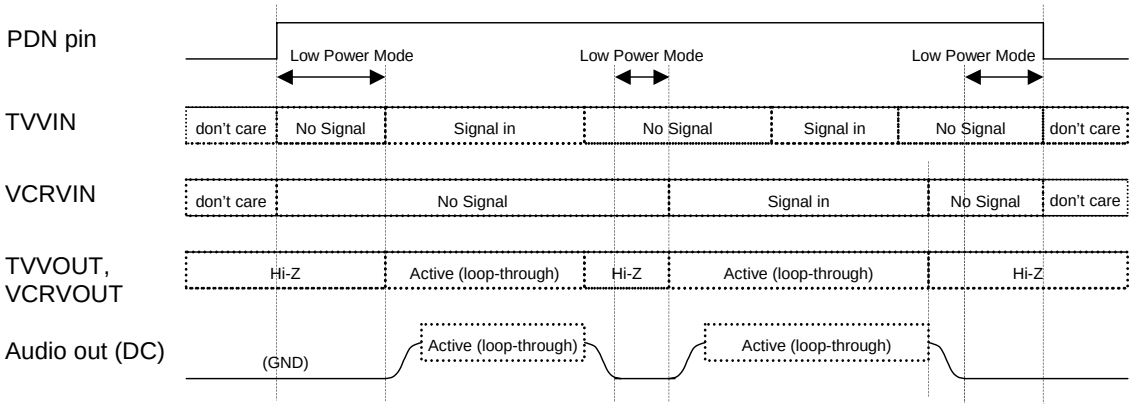
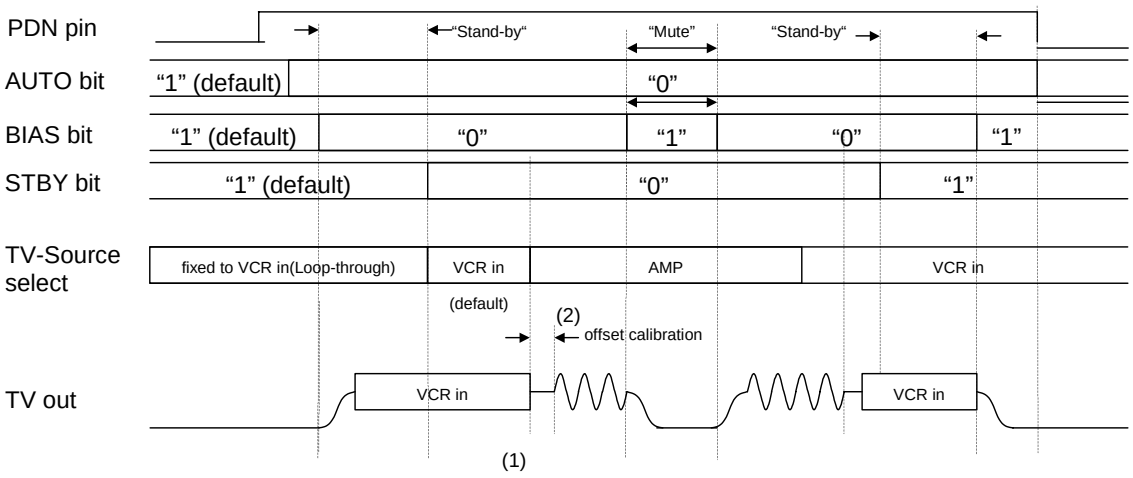


Figure 2. Typical operating sequence (auto setup mode)

■ Typical Operation Sequence (except auto setup mode)

The Figure 3 shows an example of the system timing at auto setup mode.



Notes:

(1) Mute the analog outputs externally if click noise (1) adversely affects the system.

(2) In case of the CAL bit = "1", the offset calibration is always executed when the source of TVOUTL/R pins are switched to AMP after the STBY bit is changed to "0". To disable this function, set the CAL bit = "0".

Figure 3. Typical operating sequence (except auto setup mode)

2. Audio Block

■ Switch Control

The AK4703 has switch matrixes designed primarily for SCART routing. Those are controlled via the control register as shown in, Table 3, Table 4 and Table (Please refer to the Block Diagram).

(01H: D1-D0)

TV1	TV0	Source of TVOUTL/R
0	0	AMP
0	1	VCRIN (Default)
1	0	Mute
1	1	LIN/RIN

Table 3. TVOUT Switch Configuration

(01H: D2-D0)

MSEL	TV1	TV0	Source of MONOOUT
0	0	0	AMP (L+R)/2
0	0	1	AMP (L+R)/2
0	1	0	AMP (L+R)/2
0	1	1	(Reserved)
1	0	0	AMP (L+R)/2
1	0	1	VCRIN (L+R)/2
1	1	0	Mute
1	1	1	(LIN+RIN)/2

Table 4. MONOOUT Switch Configuration

(01H: D5-D4)

VCR1	VCR0	Source of VCROUTL/R
0	0	AMP
0	1	TVIN (Default)
1	0	Mute
1	1	(Reserved)

Table 5. VCROUT Switch Configuration

3. Video Block

■ Video Switch Control

The AK4703 has switches for TV, VCR and RF modulator. Each switch can be controlled via registers independently. When AUTO bit = "1" or STBY bit = "1", these switches setting is ignored and set to fixed configuration (loop-through mode). Please refer the auto setup mode and standby mode.

(04H: D2-D0)

Mode	VTV2-0 bit	Source of TVVOUT pin	Source of TVRC pin	Source of TVG pin	Source of TVB pin
Shutdown	000	(Hi-Z)	(Hi-Z)	(Hi-Z)	(Hi-Z)
Encoder CVBS /RGB	001	ENCV pin	ENCRC pin	ENCG pin	ENCB pin
Encoder Y/C 1	010	ENCV pin	ENCRC pin	Hi-Z	(Hi-Z)
Encoder Y/C 2	011	ENCY pin	ENCC pin	Hi-Z	(Hi-Z)
VCR (default)	100	VCRVIN pin	VCRRC pin	VCRG pin	VCRB pin
TV CVBS	101	TVVIN pin	(Hi-Z)	(Hi-Z)	(Hi-Z)
(Reserved)	110	-	-	-	-
(Reserved)	111	-	-	-	-

Table 6. TV video output (Please refer notes)

(04H: D5-D3)

Mode	VVCR2-0 bit	Source of VCRVOUT pin	Source of VCRC pin
Shutdown	000	(Hi-Z)	(Hi-Z)
Encoder CVBS or Y/C 1	001	ENCV pin	ENCRC pin
Encoder CVBS or Y/C 2	010	ENCY pin	ENCC pin
TV CVBS (default)	011	TVVIN pin	(Hi-Z)
VCR	100	VCRVIN pin	VCRRC pin
(Reserved)	101	-	-
(Reserved)	110	-	-
(Reserved)	111	-	-

Table 7. VCR video output (Please refer notes)

(04H: D7-D6)

Mode	VRF1-0 bit	Source of RFV pin
Encoder CVBS1	00	ENCV pin
Encoder CVBS2	01	ENCG pin (Note 2)
VCR (Default)	10	VCRVIN pin
Shutdown	11	(Hi-Z)

Table 8. RF video output

Note 1. When input the video signal via ENCRC pin or VCRRC pin, set CLAMP1-0 bits respectively.
Note 2. When VTV2-0 bit = "001", TVG bit = "1" and VRF1-0 bit = "01", RFV pin output is same as TVG pin output (Encoder G).

■ Video Output Control (05H: D6-D0)

Each video output can be set to Hi-Z individually via control registers. These settings are ignored when the AUTO bit = "1". When the CIO bit = "1", the VCRC pin outputs 0V even if the VCRC bit = "0". When the CIO bit = "0", the VCRC pin follows the setting of VCRC bit. Please refer the "Red/Chroma Bi-directional Control for VCR SCART".

TVV: TVVOUT output control
TVR: TVRCOUT output control
TVG: TVGOUT output control
TVB: TVBOUT output control
VCRV: VCRVOUT output control
VCRC: VCRC output control
TVFB: TVFB output control
0: Hi-Z. (Default)
1: Active.

■ Red/Chroma Bi-directional Control for VCR SCART (05H: D7, D5)

The 4703 supports the bi-directional Red/Chroma signal on the VCR SCART.

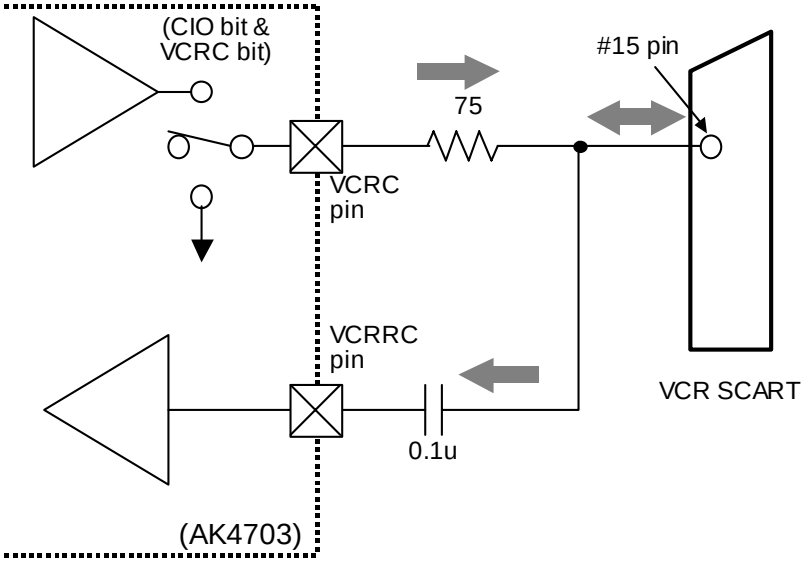


Figure 5. Red/Chroma Bi-directional Control

CIO bit	VCRC bit	State of VCRC pin
0	0	Hi-z (default)
0	1	Active
1	0	Connected to GND
1	1	Connected to GND

Table 9. Red/Chroma Bi-directional Control

■ Clamp and DC-restore circuit control (06H: D6-D5, D3-D2)

Each CVBS and Y input has the sync tip clamp circuit. The sync tip voltage at each output is 0.7V (typ). This corresponds 0.35V (typ) at the SCART connector when matched by 75Ω resistors. The CLAMP1-0 bits select the input circuit for ENCRC pin (Encoder Red/Chroma) and VCRRC pin (VCR Red/Chroma) respectively. VCLP1-0 bits select the source of DC-restore circuit.

CLAMP1: Encoder Red/Chroma (ENCRC pin) input clamp control
0: DC restore clamp active (for RED signal. Default)
1: Biased (for Chroma signal.)

CLAMP0: VCR R/C (VCRRC pin) input clamp control
0: DC restore clamp active (for RED signal)
1: Biased (for Chroma signal. Default.)

VCLP1-0: DC restore source control
When the AUTO bit = "1", the source is fixed to VCRVIN.

VCLP1 bit	VCLP0 bit	Sync Source of DC Restore
0	0	ENCV (Default)
0	1	ENCY
1	0	VCRVIN
1	1	(Reserved)

Table 10. DC restore source control

4. Blanking Control

The AK4703 supports Fast Blanking signals and Slow Blanking (Function Switching) signals for TV/VCR SCART.

■ Input/Output Control for Fast/Slow Blanking

FB1-0: TV Fast Blanking output control (07H: D1-D0)

FB1 bit	FB0 bit	TVFB pin Output Level
0	0	0V (Default)
0	1	4V
1	0	Same as VCR FB input (4V/0V)
1	1	(Reserved)

Table 11. TV Fast Blanking output (Note: minimum load is 150Ω)

SBT1-0: TV Slow Blanking output control (07H: D3-D2)

SBT1 bit	SBT0 bit	TVSB pin Output Level
0	0	< 2V (Default)
0	1	5V <, < 7V
1	0	(Reserved)
1	1	10V <

Table 12. TV Slow Blanking output (Note: minimum load is 10kΩ)

SBV1-0: VCR Slow Blanking output control (07H: D5-D4)

SBV1 bit	SBV0 bit	VCRSB pin Output Level
0	0	< 2V (Default)
0	1	5V <, < 7V
1	0	(Reserved)
1	1	10V <

Table 13. VCR Slow Blanking output (Note: minimum load is 10kΩ)

SBIO1-0: TV/VCR Slow Blanking I/O control (07H: D7-D6)

SBIO1 bit	SBIO0 bit	VCRSB pin Direction	TVSB pin Direction	
0	0	Output (Controlled by SBV1-0 bits)	Output (Controlled by SBT1-0 bits)	(Default)
0	1	(Reserved)	(Reserved)	
1	0	Input (Stored in SVCR1-0 bits)	Output (Controlled by SBT1-0 bits)	
1	1	Input (Stored in SVCR1-0 bits)	Output (Same output as VCR SB)	

Table 14. TV/VCR Slow Blanking I/O control

5. Monitor Options and INT function

■ Monitor Options (08H: D4-D0)

The AK4703 has several monitors for the input DC level of VCR slow blanking, the input DC level of VCR fast blanking and signals input to TVVIN or VCRVIN pins. SVCR1-0 bits, FVCR bit, VCMON bit and TVMON bit are reflected to these values.

SVCR1-0: VCR Slow blanking status monitor
SVCR1-0 bits reflect the voltage at VCRSB pin only when the VCRSB is in the input mode.
When the VCRSB is in the output mode, SVCR1-0 bits hold previous value.

VCRSB pin input level	SVCR1 bit	SVCR0 bit
< 2V	0	0
4.5 to 7V	0	1
(Reserved)	1	0
9.5 <	1	1

Table 15. VCR Slow Blanking monitor

FVCR: VCR Fast blanking input level monitor
This bit is enabled when TVFB bit = "1".

VCRFB pin input level	FVCR bit
< 0.4V	0
1V <	1

Table 16. VCR Fast Blanking monitor (Typical threshold is 0.7V)

VCMON: VCR input monitor
0: No video signal detected via VCRVIN pin.
1: Detects video signal via VCRVIN pin.

TVMON: TV input monitor
0: No video signal detected via TVVIN pin.
1: Detects video signal via TVVIN pin.

■ INT Function and Mask Options (09H: D3-D1)

Changes of the 08H status can be monitored via the INT pin. The INT pin is the open drain output and goes "L" for 2μs (typ.) when the status of 08H is changed. This pin should be connected to VD (typ. 5V) through 10kΩ resistor.
MVC bit, MTV bit, MFVCR bit and MSVCR bit control the reflection of the status change of these monitors onto the INT pin from report to prevent to masks each monitor.

MVC: VCR input monitor mask

AUTO bit	MVC bit	Reflection of the change of VCMON bit to INT pin	
0	0	Reflect	
0	1	NOT reflect (e.g. masked)	
1	0	Reflect	
1	1	Reflect	(Default)

Table 17. Reflection of VCMON change

MTV: TV input monitor mask

AUTO bit	MTV bit	Reflection of the change of TVMON bit to INT pin	
0	0	Reflect	
0	1	NOT reflect (e.g. masked)	
1	0	Reflect	
1	1	Reflect	(Default)

Table 18. Reflection of TVMON change

MFVCR: FVCR Monitor mask
0: Change of MFVCR is reflected to INT pin. (Default)
1: Change of MFVCR is NOT reflected to INT pin.

MSVCR: SVCR1-0 Monitor mask
0: Change of SVCR1-0 is reflected to INT pin. (Default)
1: Change of SVCR1-0 is NOT reflected to INT pin.

6. Control Interface

I^2C-bus Control Mode

1. WRITE Operations

Figure 6 shows the data transfer sequence in I^2C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 12). After the START condition, a slave address is sent. This address is 7bits long followed by an eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010001". If the slave address match that of the AK4703, the AK4703 generates the acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 13). A "1" for R/W bit indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed. The second byte consists of the address for control registers of the AK4703. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 8). The data after the second byte contain control data. The format is MSB first, 8bits (Figure 9). The AK4703 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 12).
The AK4703 can execute multiple one byte write operations in a sequence. After receipt of the third byte, the AK4703 generates an acknowledge, and awaits the next data again. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 09H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 14) except for the START and the STOP condition.

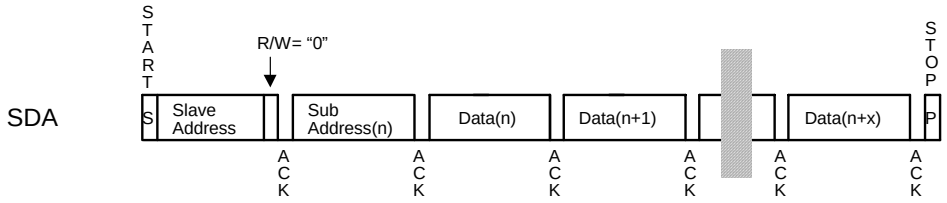


Figure 6. Data transfer sequence at the I^2C-bus mode

0	0	1	0	0	0	1	R/W

Figure 7. The first byte

0	0	0	A4	A3	A2	A1	A0

Figure 8. The second byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 9. Byte structure after the second byte

2. READ Operations

Set R/W bit = "1" for READ operations. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 09H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4703 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

2-1. CURRENT ADDRESS READ

The AK4703 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK4703 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4703 discontinues transmission.

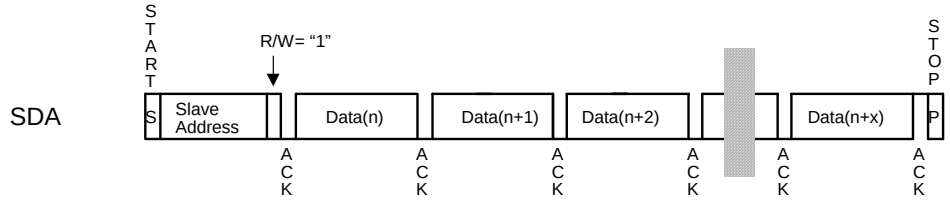


Figure 10. CURRENT ADDRESS READ

2-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address (R/W bit = "0") and then the register address to read. After the register's address is acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4703 generates an acknowledge, 1-byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4703 discontinues transmission.

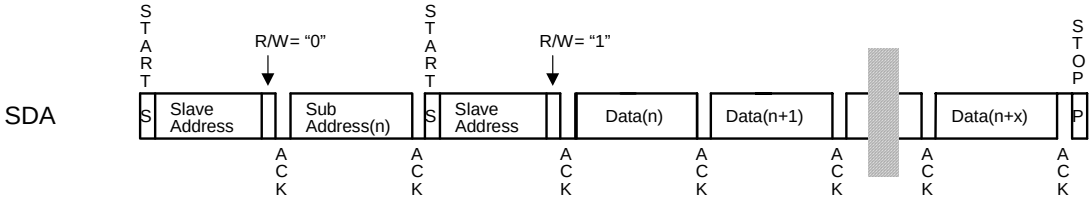


Figure 11. RANDOM ADDRESS READ

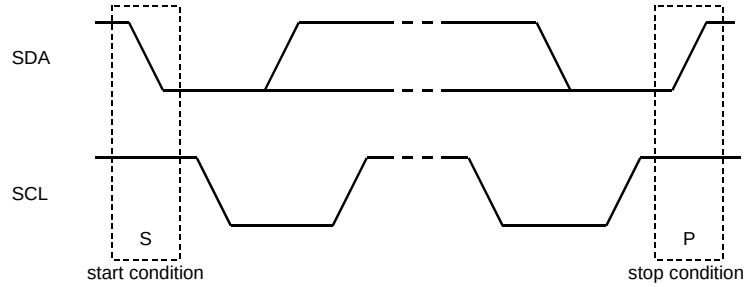


Figure 12. START and STOP conditions

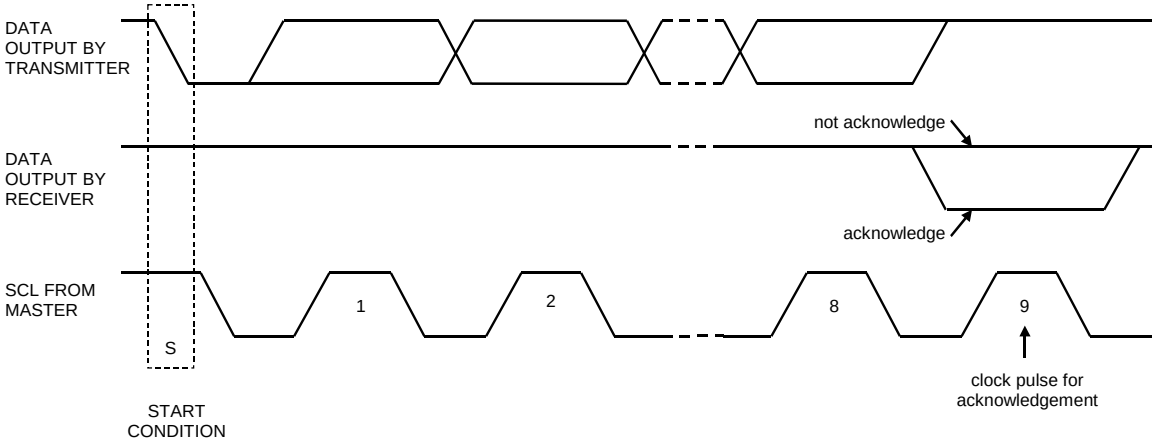


Figure 13. Acknowledge on the I^2C-bus

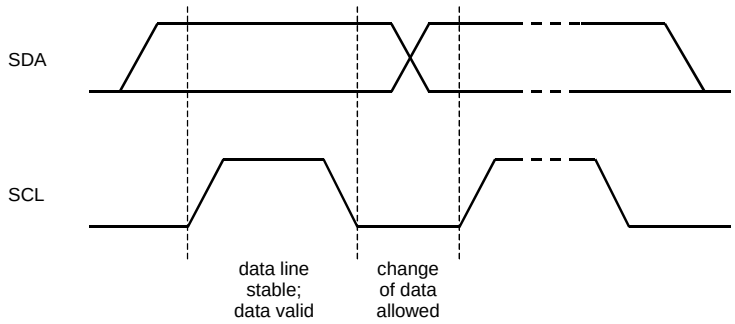


Figure 14. Bit transfer on the I^2C-bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	0	0	0	0	AUTO	AMPPD	BIAS	STBY
01H	Switch	MUTE	0	VCR1	VCR0	MONO	0	TV1	TV0
02H	Reserved	0	0	0	0	0	0	0	0
03H	Zerocross	0	VMONO	0	0	0	ZERO	ZTM1	ZTM0
04H	Video switch	VRF1	VRF0	VVCR2	VVCR1	VVCR0	VTV2	VTV1	VTV0
05H	Video output enable	CIO	TVFB	VCRC	VCRV	TVB	TVG	TVR	TVV
06H	Video volume/clamp	0	VCLP1	VCLP0	0	CLAMP1	CLAMP0	0	0
07H	S/F Blanking control	SBIO1	SBIO0	SBV1	SBV0	SBT1	SBT0	FB1	FB0
08H	S/F Blanking monitor	0	0	0	TVMON	VCMON	FVCR	SVCR1	SVCR0
09H	Monitor mask	0	0	0	MTV	MVC	MFVCR	MSVCR	0

When the PDN pin goes “L”, the registers are initialized to their default values.
While the PDN pin = “H”, all registers can be accessed.
Do not write any data to the register over 09H.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	0	0	0	0	AUTO	AMPPD	BIAS	STBY
R/W		R/W							
Default		0	0	0	0	1	1	1	1

STBY: Standby control
0: Normal Operation
1: Standby Mode (Default). All registers are not initialized.
DAC : Powered down and timings are reset.
Source of TVOUT : fixed to VCRIN,
Source of VCROUT : fixed to TVIN,
Source of MONOOUT : fixed to VCRIN,
Source of TVVOUT : fixed to VCRVIN (or Hi-Z),
Source of TVRC : fixed to VCRRC (or Hi-Z),
Source of TVG : fixed to VCRG (or Hi-Z),
Source of TVB : fixed to VCRB (or Hi-Z),
Source of VCRVOUT : fixed to TVVIN (or Hi-Z),
Source of VCRC : fixed to Hi-Z or VSS (controlled by CIO bit).

BIAS: Audio output control
0: Normal operation
1: ALL Audio outputs to GND (Default)

AMPPD: AMP power down control
0: Normal operation
1: AMP power down (Default)

AUTO: Auto startup bit
0: Auto startup disable (Manual startup).
1: Auto startup enable (Default).
Note: When the SBIO1 bit = “1”(Default = “0”), the change of AUTO bit may cause a “L” pulse on INT pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Switch	MUTE	0	VCR1	VCR0	MONO	0	TV1	TV0
R/W		R/W							
Default		1	0	0	1	0	0	0	1

TV1-0: TVOUTL/R pins source switch
- 00: AMP
- 01: VCRINL/R pins (Default)
- 10: MUTE
- 11: LIN/RIN

MONO: Mono select for TVOUTL/R pins
- 0: Stereo. (Default)
- 1: Mono. (L+R)/2

VCR1-0: VCROUTL/R pins source switch
- 00: AMP
- 01: TVINL/R pins (Default)
- 10: MUTE
- 11: Reserved

MUTE: Mute switch
- 0: Normal operation
- 1: Mute (Default)

  When Mute bit = “1”, TVOUTL/R outputs VCOM voltage after TVOUTL/R output is zero-crossing.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Selector	0	0	0	0	0	MSEL	0	0
R/W		R/W							
Default		0	0	0	0	0	1	0	0

MSEL: Selector for MONOOUT pin
- 0: Mixed output of AMP
- 1: Mixed output of TV1-0 switch (Default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Zerocross	0	VMONO	0	0	0	ZERO	ZTM1	ZTM0
R/W		R/W							
Default		0	0	0	0	0	1	0	0

ZTM1-0: The time length control of zero-cross timeout
- 00: typ. 10ms (Default)
- 01: typ. 20ms
- 10: typ. 40ms
- 11: typ. 80ms

ZERO: Zero-cross detection enable for TVOUT output
- 0: Disable
  The TVOUT outputs VCOM voltage immediately without zero-cross when MUTE bit is “1”.
- 1: Enable (Default)
  The TVOUT outputs VCOM voltage when timeout or zero-cross before timeout when MUTE bit is “1”.

VMONO: Mono select for VCROUTL/R pins
- 0: Stereo. (Default)
- 1: Mono. (L+R)/2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Video switch	VRF1	VRF0	VVCR2	VVCR1	VVCR0	VTV2	VTV1	VTV0
R/W		R/W							
Default		1	0	0	1	1	1	0	0

VTV2-0: Selector for TV video output
Please refer the Table 6.

VVCR2-0: Selector for VCR video output
Please refer the Table 7.

VRF1-0: Selector for RFV pin output
Please refer the Table 8.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Output Enable	CIO	TVFB	VCRC	VCRV	TVB	TVG	TVR	TVV
R/W		R/W							
Default		0	0	0	0	0	0	0	0

TVV: TVVOUT output control
TVR: TVRCOUT output control
TVG: TVGOUT output control
TVB: TVBOUT output control
VCRV: VCRVOUT output control
VCRC: VCRC output control (Please refer the Table 9)
TVFB: TVFB output control
0: Hi-Z (Default)
1: Active.
When the CIO pin = "H", the VCRC pin is connected to GND even if VCRC bit = "0".
When the CIO pin = "L", the VCRC pin follows the setting of VCRC bit.

CIO: VCRC pin I/O control
Please refer the Table 9.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Video volume	0	VCLP1	VCLP0	0	CLAMP1	CLAMP0	0	0
R/W		R/W							
Default		0	0	0	0	0	1	0	0

CLAMP1: Encoder R/Chroma (ENCRC pin) input clamp control
0: DC restore clamp active (for RED signal. Default)
1: Biased (for Chroma signal.)

CLAMP0: VCR R/C (VCRC pin) input clamp control
0: DC restore clamp active (for RED signal)
1: Biased (for Chroma signal. Default.)

VCLP1-0: DC restore source control
00: ENCV pin (Default)
01: ENCY pin
10: VCRVIN pin
11: (Reserved)
When the AUTO bit = "1", the source is fixed to VCRVIN pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	S/F Blanking	SBIO1	SBIO0	SBV1	SBV0	SBT1	SBT0	FB1	FB0
R/W		R/W							
Default		0	0	0	0	0	0	0	0

FB1-0: TV Fast Blanking output control (for TVFB pin)
- 00: 0V (Default)
- 01: 4V
- 10: follow VCR FB input (4V/0V)
- 11: (Reserved)

SBT1-0: TV Slow Blanking output control (for TVSB pin. minimum load is 10kΩ.)
- 00: < 2V (Default)
- 01: 5V <, < 7V
- 10: (Reserved)
- 11: 10V <

SBV1-0: VCR Slow Blanking output control (for VCRSB pin. minimum load is 10kΩ.)
- 00: < 2V (default)
- 01: 5V <, < 7V
- 10: (Reserved)
- 11: 10V <

SBIO1-0: TV/VCR Slow Blanking I/O control (Please refer the Table 14.)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	SB/FB monitor	0	0	0	TVMON	VCMON	FVCR	SVCR1	SVCR0
R/W		READ							
Default		0	0	0	0	0	0	0	0

SVCR1-0: VCR Slow blanking status monitor

SVCR1-0 bits reflect the voltage at VCRSB pin only when the VCRSB is in the input mode. When the VCRSB is in the output mode, SVCR1-0 bits hold previous value.

VCRSB pin input level	SVCR1 bit	SVCR0 bit
< 2V	0	0
4.5 to 7V	0	1
(Reserved)	1	0
9.5 <	1	1

Table 19. VCR Slow Blanking monitor

FVCR: VCR Fast blanking input level monitor

This bit is enabled when TVFB bit = "1".

VCRFB pin input level	FVCR bit
< 0.4V	0
1V <	1

Table 20. VCR Fast Blanking monitor (Typical threshold is 0.7V)

VCMON: VCR input monitor

0: No video signal detected via VCRVIN pin.
1: Detects video signal via VCRVIN pin.

TVMON: TV input monitor

0: No video signal detected via TVVIN pin.
1: Detects video signal via TVVIN pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Monitor mask	0	0	0	MTV	MVC	MFVCR	MSVCR	0
R/W		R/W							
Default		0	0	0	0	1	0	0	0

MSVCR: SVCR1-0 bits Monitor mask
0: The INT pin reflects the change of SVCR1-0 bit. (Default)
1: The INT pin does not reflect the change of SVCR1-0 bits.

MFVCR: FVCR Monitor mask
0: The INT pin reflects the change of MFVCR bit. (Default)
1: The INT pin does not reflect the change of MFVCR bit.

MVC: VCR input monitor mask
Please refer the Table 17.

MTV: TV input monitor mask
Please refer the Table 18.

SYSTEM DESIGN

TBD

Figure 15. Typical Connection Diagram

■ Grounding and Power Supply Decoupling

VD, VP, VVD1, VVD2, VSS and VVSS should be supplied from analog supply unit with low impedance and be separated from system digital supply. An electrolytic capacitor 10μF parallel with a 0.1μF ceramic capacitor should be attached to these pins to eliminate the effects of high frequency noise. The 0.1μF ceramic capacitor should be placed as near to VD (VP, VVD1, VVD2) as possible.

■ Voltage Reference

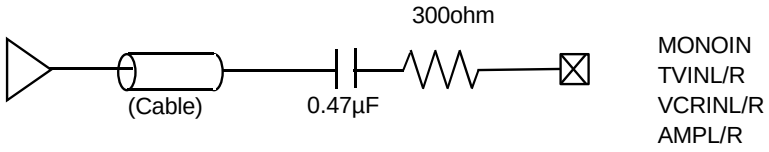
Each DVCOM/PVCOM are signal ground of this chip. An electrolytic capacitor 10μF parallel with a 0.1μF ceramic capacitor should be attached to these VCOM pins to eliminate the effects of high frequency noise. No load current may be drawn from these VCOM pins. All signals, especially clocks, should be kept away from these VCOM pins in order to avoid unwanted coupling into the AK4703.

■ Analog Audio Outputs

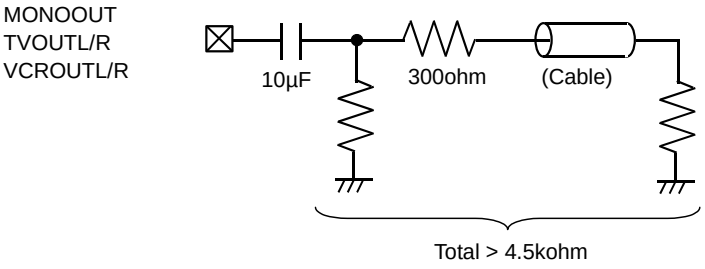
The analog outputs are also single-ended and centered on 5.6V(typ.). The output signal range is typically 2Vrms (typ@VD=5V).

■ External Circuit Example

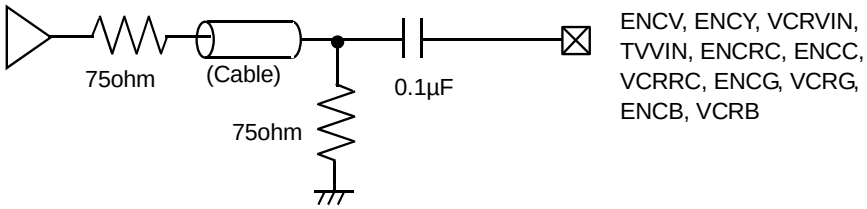
Analog Audio Input pin



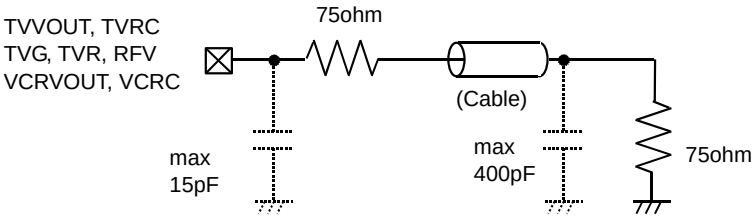
Analog Audio Output pin



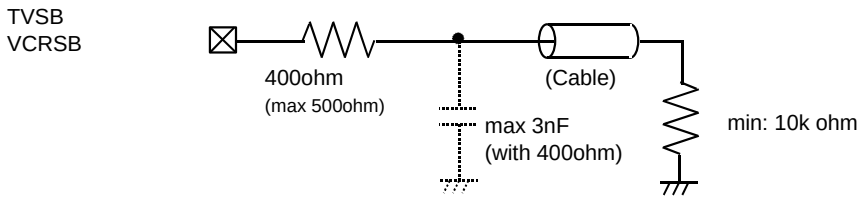
Analog Video Input pin



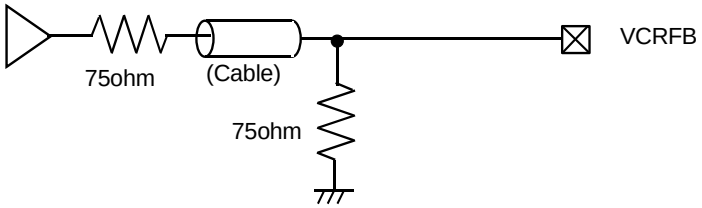
Analog Video Output pin



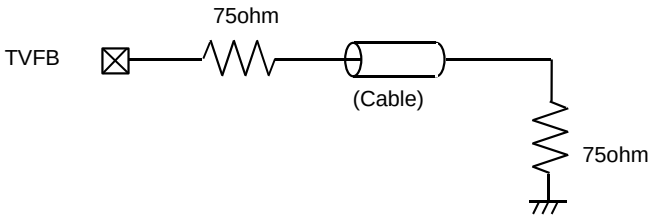
Slow Blanking pin



Fast Blanking Input pin



Fast Blanking Output pin



PACKAGE

TBD

■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING

TBD

XXXXXXXX: Date code identifier

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