AK7750

Audio DSP with Built-in Hands-Free Phone Features

General Description

The AK7750 is a highly integrated Audio Digital Signal Processor with a stereo audio codec in one chip. The AK7750 combines an on-chip DSP and an ARM7 processor that can be used to create Echo Cancellation (EC) and Noise Cancellation (NC) functions. These functions make the AK7750 a perfect choice for hands-free phones that require suppressing acoustic echo and noise. Voice quality and noise suppression levels can be precisely adjusted by externally setting various parameters. Additionally, no external Flash, ROM, or RAM is required as memories for Echo and Noise Cancellation are integrated on-chip.

By using an external microprocessor to change algorithms, the AK7750 can be used in other audio applications including sound field enhancements like surround, volume control, parametric equalizer and speaker compensation. These functions are simplified by the AK7750 through the integration of 64K bit delay data RAM, a high-performance audio Codec with sample rates from 8 KHz ~ 48 KHz, and 8-channels of Digital Audio input / output.

What's more, the latest Surround Decoders can be also be implemented by using the certified algorithms from various technology partners.

Features

[DSP Block]

- Data Word Length: 24 bit
- Machine Cycle: 27.1 ns (fastest) (768fs at 48 KHz)
- Number of Steps: 768 steps max. at fs = 48 KHz
  4608 steps max. at fs = 8 KHz
  192 steps max. at fs = 192 KHz
- Multiply: 24 x 16 -> 40 bit (enables double precision operation)
- Division: 24 / 24 -> 24 bit or 16 bit
- ALU: 34 bit arithmetic operation (overflow margin 4 bits)
  24 bit arithmetic & logic operations
- Shift: 1,2,3,4,6,8,15 Bit Left Shift with indirect shift function
  1,2,3,4,8,14,15 bit Right Shift with indirect shift function
- Program RAM (PRAM): 768 words x 32 bit
- Coefficient RAM (CRAM): 1024 words x 16 bit
- Data RAM (DRAM): 256 words x 24 bit
- Offset RAM (OFRAM): 48 words x 12 bit
- Delay RAM (DLRAM): 64K bits (following 3 types are selectable):
  - 1K words 24 bit
  - 1K words 24 bit & 2K words 16 bit (limited pointer capability)
  - 4kword 16bit
    Data Compression/Expansion circuits for 16 bit data handling are integrated on-chip
    (Dynamic-range: 23 bit equivalent, S/N+D: 15 bit equivalent (FS)).
  - In Hands-free mode, Delay RAM cannot be used.
- Registers: 34 bits x 4 (ACC) [for ALU]
  24 bit x 8 (TMP) [for DBUS Interface]
  24 bit x 6 stage stacks (PTMP) [for DBUS Interface]
- On-chip ARM7TDMI Processor:

[ADC Block]
- 24 Bit 2 Channels (fs: 8 KHz ~ 48 KHz)
- S/N+D: 91 dB (fs = 48 KHz)
- Dynamic Range & S/N: 98 dBA (fs = 48 KHz)
- On-chip DC offset canceling High Pass Filter

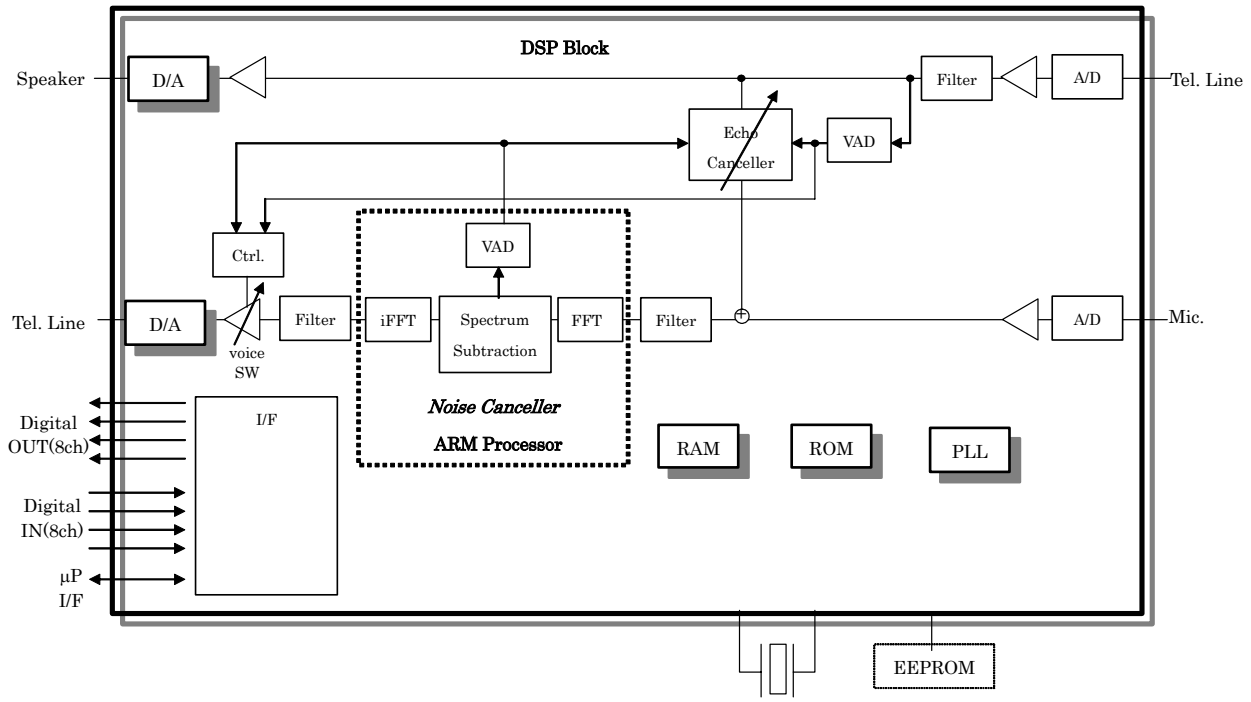
[DAC Block]
- 24 Bit 2 Channels
- S/N+D: 86 dB (fs = 48 KHz)
- Dynamic Range & S/N: 98 dBA (fs = 48 KHz)

[Input/Output Digital Interface]
- Serial Data Input 8 channels (10 channels with on-board codec.)
- Serial Data Output 6 channels (8 channels with on-board codec.)
- Microprocessor Interface: 1 set of inputs and outputs

[General]
- On-chip PLL
- On-chip EEPROM (AK6512C, AK6514C) Interface
- Single 3.3 V +/- 0.3 V Power Supply
- Operating Temperature Range: -40°C to +85°C
- 64-Pin LQFP

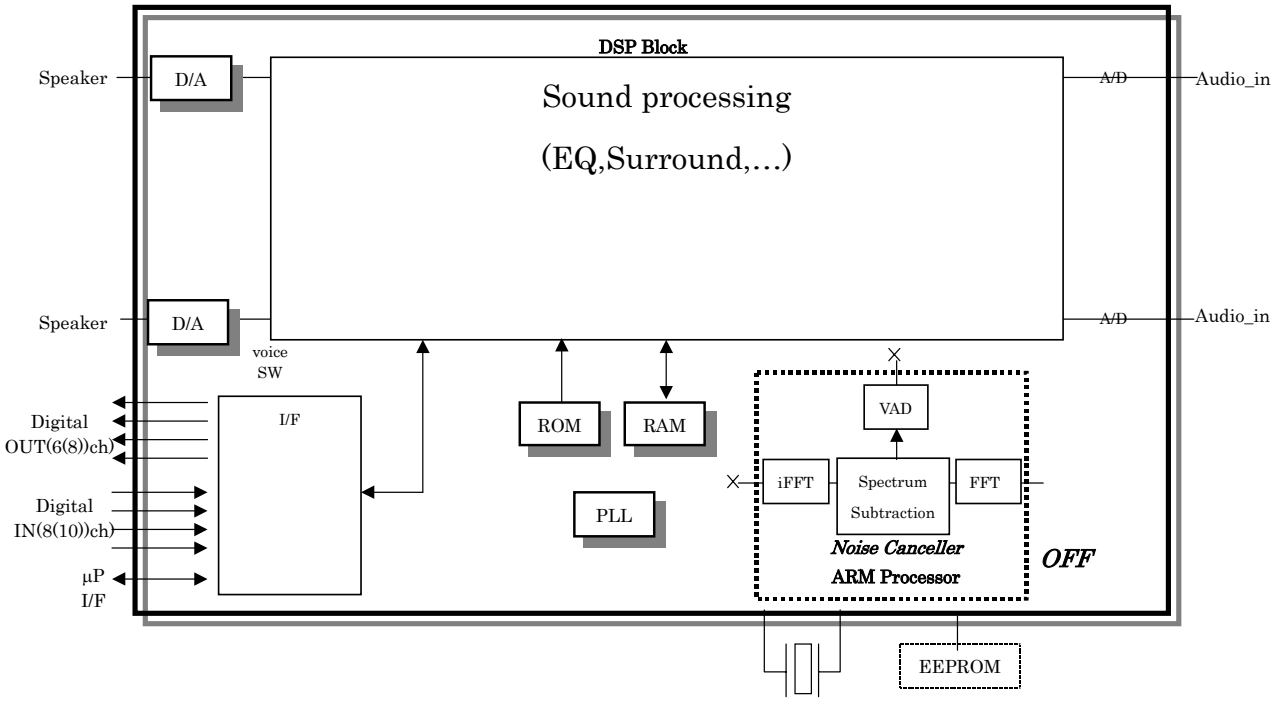
Block Diagram

(1) Hands-Free Mode Diagram



Block Diagram

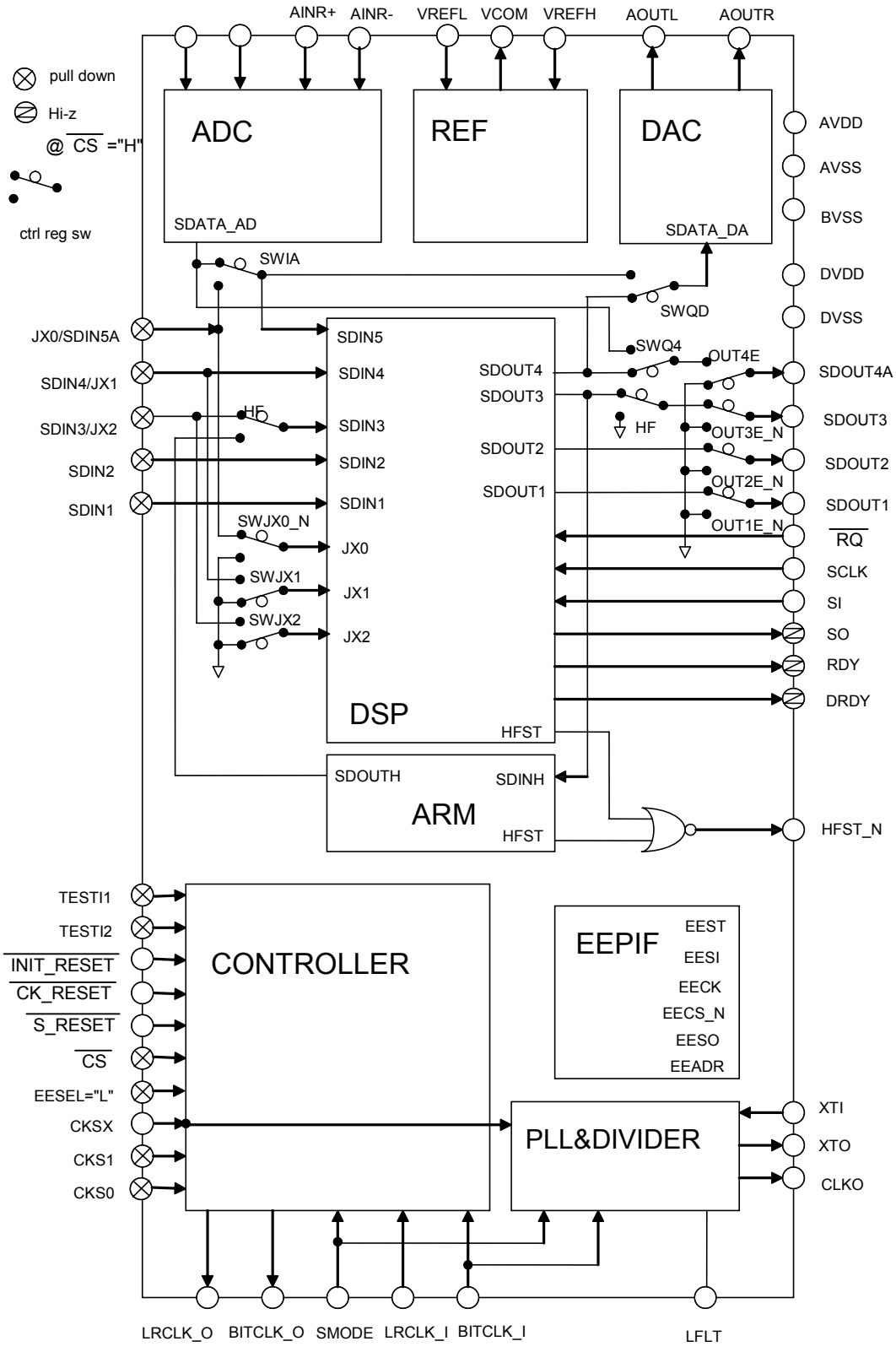
(2) Audio Surround Mode Diagram



Block Diagram

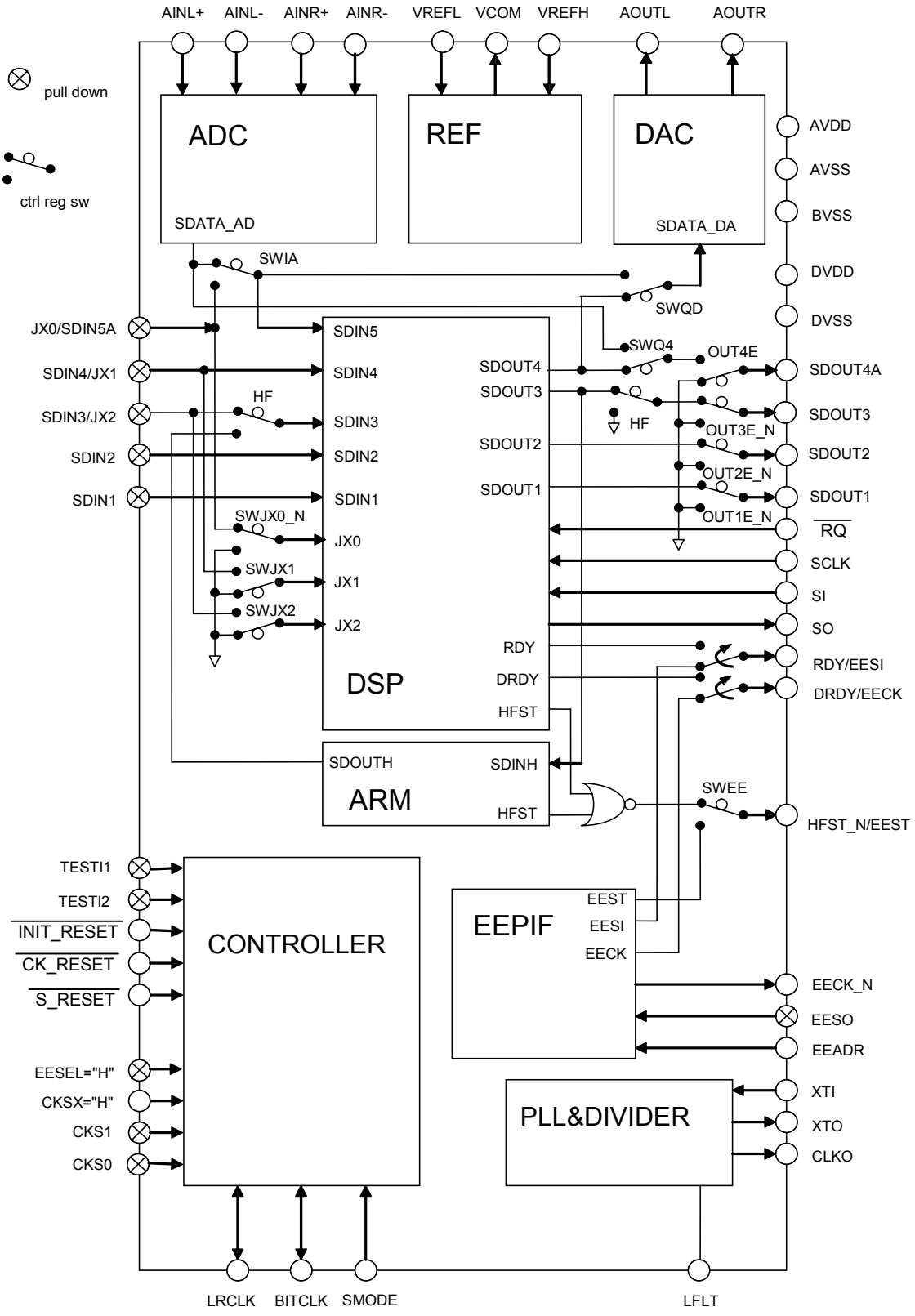
(2) Total Block Diagram

1) EESEL = " L "



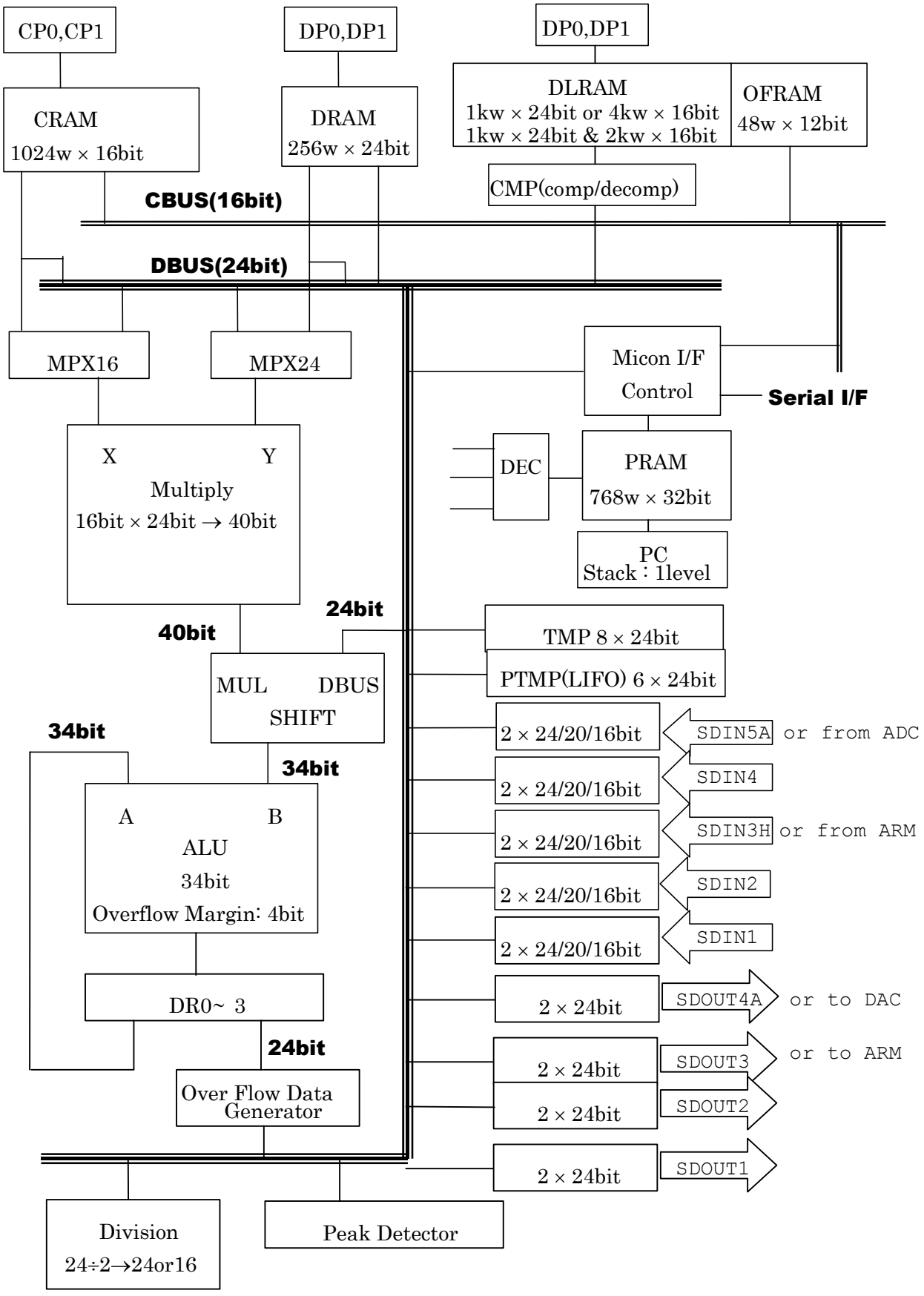
The above shows a simplified AK 7750 block diagram. It does not necessarily show the circuit diagram.

2) EESEL = " H "



The above shows a simplified AK 7750 block diagram. It does not necessarily show the circuit diagram.

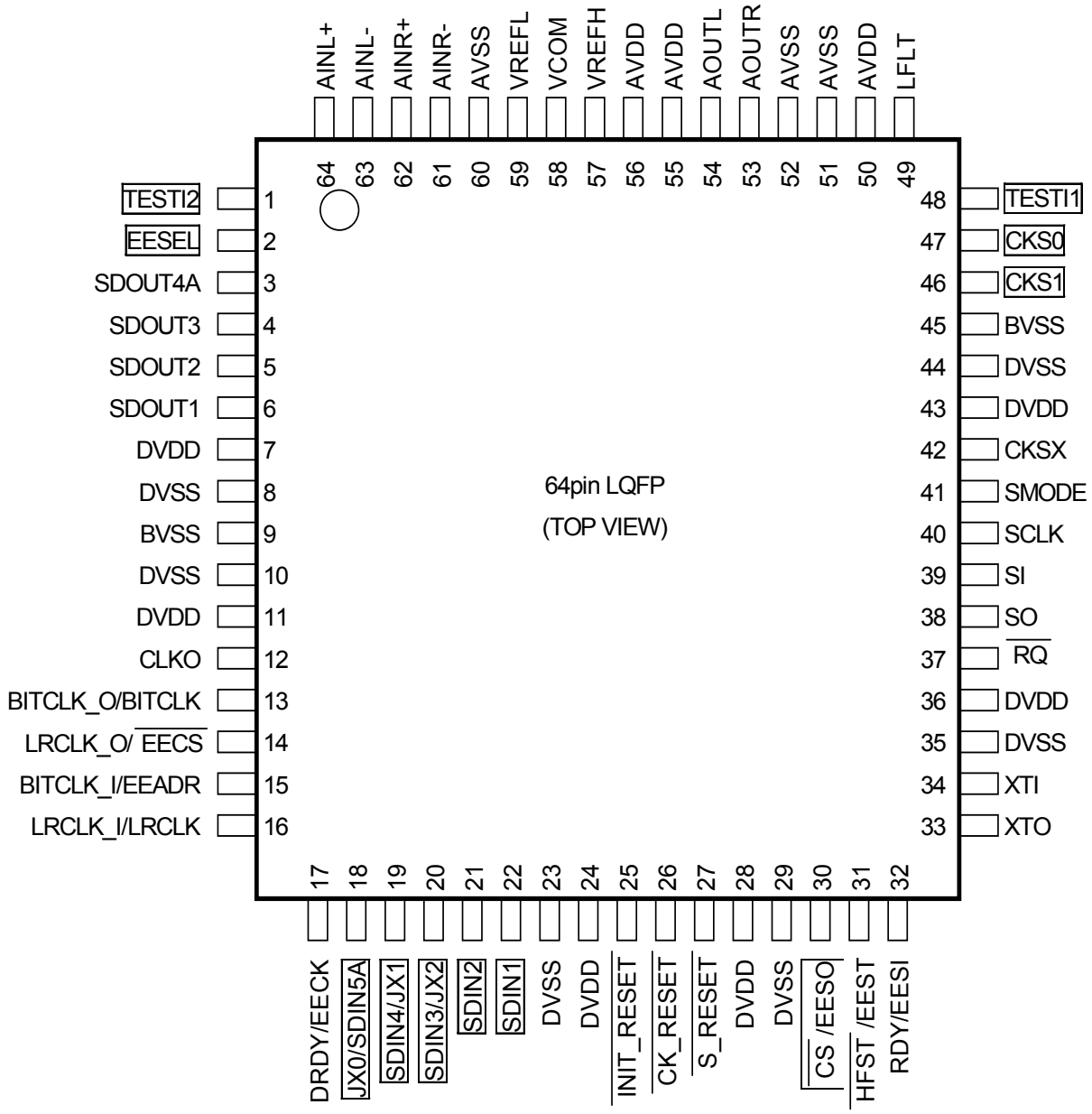
(3) DSP Block Diagram



Input/Output Pin Description

(1) Pin Assignment

Note) *** indicates *Pulled-down* pins (xxx : pin name)



*** pins (*** is pin name) are pulled down to the digital ground of the device INTERNALLY. The words, "*pulled-down*" with italic type characters in the following "Pin Functional Description" are used to clarify this function.

(3) Pin Functional Description

Pin NO.	Pin Name	I/O	Function	Pin Classification
1	TESTI2	I	**Test pin (*pulled-down*)**. Connect to DVSS	Test
2	EESEL	I	**Control mode select pin (*pulled-down*)** EESEL="L": for general use EESEL="H": program can be downloaded to the AKM's EEPROMs, AK6512C, AK6514C. EESEL pin must be fixed to either "L" or "H" level.	Control
3	SDOUT4A	O	**DSP Serial Data Output pin** - MSB-justified 24 Bit data is output. - ADC Data output, selected by Control Register setting.	Digital Serial data output
4	SDOUT3	O	**DSP Serial Data Output pin** - MSB-justified 24 Bit data is output. - "L" is output during the hands-free operation.	
5	SDOUT2	O	**DSP Serial Data Output pin** - MSB-justified 24 Bit data is output.	
6	SDOUT1	O	**DSP Serial Data Output pin** - MSB-justified 24 Bit data is output.	
7	DVDD	-	Digital Power Supply pin 3.3 V (typ)	Digital Power Supply
8	DVSS	-	**Digital Ground pin 0 V**	Digital Power Supply
9	BVSS	-	**Ground pin (silicon substrate potential)** Connect to AVSS.	Analog Power Supply
10	DVSS	-	**Digital Ground pin 0 V**	Digital Power Supply
11	DVDD	-	**Digital Power Supply pin 3.3 V (typ)**	Digital Power Supply
12	CLKO	O	**Clock Output pin** Set by Control Register	Clock Output
13	BITCLK_O (EESEL="L")	O	**Serial Bit Clock Output pin** SMODE="H": 64fs clock is output during master mode operation. SMODE="L": BITCLK-I clock is output during slave mode operation (except for DIF mode 5 and 6)	System Clock
	BITCLK (EESEL="H")	I/O	**Serial Bit Clock Input/Output pin** SMODE="H": 64fs clock is output during master mode operation. SMODE="L": 64fs clock is input during slave mode operation (48fs clock can be output, except when using CKSX=L)	System Clock
14	LRCLK_O (EESEL="L")	O	**L/R Channel Select Output pin** SMODE="H": 1fs clock is output during master mode operation. SMODE="L": LRCLK-I clock is output during slave mode operation (except for DIF mode 5 and 6).	System Clock
	$\overline{\text{EECS}}$ (EESEL="H")	O	**EEPROM Chip Select Output pin** Connect to $\overline{\text{CS}}$ pin of AK6512C/14C.	EEP

Pin NO.	Pin Name	I/O	Function	Pin Classification
15	BITCLK_I (EESEL="L")	I	**Serial Bit Clock Input pin** SMODE="H": When master mode is used, connect this pin to DVSS. SMODE="L": 64fs clock is input during slave mode operation. (48fs clock can be input except for CKSX="L"). BITCLK-I (64fs) can be used as master clock (CKSX="L") during slave mode operation	Sytem Clock
	EEADR (EESEL="H")	I	**EEP Address Select pin** AK6512C: used at EEADR="L". AK6514C: read data starting at 0000h when EEADR="L". Read data starting at 2000h when EEADR="H".	EEP
16	LRCLK_I (EESEL="L")	I	**L/R Channel Select Input pin** SMODE="H": When master mode is used, connect this pin to DVSS. SMODE="L": 1fs clock is input during slave mode operation.	System Clock
	LRCLK (EESEL="H")	I/O	**L/R Channel Select Input/Output pin** SMODE="H": 1fs clock is output during master mode operation SMODE="L": 1fs clock is input during slave mode operation	System Clock
17	DRDY (EESEL="H")	O	**Output Data Ready pin (Hi-Z)** For microprocessor interface Hi-Z state when $\overline{CS}$ ="H".	μC
	DRDY/EECK (EESEL="H")	O	**Output Data Ready pin for μC interface /** **EEPROM Serial Data Output pin.** Connect this pin to SCK pin of AK6512C/14C. After an EEPROM data read, (EEST transition from "L" to "H"), this pin is automatically switched to DRDY pin.	EEP/μC
18	JX0/SDIN5A		**External Conditional pin/DSP Serial Data Input pin (*pulled-down*).** - For normal use, this is the external conditional jump pin (JXO). - Input to the DSP's SDIN5 port is possible by setting a Control Register (normally SDIN5 is connected to ADC Serial Output, refer to block diagram). Supports MSB-justified 24 Bit /LSB-justified 24 Bit, 20 Bit, 16 Bit data formats.	Digital Conditional input / Serial data input
19	SDIN4/JX1	I	**DSP Serial Data Input pin/External Conditional pin (*pulled-down*)** - Supports MSB-justified 24Bit /LSB-justified 24Bit, 20Bit, 16bit formats - This pin can be used as external conditional jump pin JX1 by setting a control register	Digital Serial data input /conditional input

Pin NO.	Pin Name	I/O	Function	Pin Classification
20	SDIN3/JX2	I	**DSP Serial Data Input pin/External Conditional pin (*pulled-down*)** - Supports MSB-justified 24 Bit/LSB-justified 24 Bit, 20 Bit, and 16 Bit data formats. - This pin can be used as external conditional jump pin JX2 by setting a control register. - This pin cannot be used as a Serial Data input pin nor external conditional pin during hands-free mode.	Digital Serial data input /conditional input
21	SDIN2	I	**DSP Serial Data Input pin (*pulled-down*)** Supports MSB-justified 24 Bit/ LSB-justified 24 Bit, 20 Bit, and 16 Bit data format.	Digital Serial Data Input
22	SDIN1	I	**DSP Serial Data Input pin (*pulled-down*)** Supports MSB-justified 24 Bit/ LSB-justified 24 Bit, 20 Bit, and 16 Bit data format.	
23	DVSS	-	**Digital Ground pin 0 V**	Digital Power Supply
24	DVDD	-	**Digital Power Supply pin 3.3 V (typ)**	
25	$\overline{\text{INIT\_RESET}}$	I	**Initial Reset N pin (for initialization)** This is used to initialize the AK7750.This is also used to change CKS1 and CKS0 pin settings and to change XTI input frequency.	Reset
26	$\overline{\text{CK\_RESET}}$	I	**CK Reset N pin** This pin is used while $\overline{\text{S\_RESET}}$ is at "low" to change XTI input frequency and to change CKS2, CKS1, CKS0 settings. $\overline{\text{CK\_RESET}}$ bit in control register has similar function. When $\overline{\text{CK\_RESET}}$ bit is used, $\overline{\text{CK\_RESET}}$ pin must be commonly controlled with $\overline{\text{INIT\_RESET}}$ pin or it must be set to "high".	
27	$\overline{\text{S\_RESET}}$	I	**System Reset N pin**	
28	DVDD	-	**Digital Power Supply pin 3.3 V (typ)**	Digital Power Supply
29	DVSS	-	**Digital Ground pin 0 V**	Digital Power Supply
30	$\overline{\text{CS}}$ (EESEL="L")	I	**Chip Select pin for μC interface (*pulled-down*)** Leave open or connect to DVSS for normal operation When $\overline{\text{CS}}$ ="H", data on SI pin is not written and SO, RDY, DRDY pins become Hi-Z state. This function is not available at EESEL="H".	μC
	EESO (EESEL="H")	I	**EEPROM Serial Data Output pin (*pulled-down*)** Connect this pin to SO pin of AK6512C / 14C.	EEP
31	$\overline{\text{HFST}}$ (EESEL="L")	O	**Hands-Free Status pin** Normally at "H" but when an error occurs, it switches to "L" level.	μC
	$\overline{\text{HFST}}$ EEST (EESEL="H")	O	**Hands-Free Status pin / EEPROM write status pin** Normally at "H" but when an error occurs, it switches to "L". Level (SWEE bit = 0 in control register). When data read from EEPROM is complete, EEST changes from "L" to "H". The μC input interface is enabled (SWEE bit = 1 in control register).	μC /EEP

Pin NO.	Pin Name	I/O	Function	Pin Classification
32	RDY (EESEL="L")	O	**Data Write Ready pin for μC Interface (Hi-Z)** This pin becomes Hi-Z when $\overline{CS}$ ="H".	μC
	RDY/EESI (EESEL="H")	O	**Data Write Ready pin for uC interface/ EEPROM Serial Data Input Pin** Connect this pin to SI pin of AK6512C/14C. When data read from EEPROM is complete (EEST changes from "L" to "H"), this pin is automatically switched to the RDY pin function.	EEP/μC
33	XTO	O	**Oscillator Circuit Output pin** When a quartz crystal oscillator is used, it is connected between XTI pin and XTO pin. When an external clock is used, keep this pin open.	System Clock
34	XTI	I	**Oscillator Circuit Output pin** When a quartz crystal oscillator is used, it is connected between XTI pin and XTO pin. An external clock should be fed to this pin when no quartz crystal oscillator is used.	
35	DVSS	-	**Digital Ground pin 0 V**	Digital Power Supply
36	DVDD	-	**Digital Power Supply pin 3.3 V (typ)**	
37	$\overline{RQ}$	I	**Request N pin for μC Interface** μC interface is enabled when $\overline{RQ}$ ="L". Read operations during RUN mode should be made when $\overline{RQ}$ ="H". $\overline{RQ}$ should be kept "H" during the reset operation and when an external μC is not used.	μC
38	SO	O	**Serial Data Output pin for μC interface** This pin becomes Hi-Z state at $\overline{CS}$ ="H" when EESEL is at "L".	μC
39	SI	I	**Serial Data Input/Serial Data Output Control pin for μC interface** If no data is input to this pin or it is not used as Serial Data Output Control pin, set SI at "L".	μC
40	SCLK	I	**Serial Data Clock pin for μC interface** If no clock is used, set SCLK at "H".	μC
41	SMODE	I	**Slave / Master Mode Select pin** SMODE="L": Slave mode SMODE="H": Master mode	Control
42	CKSX	I	**Master Clock Select pin** CKSX="H":XTI, CKSX="L":BITCLK_I For normal operation, CKSX is set to "H".	
43	DVDD	-	**Digital Power Supply pin 3.3 V (typ)**	Digital Power Supply
44	DVSS	-	**Digital Ground pin 0 V**	
45	BVSS	-	**Ground pin (silicon substrate potential)** Tie this pin to AVSS.	Analog Power Supply

Pin NO.	Pin Name	I/O	Function	Pin Classification
46	CKS1	I	**Master Clock Set pin (*pulled-down*)**	Control
47	CKS0	I	**Master Clock Set pin (*pulled-down*)**	
48	TESTI1	I	**Test pin (*pulled-down*)** Tie this pin to DVSS.	Test
49	LFLT	-	**PLL RC component connect pin** A serially connected resistor (R=22kΩ) and capacitor (C=1.5nF) pair is connected to this pin (when PLL is not used at all, tie this pin to AVSS).	Analog Block
50	AVDD	-	**Analog Power Supply pin 3.3 V (typ).**	
51	AVSS	-	**Analog Ground pin 0 V (silicon substrate potential)**	
52	AVSS	-	**Analog Ground pin 0 V (silicon substrate potential)**	
53	AOUTR	O	**DAC R-ch Analog Output pin**	
54	AOUTL	O	**DAC L-ch Analog Output pin**	
55	AVDD	-	**Analog Power Supply pin 3.3 V (typ).**	
56	AVDD	-	**Analog Power Supply pin 3.3 V (typ).**	
57	VREFH	I	**Analog Reference Voltage Input pin** This pin is normally tied to AVDD. Connect Capacitors of 0.1 uF and 10 uF between this pin and VSS.	
58	VCOM	O	**Analog Common Voltage Output pin** Connect Capacitors of 0.1 uF and 10 uF between this pin and VSS. No external circuits should be connected to this pin.	
59	VREFL	I	**Analog Reference Voltage Input pin** Tie this pin to AVSS for normal operation.	
60	AVSS	-	**Analog Ground pin 0 V (silicon substrate potential)**	
61	AINR-	I	**ADC R-ch Analog Inverted Input pin**	
62	AINR+	I	**ADC R-ch Analog Non-Inverted Input pin**	
63	AINL-	I	**ADC L-ch Analog Inverted Input pin**	
64	AINL+	I	**ADC L-ch Analog Non-Inverted Input pin**	

Note) Digital input pins should not be kept open, except for pulled-down pins and BITCLK-I and LRCLK-I (EESEL="L") pins in master mode (pulled-down pins are kept open or connected to DVSS when they are not used).

Absolute maximum rating

(AVSS, BVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Item	Symbol	Min	Max	Units
Power supply voltage				
Analog (AVDD)	VA	-0.3	4.6	V
Digital (DVDD)	VD	-0.3	4.6	V
|AVSS(BVSS) – DVSS| Note1	ΔGND		0.3	V
Input current (Except for power supply pin)	IIN	-	±10	mA
Analog input voltage AINL+, AINL-, AINR+, AINR-, VRADH, VRADL, VRDAH, VRDAL	VINA	-0.3	VA+0.3	V
Digital input voltage	VIND	-0.3	VA+0.3	V
Operating ambient temperature	Ta	-40	85	°C
Storage temperature	Tstg	-65	150	°C

Note1) AVSS, BVSS, and DVSS must be same potential.

WARNING: Operation at or beyond these limits may result in permanent damage of the device. Normal operations are not guaranteed under these critical conditions in principle.

Recommended operating conditions

(AVSS, BVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Items		Min	Typ	Max	Units
Power supply voltage					
AVDD	VA	3.0	3.3	3.6	V
DVDD	VD	3.0	3.3	3.6	V
Reference voltage (VREF)					
VREFH Note 1)	VRH		VA		V
VREFL Note 2)	VRL		0.0		V

Note 1) VREFH normally connect with AVDD.

Note 2) VREFLnormally connect with AVSS.

Note: The analog input voltage and output voltage are proportional to the VREFL and VREFH voltages.

*) AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

Electric characteristics

(1) Analog characteristics

(Unless otherwise specified, Ta = 25°C; AVDD, DVDD = 3.3V; VREF=AVDD, VREFL=AVSS, BITCLK = 64 fs; Signal frequency 1 kHz; measuring frequency = 20 Hz to 20 kHz @48kHz; ADC with all differential inputs XTI=12.288MHz; CKSX="H"; SMODE="H");

	Parameter	Min	Typ	Max	Units
ADC Section	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) fs = 48kHz (-1dBFS) (note1)	80	91		dB
	Dynamic range fs = 48kHz (A filter) (note2)	90	98		dB
	S/N fs = 48kHz (A filter)	90	98		dB
	Inter-channel isolation (f =1 kHz) (note3)	90	105		dB
	DC accuracy				
	Inter-channel gain mismatching		0.1	0.3	dB
	Analog input				
	Input voltage (Note 4)	±1.22	±1.32	±1.42	Vp-p
	Input impedance (Note 5)		95		kΩ
DAC section	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) fs = 48kHz (0 dB)	78	86		dB
	Dynamic range fs = 48kHz(-60 dB) (A filter) (Note 2)	90	98		dB
	S/N fs = 48kHz (A filter)	90	98		dB
	Inter-channel isolation (f = 1 kHz)	90	105		dB
	DC accuracy				
	Inter-channel gain mismatching		0.2	0.5	dB
	Analog output				
	Output voltage (Note 6)	1.85	2.00	2.15	Vp-p
	Load resistance	10			kΩ
	Load capacitance			50	pF

Note: 1. When using single-ended inputs, this value is not guaranteed.
2. Indicates S/(N+D) when -60 dB signal is applied.
3. Inter-channel isolation between L-ch and R-ch at –1 dB FS signal input.
4. The full scale for analog input voltage (ΔAIN = (AIN+) - (AIN-)) can be represented by (±FS = ±(VREFH-VREFL) × 0.4).
5. Impedance is in inverse proportion to fs.
6. Full scale output voltage at VREFH = AVDD, VREFL = AVSS

(2) DC characteristics

(VDD=AVDD=DVDD=3.0~3.6V,Ta=-40°C~85°C)

Parameter	Symbol	Min	Typ	Max	Units
High level input voltage	VIH	80%VDD			V
Low level input voltage	VIL			20%VDD	V
High level output voltage Iout=-100μA	VOH	VDD-0.5			V
Low level output voltage Iout=100μA	VOL			0.5	V
Input leak current Note 1)	Iin			±10	μA
Input leak current(Pull down pin) Note 1)	Iid		22		μA
Input leak current XTI pin	Iix		50		μA

Note:

1. The pull down pins and XTI are not included.
2. The pull down pins (typ. 150kΩ) is as follows: 1, 2, 18, 19, 20, 21, 22, 30, 46, 47, and 48.

Note: Regarding the input/output levels in the text, the low level will be represented as "L" or 0, and the high level as "H" or 1.
In principle, "0" and "1" will be used to represent the bus functions (serial/parallel) such as registers.

(3) Current consumption

(AVDD=DVDD=3.0~3.6V, Ta=25°C; master clock (XTI)=12.288MHz=256fs[fs=48kHz],with PLL mode;

Power supply				
Parameter	**Min**	**Typ**	**Max**	**Units**
Power supply current note 1)				
Normal Speed				
a) AVDD		25	40	mA
b) DVDD		85	100	mA

note 1) DVDD current value may change, depending on the content of DSP program executed and clock frequency.

(4) Digital filter characteristics

Listed values are copied as reference data from the designed values and are not the guaranteed values. They are guaranteed-by-design after passing the IC tester's digital functional test..

4-1) ADC Section :

(Ta=25°C; AVDD,DVDD =3.0~3.6V; fs=48kHz; HPF=off Note 1)

parameter		Min	Typ	Max	Units
Pass band (±0.005dB) note2) (-6dB)	PB	0 -	 24.0	21.5 -	kHz kHz kHz
Stop band	SB	26.5			kHz
Pass band ripple Note 2)	PR			±0.005	dB
Stop band attenuation Note 3, 4)	SA	80			dB
Group delay distortion	ΔGD			0	μs
Group delay (Ts=1/fs)	GD		29.3		Ts

Note:
1. These frequencies scale with sampling frequency (fs). Not include HPF response.
2. The pass band is from DC to 21.5kHz when fs = 48kHz.
3. The stop band is from 26.5kHz to 3.0455MHz when fs = 48kHz.
4. When fs = 48kHz, the analog modulator samples analog input at 3.072MHz.
   The digital filter does not attenuate the input signal in the multiple bands (n x 3.072MHz ± 21.99kHz; n=0, 1, 2, 3...) of the sampling frequency.

4-2) DAC section
a) DAF bit = '0' (CONT6 D6)

(Ta=25°C; AVDD,DVDD =3.0~3.6V; fs=48kHz)

Parameter	Symbol	min	typ	max	Units
Digital filter					
Pass band ±0.08dB	PB	0		21.2	kHz
(-0.28dB) (Note 1)		-	21.7	-	kHz
(-6.0dB)		-	24.0	-	kHz
Stop band (Note 1)	SB	26.5			kHz
Pass band ripple	PR			±0.04	dB
Stop band attenuation	SA	47			dB
Group delay (Ts=1/fs) (Note 2)	GD	-	15		Ts
Digital filter+SCF					
Amplitude characteristics 0 to 20.0kHz			±0.5		dB

Note:
1. The pass band and stop band frequencies are proportional to "fs" (system sampling rate), and represents PB=0.4535fs(@-0.06dB) and SB=0.546fs, respectively.
2. The digital filter's delay is calculated as the time from setting 24 Bit data into the input register until an analog signal is output.

b) DAF bit = '1' (CONT6 D6)

(Ta=25°C; AVDD,DVDD =3.0~3.6V; fs=48kHz)

Parameter	Symbol	min	typ	max	Units
Digital filter					
Pass band ±0.02dB	PB	0		20.6	kHz
(-0.48dB) (Note 1)		-	21.7	-	kHz
(-6.0dB)		-	24.0	-	kHz
Stop band (Note 1)	SB	27.4			kHz
Pass band ripple	PR			±0.01	dB
Stop band attenuation	SA	59			dB
Group delay (Ts=1/fs) (Note 2)	GD	-	15		Ts
Digital filter+SCF					
Amplitude characteristics 0 to 20.0kHz			±0.5		dB

Note:
1. The pass band and stop band frequencies are proportional to "fs" (system sampling rate), and represents PB=0.4292fs(@-0.06dB) and SB=0.571fs, respectively.
2. The digital filter's delay is calculated as the time from setting 24 Bit data into the input register until an analog signal is output.

(5) Switching characteristics

1) System clock

(AVDD=DVDD=3.0 to 3.6V,Ta= -40°C to 85°C)

Parameter	Symbol	min	typ	max	Units
Maser clock(XTI) @CKSX="H"					
a) when a crystal oscillator is used (note 1)					
CKS[1:0]=0h	fXTI	-	11.2896 12.288	-	MHz
CKS[1:0]=1h	fXTI	-	16.9344 18.432	-	MHz
CKS[1:0]=2h	fXTI	-	22.5792 24.576	-	MHz
b)when an external clock is used (note 1)					
Duty factor (≤18.5MHz) (>18.5MHz)		40 45	50 50	60 55	% %
CKS[1:0]=0h (PLL operation range)	fXTI	11.0		12.33	MHz
CKS[1:0]=1h (PLL operation range)	fXTI	16.5		18.6	MHz
CKS[1:0]=2h (PLL operation range)	fXTI	22.0		24.66	MHz
CKS[1:0]=3h (PLL is not used)	fXTI	33.0		37.0	MHz
Clock rise time Clock fall time	tCR tCF			6 6	ns ns
LRCLK_I,LRCLK frequency note2)	fs	8	48	192	kHz
Slave mode: Clock rise time Slave mode: Clock fall time	tLR tLF			6 6	ns ns
BITCLK_I ,BITCLK frequency (@CKSX="H") (note3)	fBCLK	48		64	fs
Slave mode: high level width Slave mode: high level width	tBCLKH tBCLKL	34 34			ns ns
Slave mode: clock rise time Slave mode: clock fall time	tBR tBF			6 6	ns ns
BITCLK_I,BITCLK frequency (@CKSX="L",SMODE="L") (note 4)	fBCLK	-	64	-	fs
Duty factor		40	50	60	%
Slave mode: high level width Slave mode: high level width	tBCLKH tBCLKL	34 34			ns ns
Slave mode: clock rise time Slave mode: clock fall time	tBR tBF			6 6	ns ns

note1) CKS1=CKS[1].CKS[0]=CKS0

note2) LRCLK and sampling rate (fs) must be identical.

note3) 48 fs is used for slave mode (only 64 fs is available for hands-free mode)

note4) BITCLK-I or BITCLK is used as clock input. BITCLK must be precisely divided into 64 clocks in 1 fs time.

2) Reset

(AVDD=DVDD=3.0 to 3.6V,Ta=-40°C to 85°C)

Parameter	Symbol	min	typ	max	Units
$\overline{\text{INIT\_RESET}}$ note 1)	tRST	400			ns
$\overline{\text{CK\_RESET}}$	tRST	400			ns
$\overline{\text{S\_RESET}}$	tRST	400			ns

note1) At the power-on, it is OK to keep this pin to “L”. “H” transition must be made after the power-on and master clock is full running.

3) Audio Interface

(AVDD=DVDD=3.0 to 3.6V,Ta= Ta=-40°C to 85°C, CL=20pF)

Parameter	Symbol	min	typ	max	Units
Slave mode					
BITCLK frequency	fBCLK	48	64	64	fs
Delay time from BITCLK"↑“ to LRCLK note1)	tBLRD	40			ns
Delay time from LRCLK to BITCLK"↑" note1)	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			80	ns
Delay time from BITCLK to serial data output	tBSOD			80	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns
Master mode					
BITCLK frequency	fBCLK		64		fs
BITCLK duty factor			50		%
Delay time from BITCLK"↑" to LRCLK note1)	tBLRD	40			ns
Delay time from LRCLK to BITCLK"↑" note1)	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			80	ns
Delay time from BITCLK to serial data output	tBSOD			80	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns
PCM Interface mode (SF/LF)					
LRCLK frequency	fLRCK	8		48	kHz
BITCLK frequency	fBCLK		64		fs
BITCLK duty factor			50		%
Delay time from BITCLK"↑" to LRCLK note1)	tBLRD	40			ns
Delay time from LRCLK to BITCLK"↓" note1)	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			80	ns
Delay time from BITCLK to serial data output	tBSOD			80	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns
LRCLK high level width (SF)	tLCKKH		64		fs
LRCLK high level width (LF)	tLCLKH	300			ns
LRCLK low level width (LF)	tLCLKL	1200			ns

Note 1) this value is specified such that LRCLK edge and rising edge of BITCLK never overlap

4) Microprocessor Interface

(AVDD=DVDD=3.0 to 3.6V,Ta= Ta=-40°C to 85°C, CL=20pF)

Parameter	symbol	min	typ	max	Units
μC I/F signal					
$\overline{RQ}$ fall time	tWRF			8	ns
$\overline{RQ}$ rise time	tWRR			8	ns
SCLK fall time	tSF			8	ns
SCLK rise time	tSR			8	ns
SCLK low level width	tSCLKL	100			ns
SCLK high level width	tSCLKH	100			ns
μC → AK7750					
$\overline{S\_RESET}$ "↓" to $\overline{RQ}$ "↓"	tREW	200			ns
$\overline{RQ}$ "↑" to $\overline{S\_RESET}$ "↑" note1)	tWRE	200			ns
$\overline{RQ}$ high level width	tWRQH	200			ns
Time from $\overline{RQ}$ "↓" to SCLK"↓"	tWSC	200			ns
Time from SCLK"↑" to $\overline{RQ}$ "↑"	tSCW	12×tMCLK			ns
SI latch setup time	tSIS	100			ns
SI latch hold time	tSIH	100			ns
AK7750 → μC (DBUS output)					
SCLK"↑" to DRDY"↓"	tSDR			3×tMCLK	ns
Time from SI "↑" to DRDY"↓"	tSIDR			3×tMCLK	ns
SI high level width	tSIH	3×tMCLK			ns
Delay time from SCLK"↓" to SO output	tSOS			100	ns
Hold time from SCLK "↑" to SO outout	tSOH	100			ns
AK7750 → μC (RAM DATA read-out)					
SI latch setup time(SI="H")	tRSISH	30			ns
SI latch setup time(SI="L")	tRSISL	30			ns
SI latch hold time	tRSIH	30			ns
Delay time from SCLK "↓" to SO output	tSOD			100	ns
AK7750 → μC (CRC result-out) note2)					
Delay time from $\overline{RQ}$ "↑" to SO output	tRSOC			200	ns
Delay tiem from $\overline{RQ}$ "↓" to SO output note3)	tFSOD	50			ns
$\overline{CS}$ **(EESEL="L" or open)**					
$\overline{CS}$ fall time	tCSF			8	ns
$\overline{CS}$ rise time	tCSR			8	ns
Time from $\overline{S\_RESET}$ "↓" to $\overline{CS}$ "↓"	tWRCS	400			ns
Time from $\overline{CS}$ "↑" to $\overline{S\_RESET}$ "↑"	tWCSR	400			ns
$\overline{CS}$ high level width	tWCSH	800			ns
Time from $\overline{CS}$ "↓" to $\overline{RQ}$ "↓"	tWCSRQ	400			ns
Time from $\overline{RQ}$ "↑" to $\overline{CS}$ "↑"	tWRQCS	400			ns
$\overline{CS}$ "↓" to SO,RDY,DRDY Hi-Z release (RL=10kΩ)	tCSHR			600	ns
$\overline{CS}$ "↑" to SO,RDY,DRDY Hi-Z (RL=10kΩ)	tCSHS			600	ns
EEPROM → AK7750(EESEL="H")					
EESO latch setup time	tEESOS	100			ns
EESO latch hold time	tEESOH	100			ns

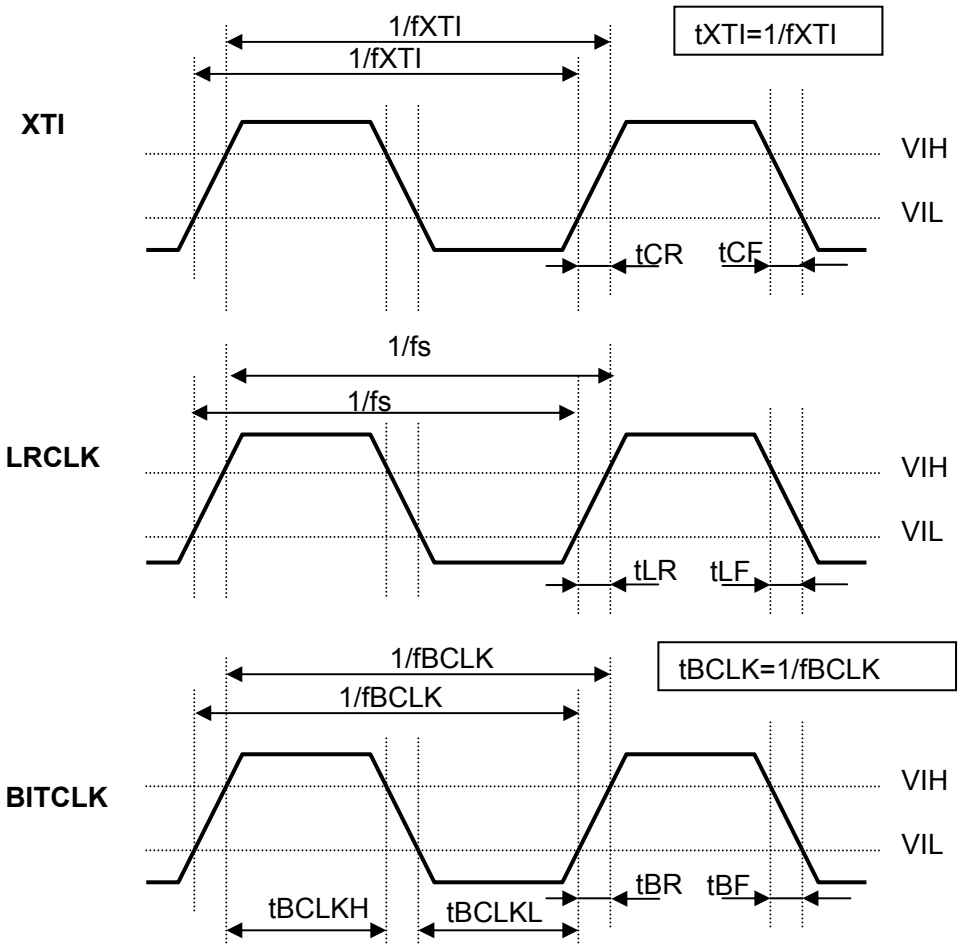
Note1: Excluding an external conditional jump at reset.

Note2: This is a case where the remainder of serial data D(x) ,divided by the Generator Polynomial G (x) is equal to R (x). SO becomes "H".

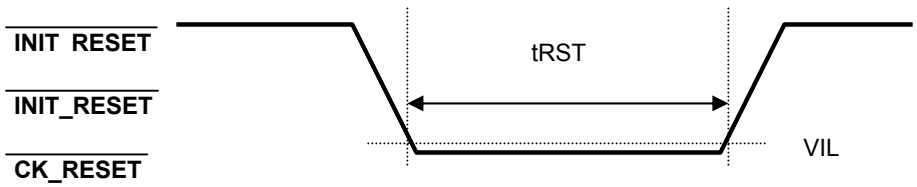
Note3: This means that data must be taken into the microprocessor 50 ns earlier than the falling edge of $\overline{RQ}$ (this applies when no read-out is made during RUN).

(6) Timing waveform

6-1) System clock

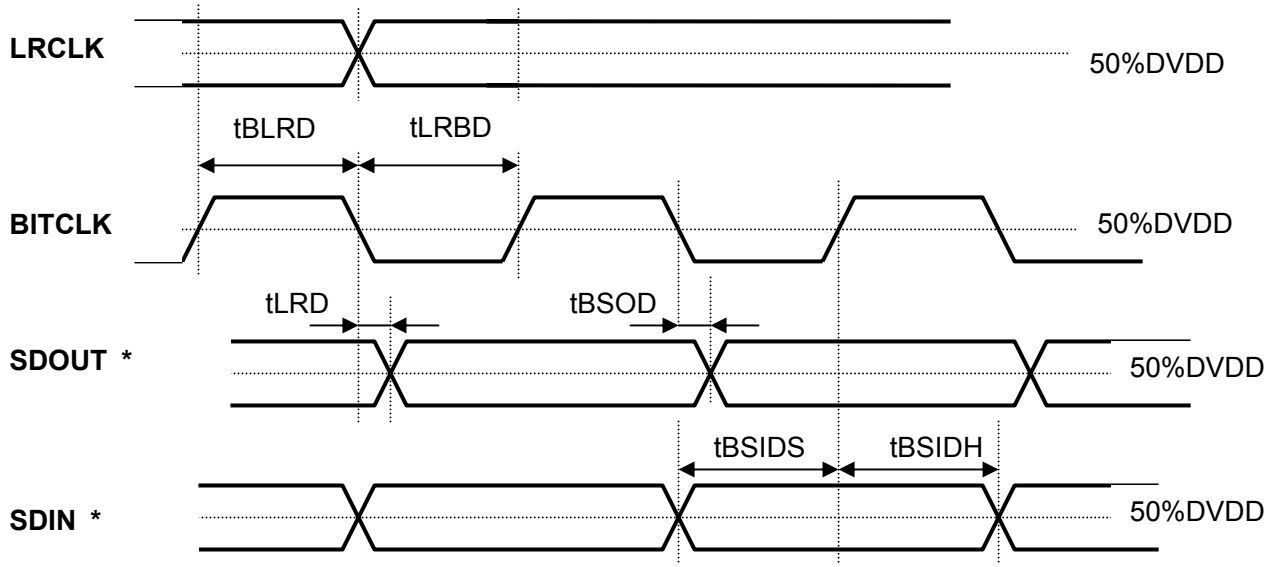


6-2) Reset



6-3) Audio Interface

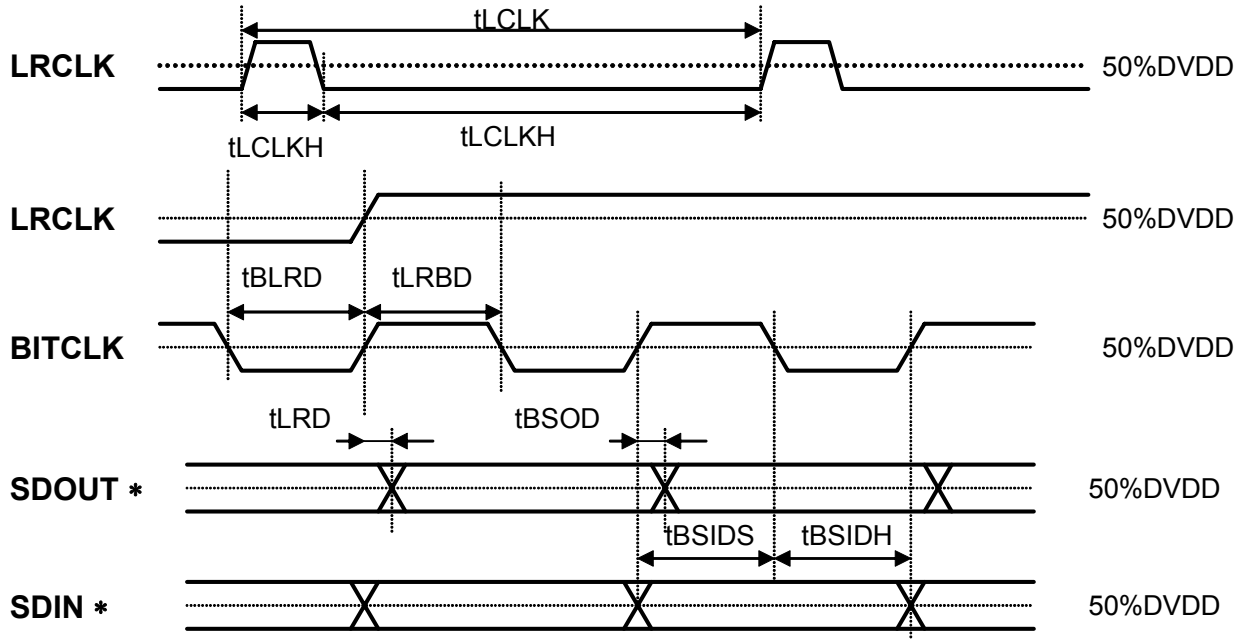
a) Standard/I2S Compatible Format



SDIN *=SDIN1,SDIN2,SDIN3,SDIN4,SDIN5A

SDOUT *=SDOUT1,SDOUT2,SDOUT3,SDOUT4

b) PCM Format

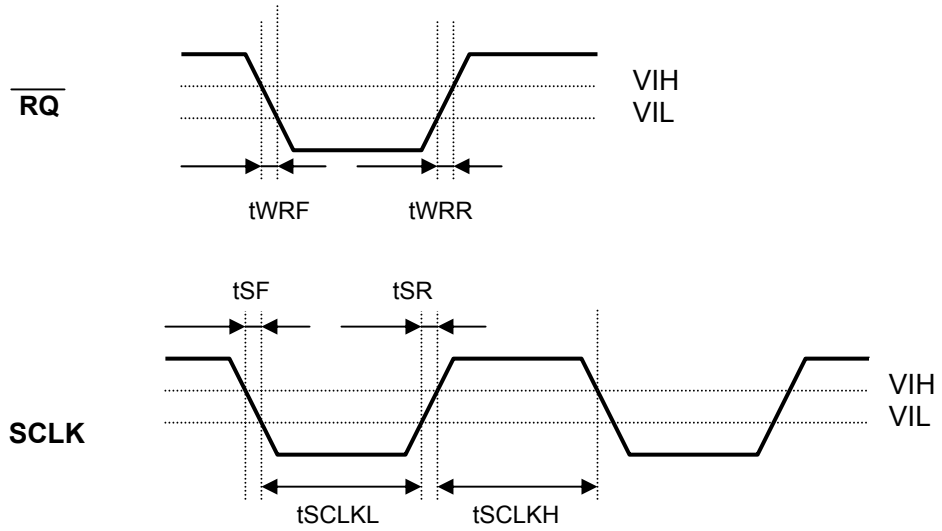


SDIN *=SDIN1,SDIN2,SDIN3,SDIN4,SDIN5A

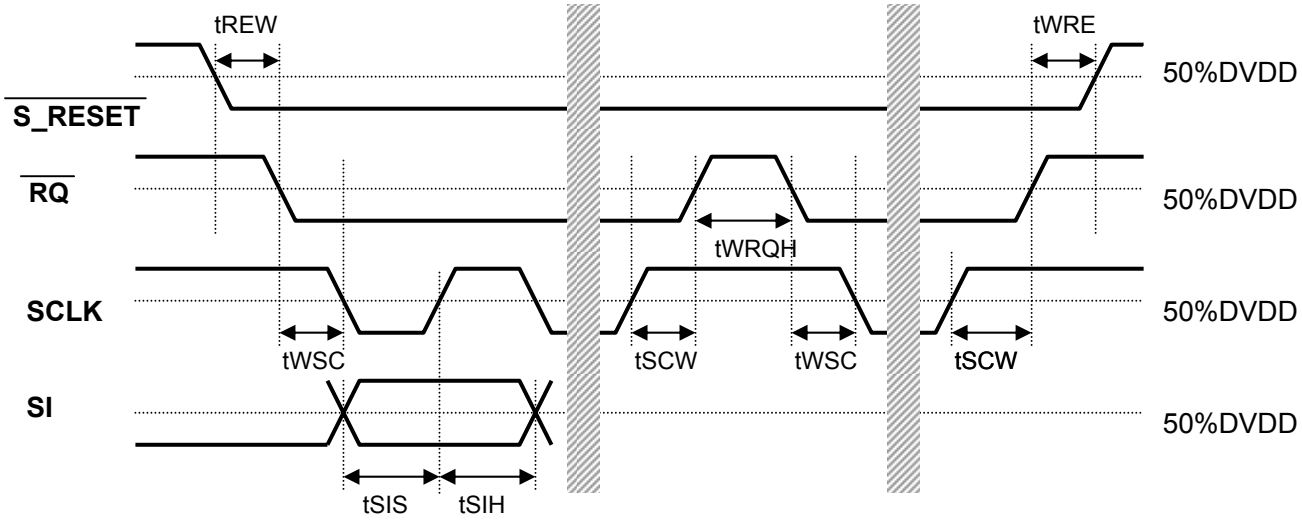
SDOUT*=SDOUT1,SDOUT2,SDOUT3,SDOUT4A

6-4) μC Interface

■ μC interface signal



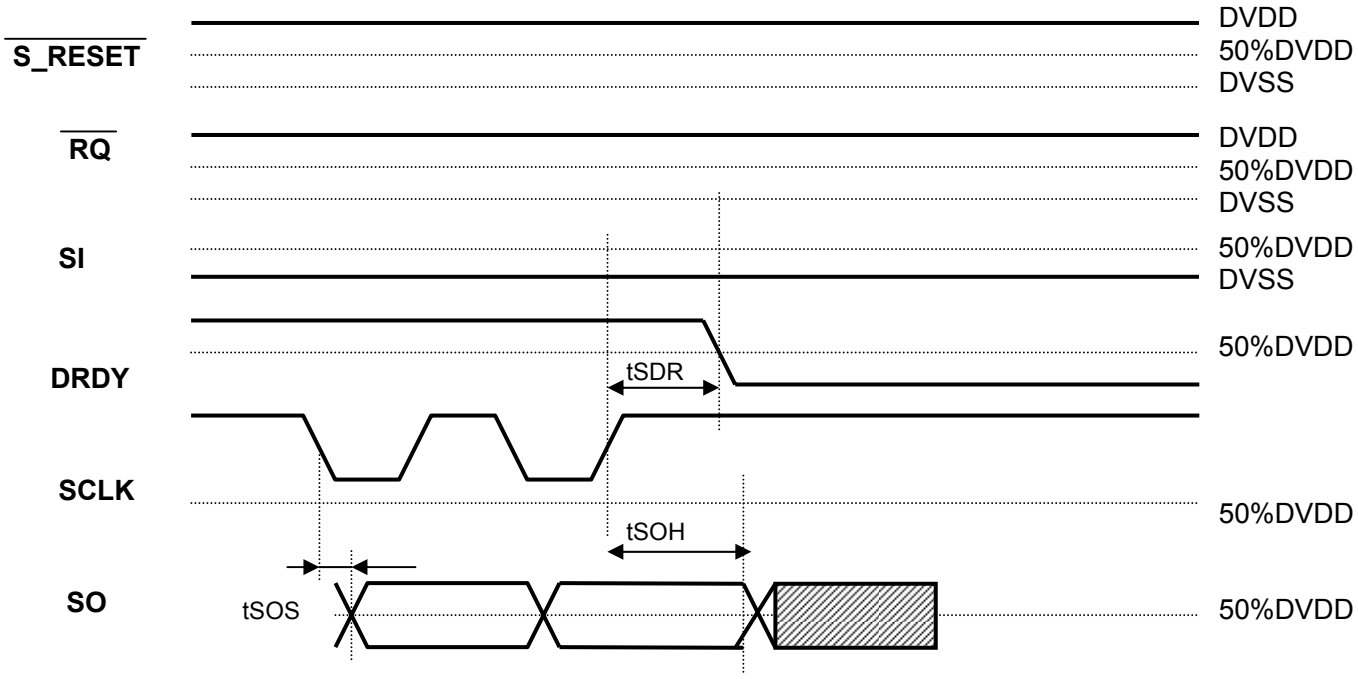
■ μC → AK7750



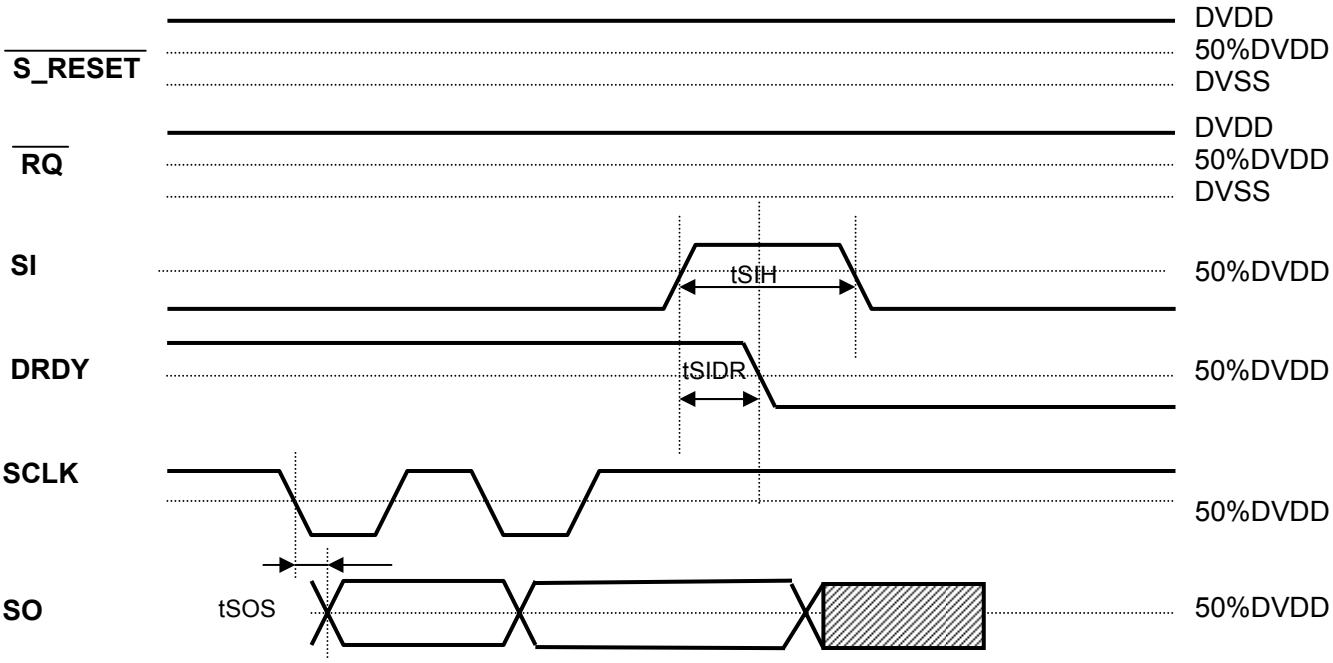
Note: Timing is identical in RUN mode except that $\overline{\text{S\_RESET}}$ becomes “H.

■ AK7750 → μC(DBUS output)

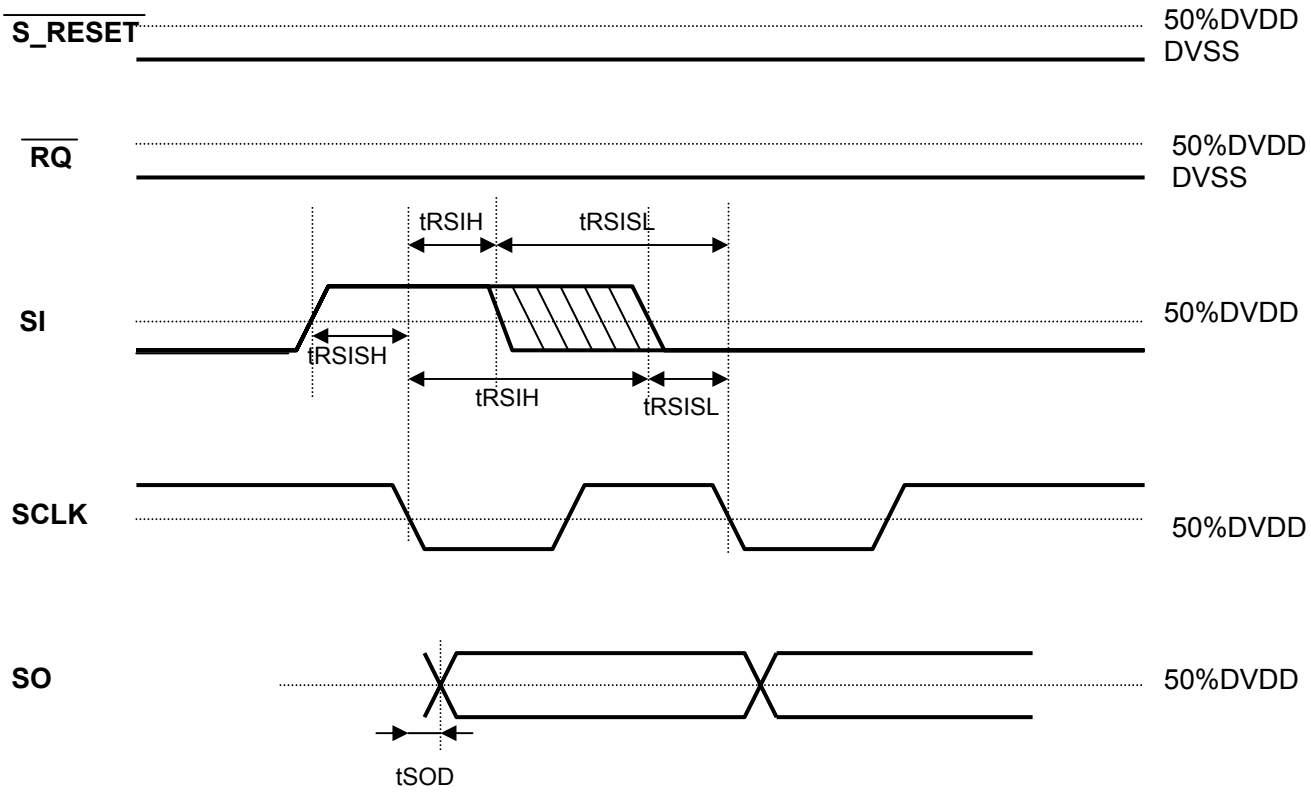
1) DBUS 24bit output



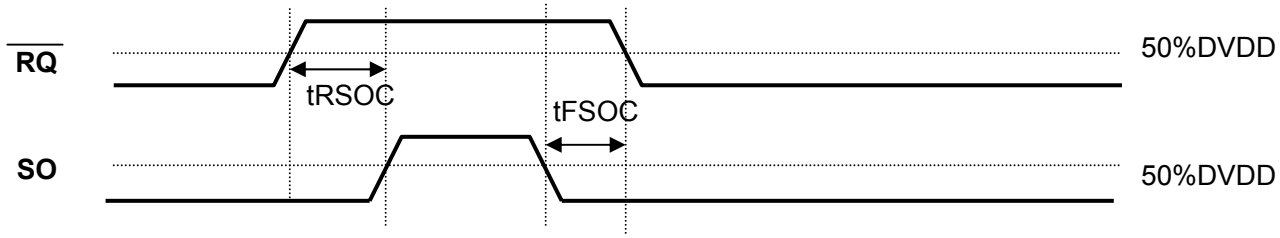
2) DBUS under 24 Bit output (SI is used)



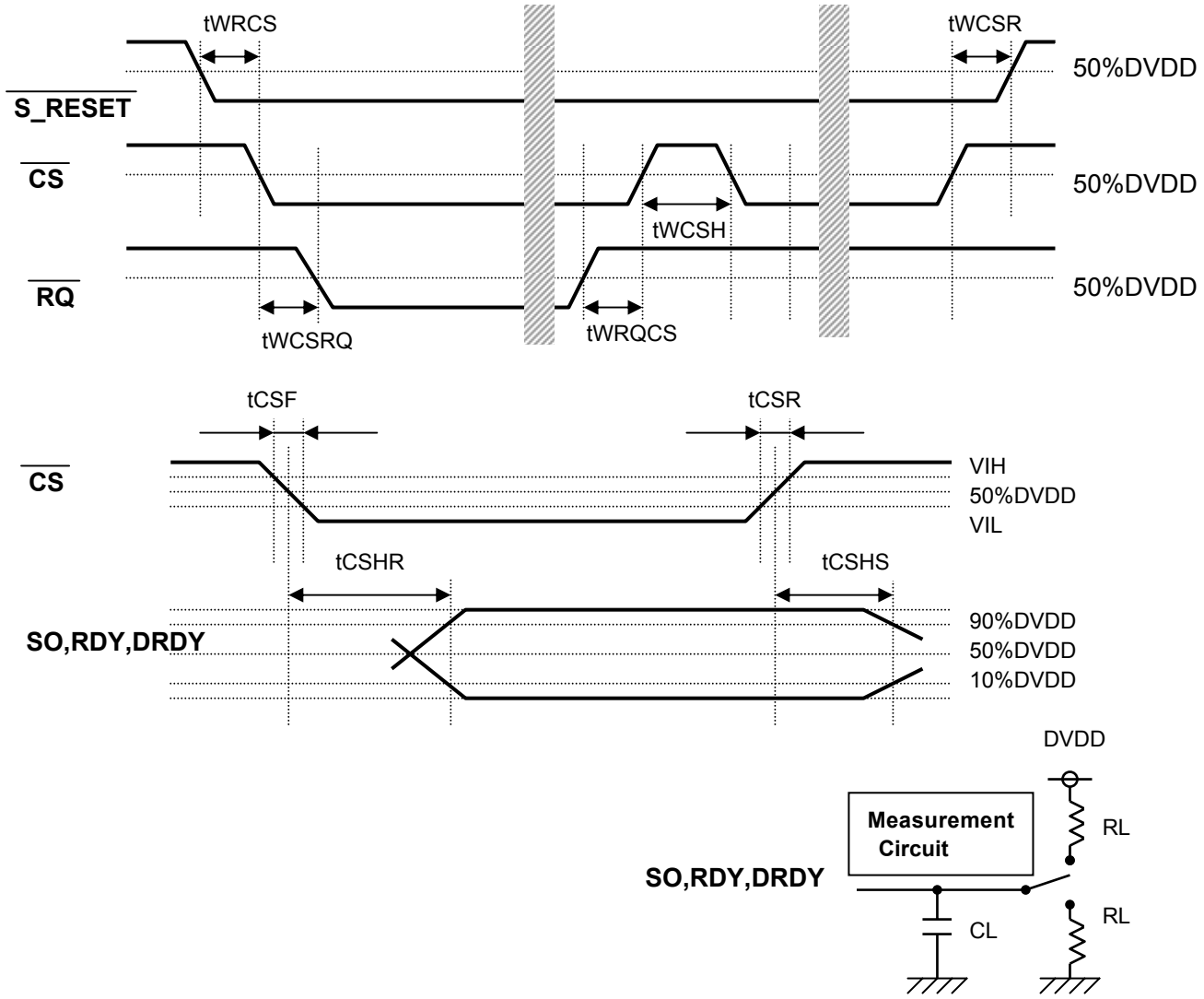
■ AK7750 → μC(RAM DATA read-out)



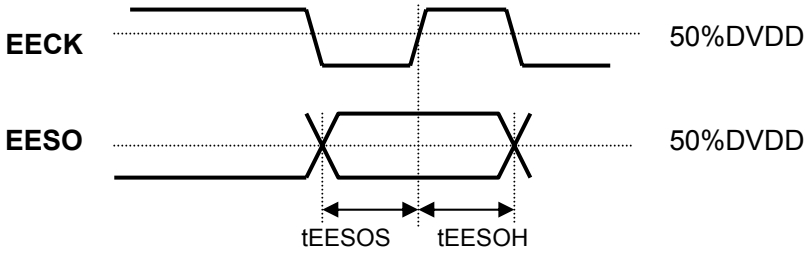
■ AK7750 → μC(CRC check: remainder of D (x) / G (x)) = R (x))



■ $\overline{CS}$ (EESEL="L" or OPEN)



■ EEPROM → AK7750



Functional Description

(1) Various Pin Setting

1) CKS1,CKS0 : Master Clock (MCLK) Set pin
CKSX : Master Clock Select pin

The AK7750 usually operates using a 36.864 MHz Master Clock (MCLK) (or 33.8688 MHz). When CKSX = "H", the XTI input clock is selected by the CKS1 and CKS0 pins.

In addition to the normal use described above, the AK7750 can also operate using BITCLK-I or BITCLK as a master clock input during slave mode operation (SMODE = "L") by setting CKSX = "L".
Since the AK7750 is running in slave mode instead of master mode, certain modes may not be available since the AK7750 modes are restricted by the incoming audio clock.

■ Mode setting by CKSX, CKS1, CKS0 pins
a) XTI selection at CKSX = "H"

fs: sampling frequency

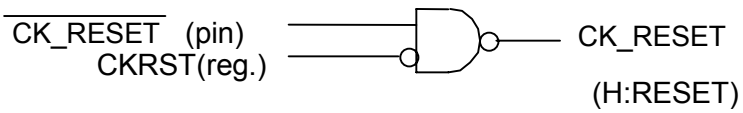
XTI	CKS	XTI			Internal
mode	[1:0]	XTI	Fs:48kHz series	fs:44.1kHzseries	PLL
0	0h	MCLK/3	12.288MHz	11.2896MHz	use
1	1h	MCLK/2	18.432MHz	16.9344MHz	use
2	2h	MCLK*(2/3)	24.576MHz	22.5792MHz	use
3	3h	MCLK	36.864MHz	33.8688MHz	not use

note) CKS1 = CKS[1],CKS0 = CKS[0]
A crystal oscillator cannot be used in XTI mode 3.
For hands-free mode, use fs = 48 KHz.

Sample-rate setting is performed using the (CONT0) control register.
Usually XTI modes 0 and 1 are used (XTI mode 0 is selected when CKS1 and CKS0 pins are left open).
XTI mode 2 is only used when a 512 fs clock is available externally. XTI mode 3 is used when the PLL is not used.

To change clock settings after power on (CKS1, CKS0 and CKSX),an initial reset ($\overline{\text{INIT\_RESET}}$ = "L", $\overline{\text{S\_RESET}}$ = "L"), or during a clock reset ($\overline{\text{CK\_RESET}}$ = "L", $\overline{\text{S\_RESET}}$ = "L") should be performed. Since the PLL circuit and internal clocks are controlled by CKS1, CKS0 and CKSX pins, an erroneous operation may occur if any pin setting changes occur under any conditions other than those described above (same conditions apply when changing the input for XTI).

A reset can be performed using either the pin $\overline{\text{CK\_RESET}}$ or the CKRST bit (CONT0:D1) in control register. When using the register RESET, the $\overline{\text{CK\_RESET}}$ pin should be set to "H" or should be linked together with $\overline{\text{INIT\_RESET}}$ pin.



$\overline{\text{CK\_RESET}}$ (pin) and CKRST(reg.) relation

b) BITCLK(_I) Selection at CKSX = "L" (SMODE = "L")

EESEL="L" fs: sampling frequency

BCK mode	CKS [1:0]	BITCLK_I	(64fs)	@SMODE="L"		Internal PLL
		BITCLK_I	sample rate	fs:48kHz series	fs:44.1kHz series	
0	0h	MCLK/12	standard speed	3.072MHz	2.8224MHz	use
1	1h	MCLK/6	double speed	6.144MHz	5.6448MHz	use
2	2h	MCLK/3	4X speed	12.288MHz	11.2896MHz	use
3	3h	MCLK/72	fs=8kHz	512kHz	-	use

EESEL="H"

BCK mode	CKS [1:0]	BITCLK	(64fs)	@SMODE="L"		Internal PLL
		BITCLK	sample rate	fs:48kHz series	fs:44.1kHz series	
0	0h	MCLK/12	standard speed	3.072MHz	2.8224MHz	use
1	1h	MCLK/6	double speed	6.144MHz	5.6448MHz	use
2	2h	MCLK/3	4x speed	12.288MHz	11.2896MHz	use
3	3h	MCLK/72	fs=8kHz	512kHz	-	use

note1) CKS1 = CKS[1],CKS0 = CKS[0]
note2)BITCLK_I clock is selected at EESEL = "L" and BITCLK clock is selected at EESEL = "H".
note3) Hands-free mode is available only when BCK mode 3 is selected.

BCK modes are also used to generate internal master clock other than used as a primary bit clock. Therefore some limitations exist when to use BITCLK (_I) (for details, please refer to item b) of the Clock Source description).

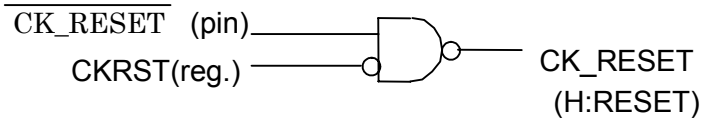
BCK mode is not available when the device operates at master mode.

The sampling rate is fixed by BCK mode that is not affected by the speed setting (standard speed, double speed, and 4x speed) of the control register.

Both of internal ADC and DAC are not available when BCK mode 1or 2 is selected. PSAD(D7) bit in CONT2 register and PSCODEC(D7) bit in the CONT6 register should be set to "1".

Please set XTI = "L" when XTI is not used at all.

When to switch setting of CKS1, CKS0 and CKSX after the power-on, it should be done either during the initial reset ($\overline{\text{INIT\_RESET}}$ = "L", $\overline{\text{S\_RESET}}$ = "L") or during the clock reset ($\overline{\text{CK\_RESET}}$ = "L", $\overline{\text{S\_RESET}}$ = "L"). Since PLL circuit and internal clocks are controlled by CKS1, CKS0 and CKSX pins, an erroneous operation may occur if any pin set change is taken place under any conditions other than those described above (same conditions apply when to change input BITCLK(_I)).
Instead of $\overline{\text{CK\_RESET}}$, D1 bit in control register (CONT0: D1) can be used. In this case, $\overline{\text{CK\_RESET}}$ pin should be set to "H" or should be linked together with $\overline{\text{INIT\_RESET}}$ pin.



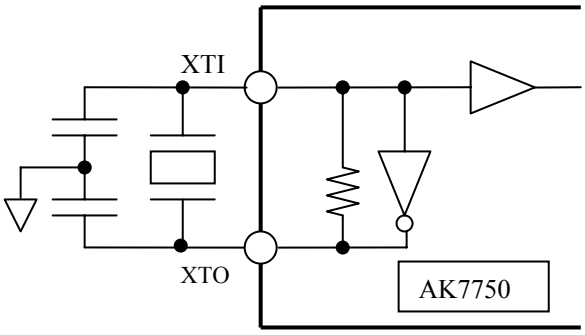
$\overline{\text{CK\_RESET}}$ (pin) and CKRST(reg.) relation

■ **Clock Sources**

a) XTI selection at CKSX = "H".

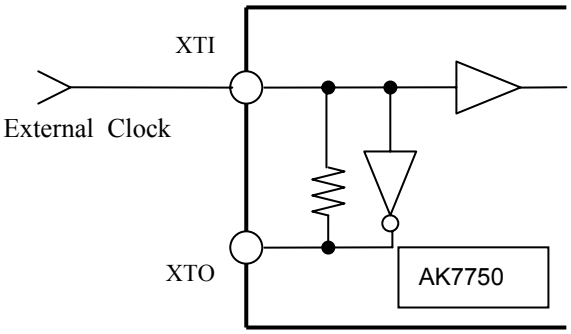
Clocks can be supplied to the AK7750's XTI pin as follows:

When one of the XTI Modes 0,1 and 2 is used, either connect a proper crystal oscillator between XTI and XTO pins or feed a clock of proper frequency to the XTI pin.



When a crystal oscillator is used: XTI Modes 0,1,2

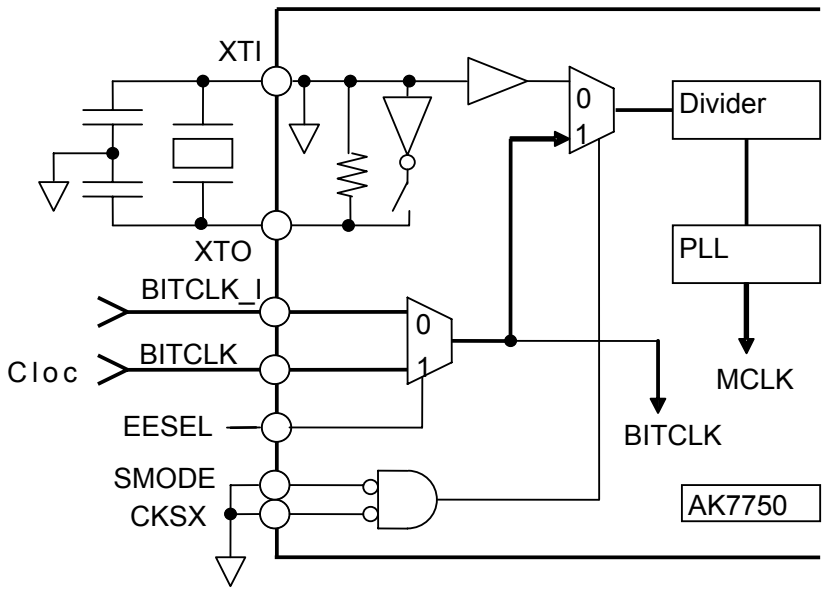
When XTI Mode 3 is used, feed a clock of proper frequency to the XTI pin.



When an external clock is used : XTI Mode 3

b) BITCLK(_I) Selection at CKSX = "L" (`SMODE="L")

BCK Modes 0,1,2 are used when bit clock (BITCLK_I,BITCLK) is used instead of XTI. A clock fed on the BITCLK-I pin is directly frequency-multiplied by the PLL and a master clock (MCLK) is generated.



Internal connection image diagram

Input on BITCLK(_I) pin a divided-by-64 clock of the LRCLK(_I) (64fs).
(BITCLK(_I) must be in synchronized with LRCLK (_I)).

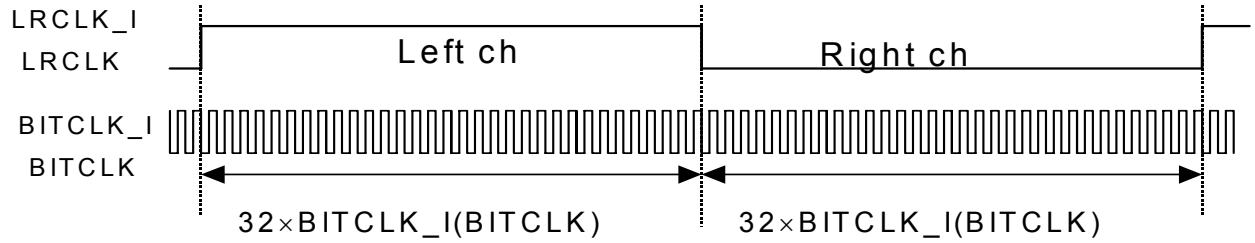


Figure BITCLK (-I) and LRCLK (-I) relation (BITCLK (-I) = LRCLK (-I) / 64)

■ Modes vs. PLL Relation

a) XTI Selection at CKSX = "H"

In the AK7750, the internal master clock MCLK usually runs at 36.864 MHz max. as shown below.

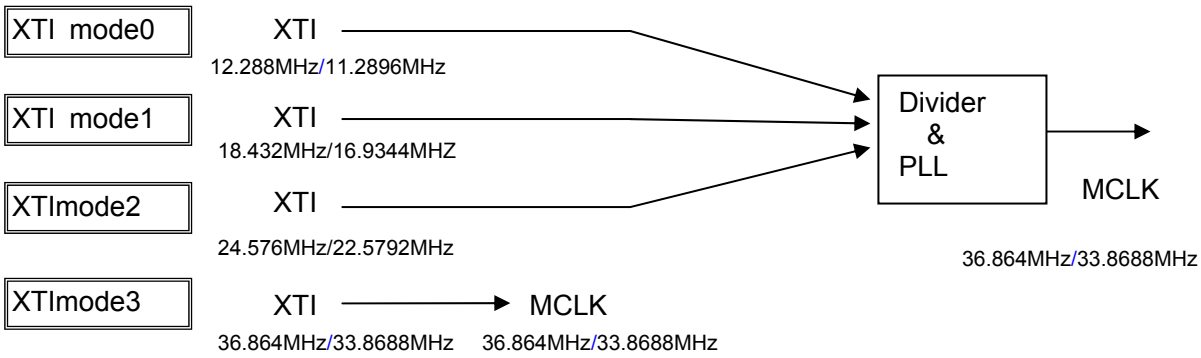


Figure Mode Set vs. MCLK (internal master clock) relation

b) BITCLK(_I) Selection at CKSX = "L" (@SMODE = "L")

In the AK7750, the internal master clock MCLK usually runs at 38.864 MHz max. as shown below.

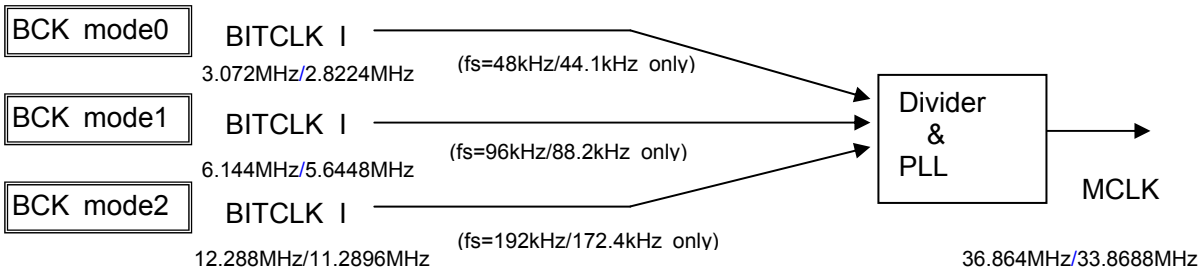


Figure Mode Set vs. MCLK (internal master clock) relation

2) SMODE: Slave, Master Mode Select pin

Set the input /output of LRCLK and BITCLK.

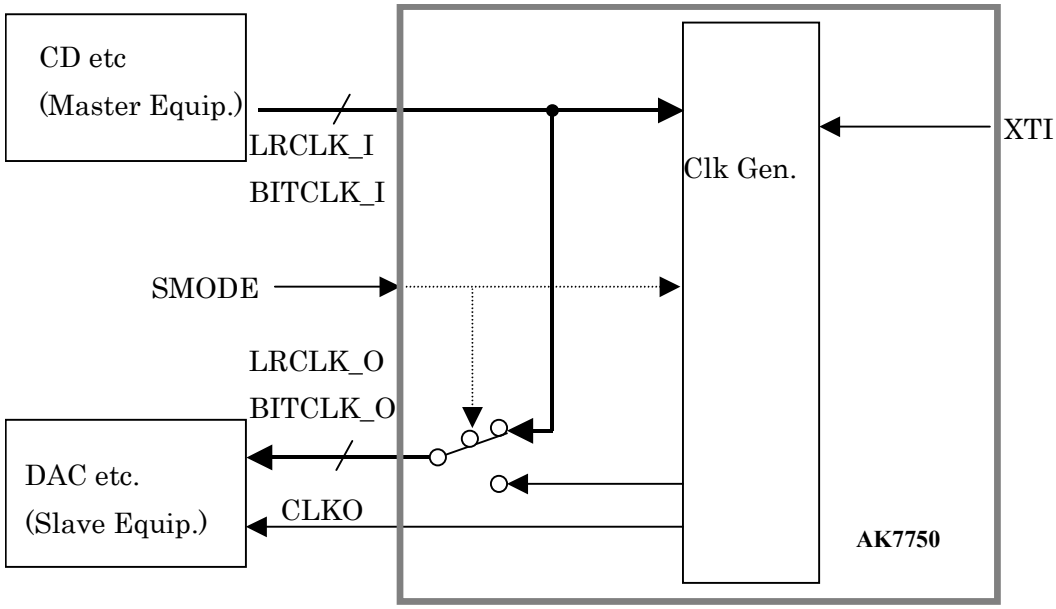
a) Slave Mode : SMODE = "L "

- **EESEL = " L "**

  LRCLK_I (1fs) & BITCLK_I (64fs) become inputs.

  LRCLK_I,BITCLK_I are directly output on LRCLK_O and BITCLK_O respectively. Output can be set via a control register.

  Note) 48fs can be input on BITCLK_I pin for modes other than hands-free mode or when CKSX = "L" (64fs corresponds to hands-free mode and CKSX = "L").



  At CKSX = "H", XTI and LRCLK_I must be synchronized, but need not be in phase.

  At CKSX = "L", BITCLK_I and LRCLK_I must be synchronized.

- **EESEL = "H"**

  LRCLK (1fs) and BITCLK (64fs) become inputs.

  At CKSX = "H", XTI and LRCLK must be synchronized, but need not be in phase.

  At CKSX = "L", BITCLK and LRCLK must be synchronized.

  Note) 48fs can be input on BITCLK pin except in hands-free mode (64fs corresponds to hands-free mode).

b) Master Mode: SMODE = "H"

Master mode requires a clock input to XTI.

When a clock is applied to the XTI input, LRCLK (LRCLK_O) and BITCLK (BITCLK_O) are automatically generated by an XTI-synchronized internal counter.

No output is available on LRCLK (LRCLK_O) and BITCLK (BITCLK_O) pins during an initial reset ($\overline{\text{INIT\_RESET}}$ = "L") or a system reset (INIT_RESET = "H" and $\overline{\text{S\_RESET}}$ = "L").

- **EESEL = "L"**

  LRCLK_O(1fs) and BITCLK_O(64fs) are output.

  When LRCLK_I and BITCLK_I pins are not connected to any external circuit, these pins should be tied low ("L" level, (DVSS)).

  When the AK7750 is used in Analog-to-Analog fashion and when LRCLK_O and BITCLK_O are not required (SDIN and SDOUT pins are not used), BITCLK_O and LRCLK_O can be programmed by setting a control register.

- **EESEL = "H"**

  LRCLK (1fs) and BITCLK (64fs) are output.

  When the AK7750 is used in Analog-to-Analog fashion and when LRCLK and BITCLK are not required (SDIN and SDOUT pins are not used), BITCLK_O and LRCLK_O can be programmed by setting a control register.

c) SMODE Pin Switching

Setting the SMODE pin function after power-on should be performed either during an initial reset ($\overline{\text{INIT\_RESET}}$ = "L" and $\overline{\text{S\_RESET}}$ = "L"), or during a clock reset ($\overline{\text{CK\_RESET}}$ = "L" and $\overline{\text{S\_RESET}}$ = "L").

Since switching between Slave and Master modes is controlled by the SMODE pin, an erroneous operation may occur if pin set changes take place under any conditions other than those described above.

In Slave mode operation, internal clock phase-synchronization is performed at the release of system reset (from $\overline{\text{S\_RESET}}$ = "L" to "H"). It should be noted that switching to Slave mode in the middle of an operation may cause an erroneous results.

d) Corresponding Table of SMODE, CKSX and EESEL pins

CKSX	SMODE	EESEL	selected CLK	note
"H"	"L"	"L"	XTI	
"H"	"H"	"L"	XTI	
"H"	"L"	"H"	XTI	
"H"	"H"	"H"	XTI	
"L"	"L"	"L"	BITCLK_I	
"L"	"L"	"H"	BITCLK	
"L"	"H"	"L"	N/A	not available
"L"	"H"	"H"	N/A	not available

(2) Control Register Settings

In the AK7750, control registers are programmed via the microprocessor interface. There are 8 registers in total. Each register is configured with 7 bits, but SCLK always requires 16 bit data clocks (8 bits for Command Code and 8 bits for DATA).

The Register configuration is listed below. Each control register value is set when D0 is written.
Control register writes are performed during a system reset ($\overline{\text{S\_RESET}}$ = "L"), but reads can be performed at any time during normal chip operation.

Control registers are initialized by an $\overline{\text{INIT\_RESET}}$ = "L". They are not initialized by a system reset ($\overline{\text{S\_RESET}}$ = "L").

TEST: for testing purpose (set to "0")
X: The value "0" must be set with a write operation. Failure to do say will result in an unknown value during a read operation.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
W	R										
60h	70h	CONT0	DFS2	DFS1]	DFS0	DIF2	DIF1	DIF0	CKRST	X	0000_000x
62h	72h	CONT1	DATARAM	RM	BANK1	BANK0	CMP_N	SS1	SS0	X	0000_000x
64h	74h	CONT2	PSAD	OUT3E_N	OUT2E_N	OUT1E_N	NRDY	TEST	TEST	X	0000_000x
66h	76h	CONT3	SWJX2	SWJX1	SWJX0_N	SWQ4	SWIA	SWQD	SWEE	X	0000_000x
68h	78h	CONT4	TEST	CLKS1	CLKS0	CLKE_N	BLCKE_N	OUT4E	TEST	X	0000_000x
6Ah	7Ah	CONT5	HF_RST_N	HF	PID	SSDIN4	SSDIN3	OP1	OP0	X	0000_000x
6Ch	7Ch	CONT6	PSCODEC	DAF	SF1	SF0	SMUTE	TEST	TEST (PLLSTBY)	X	0000_000x
-	DCh	CONT7	SRRQ	CRCL	TEST	TEST	TEST	TEST	TEST	X	0000_000x

Note) Do not write other data values or addresses.

1. In order to prevent erroneous operation, write to the CONT0 and CONT5 registers only during a system reset ($\overline{\text{S\_RESET}}$ = "L").
2. It is recommended that CONT1 ~ CONT4, CONT6 ~ CONT7 registers are also only written to at a system reset ($\overline{\text{S\_RESET}}$ ="L").
3. TEST means for testing, and 0 should be written.
4. Default means an initialized value, to which register is initialized by $\overline{\text{INIT\_RESET}}$ = "L".

1) CONT0 : Sampling Rate Selection and Interface Types

writing is possible only at a system reset ($\overline{\text{S\_RESET}}$ = "L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
60h	70h	CONT0	DFS2	DFS1	DFS0	DIF2	DIF1	DIF0	CKRST	X	0000_000x

① D7, D6, D5: DFS [2:0] Sampling Rate Set

fs: sampling frequency

DFS mode	DFS [2:0]	fs(kHz)	DSP STEP	AD operation	DA operation
0	0h	48(,44.1)	768	○	○
1	1h	96(,88.2)	384	×	×
2	2h	192(,176.4)	192	×	×
3	3h	32(,29.4)	1152	○	○
4	7h	8	4608	○	○

note1) mode and sampling rate selection are only valid in modes 0 ~ 4.
note2) when selecting modes 1 or 2, "1" must be set at PSAD (D7) bit of CONT2 register and at PSCODEC (D7) bit of CONT6 register. When CKSK is set to "L", operation follows the CSK0 and CSK1 setting.

② D4, D3, D2: DIF [2:0] Input Mode Selection of SDIN1, SDIN2, SDIN3H, SDIN4, SDIN5A

DIF mode	SMODE	DIF[2]	DIF[1]	DIF[0]	
0	"L","H"	0	0	0	MSB-justified format(24bit)
1	"L","H"	0	0	1	LSB-justified format(24bit
2	"L","H"	0	1	0	LSB-justified format(20bit)
3	"L","H"	0	1	1	LSB-justified format(16bit)
4	"L","H"	1	0	0	I2S format(24bit)
	"L"	1	0	1	PCM1 SF(64fs only)
	"L"	1	1	0	PCM2 LF(64fs only)

③ D1:CKRST

0: operating condition
1: internal clock reset

When CKS2, CKS1, CKS0 and SMODE pins are switched or when the XTI input clock is changed, the new settings will take effect after toggling the CKRST from "1" to "0" (similar to $\overline{\text{CK\_RESET}}$ pin).

④ D1: Set "0"

note) under-lined values in ① ~ ③ above indicate the default values

2) CONT1: RAM control

This register should be changed only during a system reset ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
62h	72h	CONT1	DATARAM	RM	BANK1	BANK0	CMP_N	SS1	SS0	X	0000_000x

① D7:DATARAM DATARAM addressing mode selector

0: Ring addressing mode

1: Linear addressing mode

DATARAM is 256-words x 24-bits and has 2 addressing pointers (DP0, DP1).

Ring addressing mode: The starting address increments by 1 every sample period.

Linear addressing mode: The starting address is always the same, DP0 = 00h and DP1 = 80h.

② D6:RM: Decompress bit mode

0: SIGN bit

1: Random data

When either Data Compression or Data Expansion mode is selected (CMP-N (D3) = "0"), data for the lower bits where no data exists at the data expansion is selectable. When it is "0", the sign bit is filled in and when it is "0", the M-series random number is filled in.

③ D5,D4:BANK[1:0] DLRAM Setting

Mode	BANK1	BANK0	Memory
0	0	0	24bit 1kword(RAM A)
1	0	1	16bit 2kword(RAM A),24bit 1kword(RAM B)
2	1	0	24bit 1kword(RAM A),16bit 2kword(RAM B)
3	1	1	16bit 4kword(RAM A)

note) When a hands-free function is used, set the DLRAM at mode0, which allocates the memory for hands-free processing.

At DLRAM mode3, both Pointers 0 & 1 can be used. With DLRAM modes0, 1 and 2, Pointer 0 is allocated to RAM A and Pointer 1 is allocated to RAM B.

④ D3:CMP_N 16bitDLRAM Compress & Decompress selector

When mode 1,2 or 3 is selected, this register can turn ON or OFF the compress/decompress function.

0 : Compression / Expansion ON

1 : Compression / Expansion OFF

When both compression and expansion are enabled (ON), the upper 23 bit data on DBUS is compressed to 15 bit data and it is written into DLRAM.

In read mode, the 15 bit data is expanded and the resulting data is output on DBUS.

Lower bit setting during data expansion follows as is set by D6 : RM.

With this data compression, 23 bit equivalent Dynamic Range and 15 bit equivalent S/N + D are obtained.

When both compression and expansion are disabled (OFF), the upper 16 bit data on DBUS is directly written into or read out of DLRAM. During the read operation, the lower 16 bit returns to DBUS a value of 0000h.

⑤ D2,D1:SS[1:0] DLRAM setting of sampling timing (only for RAM A)

Mode	SS1	SS0	RAM A mode selected by BANK[1:0]
0	0	0	Update every sampling time
1	0	1	Update every 2 sampling time
2	1	0	Update every 4 sampling time
3	1	1	Update every 8 sampling time

Note) When modes 1,2 or 3 are selected, aliasing will occur.

⑥ D0: set to "0"

Note) Underlines "_" mean default setting.

3) CONT2: ADC control, Serial output set and others

Change this register only during a system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
64h	74h	CONT2	PSAD	OUT3E_N	OUT2E_N	OUT1E_N	TEST	TEST	TEST	X	0000_000x

① **D7:PSAD**

0:Normal operation
1:ADC power save

When the ADC is not used, it is put into power-save mode by setting D7 = 1 (SDATA digital output of ADC becomes 00 0000h). In a double or 4X speed mode, set this bit to "1". When returning to normal mode, write "0" to this bit during a system reset.

② **D6: OUT3E_N**

0 : SDOUT3 output enable
1 : SDOUT3 = "L"

③ **D5: OUT2E_N**

0 : SDOUT2 output enable
1 : SDOUT2 = "L"

④ **D4: OUT2E_N**

0 : SDOUT1 output enable
1 : SDOUT1 = "L"

⑤ **D3:TEST**

0:Normal operation
1:Test mode (Do NOT use this mode)

⑥ **D2:TEST**

0:Normal operation
1:Test mode (Do NOT use this mode)

⑦ **D1:TEST**

0:Normal operation
1:Test mode (Do NOT use this mode)

⑧ **D0: set "0"**

Note): Underlines "_" mean default setting.

4) CONT3 : Internal Path Select (refer to (2) Total Block Diagram)

Writing during the system reset ($\overline{\text{S\_RESET}}$ = "L") is recommended.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
66h	76h	CONT3	SWJX2	SWJX1	SWJX0_N	SWQ4	SWIA	SWQD	SWEE	X	0000_000x

① **D7:SWJX2**

0: SDIN3 / JX2 pin is used as SDIN3 pin (JX2 = 0).

1: SDIN3 / JX2 pin is used as JX2 pin.

② **D6:SWJX1**

0: SDIN4 / JX1 pin is used as SDIN4 pin (JX1 = 0).

1: SDIN4 / JX1 pin is used as JX1 pin.

③ **D5:SWJX0_N**

0: JX0 / SDIN5A pin is used as JX0 pin.

1: JX0 / SDIN5A pin is used as SDIN5A pin (JX0 =0).

④ **D4:SWQ4**

0: DSP SDOUT4 is selected.

1: ADC SDATA-AD is selected.

⑤ **D3:SWIA**

0: ADC SDATA-AD is selected.

1: JX0 / SDIN5A pin is selected.

⑥ **D2:SWQD**

0: DSP SDOUT4 is output

1: Data selected by SWIA is output.

⑦ **D1:SWEE Status Information Select (EESEL = "H")**

0: HFST N is selected.

1: EEST is selected.

⑧ **D0 : set "0"**

note) Under-lined set values in ① ~⑦ above indicate the default values.

5) CONT4 : CLKO and Other Setting

Writing during the system reset ($\overline{\text{S\_RESET}}$ = "L") is recommended.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
68h	78h	CONT4	TEST	CLKS1	CLKS0	CLKE_N	BLCKE_N	OUT4E	TEST	X	0000_000x

① D7:TEST

0: normal operation

1: Test mode (do not use)

② D6,D5:CLKS1,CLKS0 CLKO Output Clock Select

CLKO outputs "L" level during the system reset. After the release of the system reset, selected value is output by CLKS1 and CLKS0.

CLKS mode	CLKS1	CLKS0	CLKO
0	0	0	see the following table
1	0	1	MCLK/3
2	1	0	MCLK/2
3	1	1	N/A

1) in CLKS mode 0, at CKSX = "1" or (CKSX = "L" & SMODE = "H")

fs: sampling frequency

DFS mode	DFS [2:0]	fs(kHz)	CLKO output
0	0h	48(,44.1)	256fs
1	1h	96(,88.2)	N/A
2	2h	192(,176.4)	N/A
3	3h	32(,29.4)	256fs
4	7h	8	1024fs

2) in CLKS mode 0,at CKSX = "L" & SMODE = "L"

fs: sampling frequency

BCK mode	CKS pin [1:0]	fs(kHz)	CLKO output
0	0h	48(,44.1)	256fs
1	1h	96(,88.2)	N/A
2	2h	192(,176.4)	N/A
3	3h	8	1024fs

③ D4:CLKE_N CLKO Output Control pin

0: CLKO output select

1: CLKO output is set to "L".

④ D3:BITCLKE_N BITCLK, LRCLK Output Control pin

0: enables outputs of BITCLK,LRCLK(@EESEL="H",SMODE="H"),BITCLK_O,LRCLK_O

1: sets BITCLK, LRCLK(@EESEL = "H", SMODE = "H"),BITCLK_O,LRCLK_O outputs to either "L" or "H" .

⑤ D2:OUT4E

0: SDOUT4A = "L"

1: SDOUT4A output enable

⑥ D1:TEST

0: normal operation

1: Test mode (do not use)

⑦ D0 : set "0".

note) Under-lined set values in ① ~⑥ above indicate the default values.

6) CONT5 : HF Set & Instruction Set

The setting is enabled only during the system reset ($\overline{\text{S\_RESET}}$ = "L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
6Ah	7Ah	CONT5	HF_RST_N	HF	PID	SSDIN4	SSDIN3	OP1	OP0	X	0000_000x

① D7: HF_RST_N

0: reset the ARM for hands-free use.

1: release the reset of the ARM for HF use.

Set HF-RST-N = 1 and after the system reset is released, it is put into hands-free mode.
In order to return from the hands-free mode to normal DSP mode, set HF-RST-N = 0.

② D6: HF

0: normal mode set

1: hands-free mode set

DSP_SDIN3 and DSP_SDOUT3 are switched to the ARM interface.
SDIN3 cannot be used (can be used as JX1). Output of PIN-SDOUT3 becomes "L".

③ D5: PID Selection of hands-free parameters sets

0 : ROM data is used (Default set of hands-free parameters)

1 : Param Register RAM is used

Noise canceller uses the customized parameter set which is allocated in RAM area. The procedure for getting the optimized hands-free parameters is described in the page <TBD>.

④ D4: SSDIN4 Selection of DSP instrcution

0 : ODRB*,MSRG*

1 : INL4*, INR4*(SDIN4 Digital Input)

This bit switches the source of DBUS from ODRB*, MSRG* to INL4*, INR4*.
(*: ODRB, MSRG, INL4, INR4 are assembler code. Please see other document for the detail)

⑤ D3: SSDIN3 Selection of DSP instruction

0 : TDR2*, TDR3* (DR2, DR3 Through Output)

1 : INL3*, INR3* (SDIN3 Digital Input)

This bit switches the source of DBUS from TDR2*, TDR3* to INL3*, INR3*.
(*: TDR2, TDR3, INL3, INR3 are assembler code. Please see other document for the detail)

⑥ D2, D1 : OP1, OP0 Offset- RAM- Pointer Mode Select

mode	OP1	OP0	Pointer 1	Pointer 0
0	0	0	DBUS immediate pointer	OFFSET indirect pointer
1	0	1	OFFSET indirect pointer	OFFSET indirect pointer
2	1	0	DBUS immediate pointer	DBUS immediate pointer
3	1	1	N/A	N/A

note) Even when DLC* is issued in mode 1, the offset address (location) is valid.
(*: DLC is assembler code. Please see other document for the detail)

⑦ D0 : set "0".

note) Under-lined set values in ① ~⑥ above indicate the default values.

7) CONT6 : DAC Setting etc

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
6Ch	7Ch	CONT6	PS CODEC	DAF	SF1	SF0	SMUTE	TEST	TEST	X	0000_000x

① **D7:PSCODEC ADC, DAC power-down**

0: normal operation

1: power –down ADC, and DAC

Note1) PDAD bit in the CONT2 register must be set to “1” when this bit is set to “1”.

Note 2) In a double or 4X speed mode, this bit, and PSAD bit must be set to “1”.

② **D6: DAF Selection of DAC digital filter**

0: DAC digital filter characteristics a) in page 17

1: DAC digital filter characteristics b) in page 17

The change must be set at system reset.

When the sample rate is set to 8kHz, DAF=”1” is recommended

③ **D5, D4: SF1, SF0 Selection of DAC soft mute cycle time**

SF mode	SF1	SF0	
0	0	0	1008 LRCLK cycle
1	0	1	4032 LRCLK cycle
2	1	0	504 LRCLK cycle
3	1	1	2016 LRCLK cycle

④ **D3: SMUTE Soft Mute Selection**

0 : normal operation

1 : DAC soft mute enable

⑤ **D2:TEST(SEL_MCLK)**

0 : normal operation

1 : Test mode (do not use).

⑥ **D1:TEST(PLLSTBY)**

0 : normal operation

1 : Test mode (do not use).

⑦ **D0 : set “0”.**

note) Under-lined set values in ① ~ ⑥ above indicate the default values.

8) CONT7 : Hands-Free Status / Request

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
X	DCh	CONT7	SRRQ	TEST	TEST	TEST	TEST	TEST	TEST	X	0000_000x

*) This register, together with $\overline{\text{HFST}}$ pin, is used to inform the host microcontroller that the hands-free operation is enabled. $\overline{\text{HFST}}$ pin is usually at “H” but when an exception/interrupt occurs, this pin notifies the host(this pin becomes “L”, and SRRQ goes to “1”).
Upon receipt of $\overline{\text{HFST}}$ = “L”, the host is expected to read and process the CONT7 register, depending on the register content. This register is cleared by setting $\overline{\text{S\_RESET}}$ pin to “L”, and $\overline{\text{HFST}}$ pin returns to “H”. Reading should be made during $\overline{\text{S\_RESET}}$ = “H” (during RUN).

① **D7:SRRQ**

0: normal operation

1: requests that the host enable S-RESET.

This bit Indicates that a hardware-related error has occurred in hands-free mode.

If same error occurs again , initialize the AK7750 by issuing $\overline{\text{S\_RESET}}$ = “L”.

② **D6,D5,D4,D3,D2,D1,D0:TEST_MON**

Monitor pin for test.

(3) Power-ON Sequence

Power-On while holding $\overline{\text{INIT\_RESET}}$ = “L” and $\overline{\text{S\_RESET}}$ = “L”.
Control registers are initialized during $\overline{\text{INIT\_RESET}}$ = “L” (see note 1 and note 2).
After power is applied, $\overline{\text{INIT\_RESET}}$ = “H” and REF generating circuit (Analog Reference Voltage source) and PLL are turned on, and master clock is generated by the PLL.
Communication with the AK7750 should be made after the PLL oscillation is stabilized (50ms@ XTI mode, and BCK mode 0/1/2; 175ms@BCK mode 3).
An initialization by $\overline{\text{INIT\_RESET}}$ is usually required only for power- on.
The power should be turned on when $\overline{\text{CK\_RESET}}$ pin is linked with $\overline{\text{INIT\_RESET}}$ or while it is fixed to “H”.

Note1) to assure proper initialization, it is necessary that power is turned on and then the master clock (XTI) is supplied.

Note2) when a crystal oscillator is used, $\overline{\text{INIT\_RESET}}$ should be set to “H” after the oscillation is stabilized. Stabilization time of the oscillation varies depending upon types of crystal oscillators and external circuits used.

Note) Do not stop the system clocks (Slave Mode: XTI, LRCLK, BITCLK and Master Mode : XTI) except during the initial reset ($\overline{\text{INIT\_RESET}}$ = “L” and $\overline{\text{S\_RESET}}$ = “L”) or at a system reset ($\overline{\text{S\_RESET}}$ = “L”) or at a Clock reset ($\overline{\text{CK\_RESET}}$ = “L”).
If these clocks are not applied, there is a possibility that an excess current will flow, causing erratic operation.

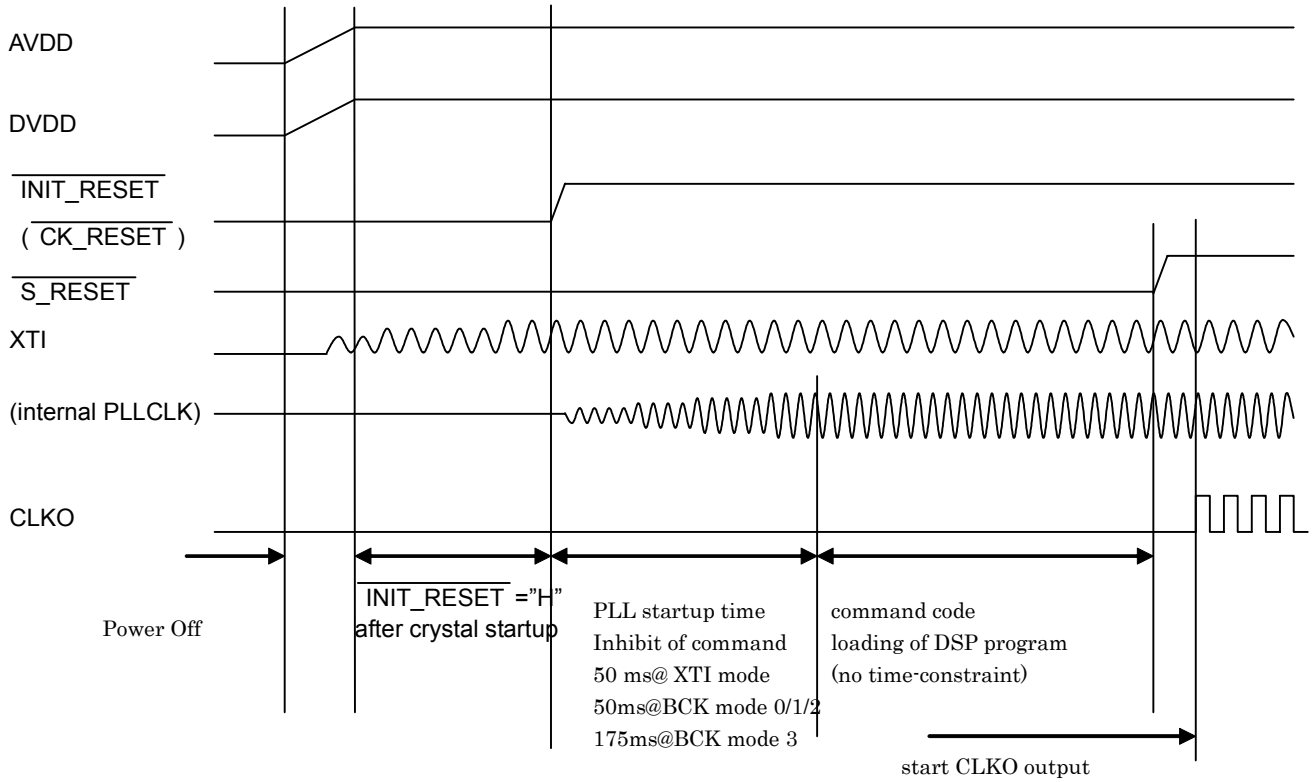


Figure Power-up Sequence

(4) About Reset

The AK7750 has 3 reset pins, $\overline{\text{INIT\_RESET}}$, $\overline{\text{S\_RESET}}$ and $\overline{\text{CK\_RESET}}$.
There are 2 reset bits in control registers HF_RESET_N (CONT5 D7) and CKRST (CONT0 D1).
A clock reset $\overline{\text{CK\_RESET}}$ (CKRST) will be described in section (5) , “Switching Clocks”.
When the $\overline{\text{CK\_RESET}}$ pin is not used, either connect it to the $\overline{\text{INIT\_RESET}}$ pin or set it to “H”.
HF_RESET_N is described in section (2) “Control Register Settings”.

$\overline{\text{INIT\_RESET}}$ is used to initialize the AK7750 as is described in the Power-on Sequence description.
When changing CKS1, CKS0, CKSX or SMODE, or when changing the XTI pin’s input clock frequency, it is recommended to execute it during the initial reset ($\overline{\text{INIT\_RESET}}$ = “L”, $\overline{\text{S\_RESET}}$ = “L”). A change can be made during a clock reset ($\overline{\text{CK\_RESET}}$, CKRST) if audio interruption is acceptable and no other setting changes are made.

Since the CKS1, CKS0, CKSX, SMODE and XTI pins are involved in PLL and internal clock control, erroneous operation may occur if any changes are made other than during initial reset or clock reset.
With $\overline{\text{INIT\_RESET}}$ = “H” & $\overline{\text{S\_RESET}}$ = “L”, the device is put into system reset condition (“ reset “implies a system reset).
Usually program and RAM data is written during a system reset (excluding write during RUN).
During a system reset, both the ADC and DAC are reset. The REF generating circuit remains in operation.
CLKO output and LRCLK, BITCLK in Master mode are stopped during a system reset.
System reset is released by rising $\overline{\text{S\_RESET}}$ to “H”, which starts the internal counters.

In Master mode, LRCLK and BITCLK are generated by the AK7750’s counters, which may generate a clock conflict if other devices are not properly initialized. In Slave mode, when a system reset is released, internal timing starts to operate in sync with the rising edge of LRCLK (in standard input format).
Timing adjustment between an external clock and internal timing is made during this time. During the operation, if the phase-difference (both at the rising edge and at the falling edge) between LRCLK and internal timing is within 2 clock pulses of BITCLK (64fs), operation continues.
When the phase-difference becomes larger than the above range, a phase adjustment is made in sync with the rising edge of LRCLK (in standard input format).
This circuit protects the AK7750 from becoming out of sync with external circuits due to noise etc. Correct data is not output for a while even after out-of-sync condition returns to normal.

In the ADC, data output is available 516 LRCLK clocks after the internal counters start to operate (internal counters start to operate right after the release of system reset in Master mode, or in Slave mode approximately 2 LRCLK clocks after the release of system reset).

The AK7750 returns to normal operation at the rising edge of $\overline{\text{S\_RESET}}$.

The AK7750 goes from normal state to system reset state by the falling edge of $\overline{\text{S\_RESET}}$. Please do not stop the input clock for 3 MCLK times period after the falling edge of $\overline{\text{S\_RESET}}$.

(5) About Clock Changes

Changes to CKS1, CKS0, CKSX or SMODE are made during the system reset ($\overline{\text{S\_RESET}}$ = "L", $\overline{\text{INIT\_RESET}}$ = "H"), or when an input clock is switched (XTI @ CKSX= "H" or BITCLK (_I) @ (CKSX = "L" & SMODE = "L")). A clock reset is made using either the $\overline{\text{CK\_RESET}}$ pin or by using CKRST control register bit. After a reset, the internal Master clock, MCLK, is stopped and it is safe to change settings (MCLK = 36.864 MHz or 33.8688 MHz) during the system reset.

After executing a system reset, clock reset is performed by changing the $\overline{\text{CK\_RESET}}$ pin from "H" to "L", and by continuously supplying a clock- for a duration of longer than 120 / MCLK [us] from the falling edge of $\overline{\text{CK\_RESET}}$ ($\overline{\text{S\_RESET}}$ and $\overline{\text{CK\_RESET}}$ pins can be simultaneously set to low). When the CKRS control register is used, the duration is 120 / MCLK [us] from the rising edge of 16th clock of CONT0.

Pin setting and input clock changes (XTI @ CKSX = "H" or BITCLK (_I) @ (CKSX = "L" & SMODE = "L") should be done after MCLK is stopped.

After changes are made and after the input clock is stabilized to the new value, release $\overline{\text{CK\_RESET}}$ from "L" to "H" and PLL is restarted.

Do not transmit the DSP program and coefficient data from the microprocessor until the PLL reaches stable oscillation (about 25ms). Control register read/write operations are allowed after the input clock is stabilized to the new value.

The AK7750 returns to normal operating condition by rising $\overline{\text{S\_RESET}}$ to "H" after the DSP program and coefficient data are transmitted. When pin-set- and clock input switches are made and μC interface is not used, it is possible to raise both the $\overline{\text{CK\_RESET}}$ and $\overline{\text{S\_RESET}}$ pins simultaneously to return the AK7750 to normal operation. However an internal circuit reset cannot be released until the PLL reaches its stable oscillation (about 25ms) even if $\overline{\text{S\_RESET}}$ is released.

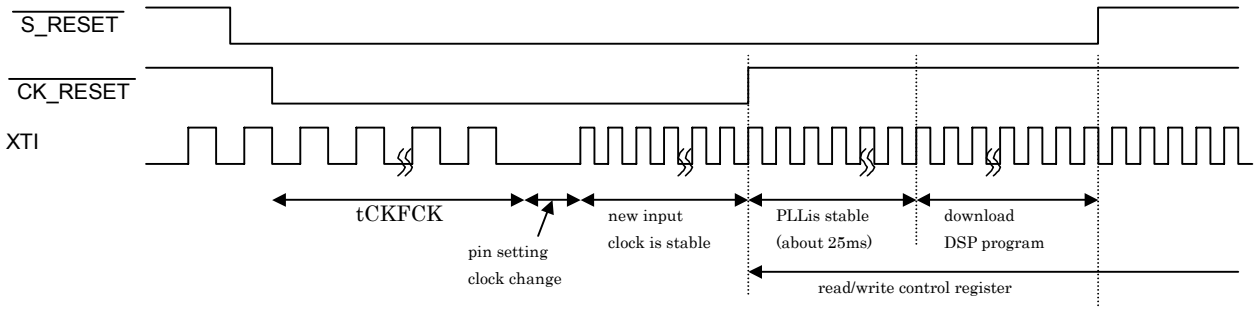


Figure $\overline{\text{CK\_RESET}}$ Sequence

tCKFCK table(XTI mode)

XTI mode	CKS [1:0]	XTI	tCKFCK(min) XTI cycles	fs:48kHz series	fs:44.1kHz series
0	0h	MCLK/3	40	3.3μs	3.6μs
1	1h	MCLK/2	60	3.3μs	3.6μs
2	2h	MCLK*(2/3)	80	3. 3μs	3.6μs
3	3h	MCLK	10	0.3μs	0.3μs

tCKFCK table(BCK mode)

BCK mode	CKS [1:0]	BITCLK	tCKFCK(min) BITCLK cycles	fs:48kHz series	fs:44.1kHz series
0	0h	MCLK/12	10	3.3μs	3.6μs
1	1h	MCLK/6	20	3.3μs	3.6μs
2	2h	MCLK/3	40	3.3μs	3.6μs
3	3h	MCLK/72	10	19.5μs	NA

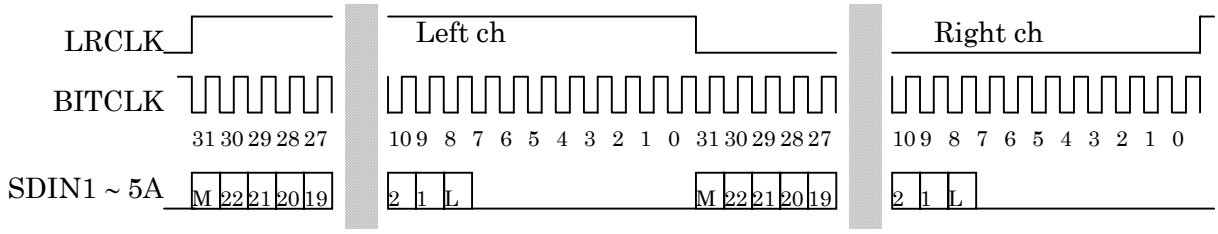
(6) Audio Data Interface

Serial Audio Data pins, SDIN1, SDIN2, SDIN3, SDIN4, SDIN5A, SDOUT1, SDOUT2, SDOUT3, SDOUT4A interface with external systems using LRCLK and BITCLK.
Proper control register settings are required. Please refer to the Total Block Diagram and the Control Register Setting section.

Data Format is in 2's complement with MSB first.
Supported Input and Output Formats are AKM's standard format plus I2S compatible mode. In this mode, interface of all input and output audio data pins are also I2S compatible.
The default setting is MSB-justified 24 bit format, but by properly setting the control register CONT0 DIF1(D3), DIF0 (D2), other formats such as LSB-justified 24-bit, LSB-justified 20-bit and LSB-justified 16-bit are also supported (note : CONT0 DIFS (D4) = 0). However, SDIN1, SDIN2, SDIN3, SDIN4 and SDIN5A must all be set to the same format, and cannot be independently set to support different formats. Outputs SDOUT1, SDOUT2, SDOUT3 and SDOUT4A are in MSB-justified, fixed-24 bit data.

1) Standard Input Format (DIF[2] = 0 : default value)

a) DIF mode 0 (DIF[2:0] = 0h : default value)

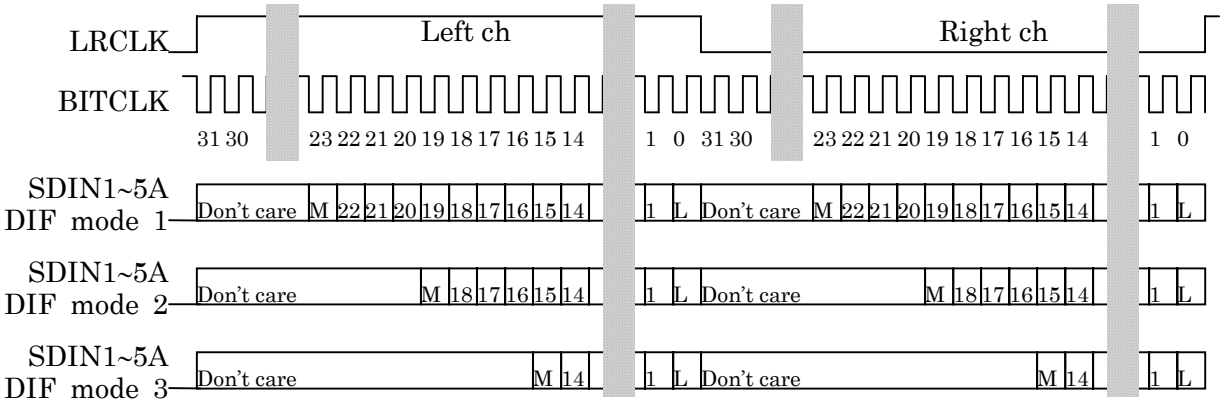


M: MSB, L: LSB

When MSB-justified 20-bit data is input to SDIN1, 2, 3, 4A, fill 4 zeros ("0") in sequence, starting at the LSB of each data.

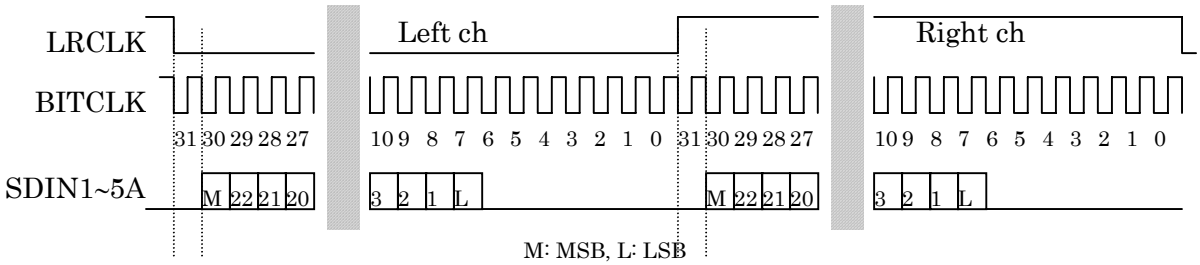
b) DIF mode 1,2,3

SDIN1, 2, 3, 4, 5A	mode 1: (DIF[2:0] = 1h	LSB-justified 24 bit)
SDIN1, 2, 3, 4, 5A	mode 2: (DIF[2:0] = 2h	LSB-justified 20 bit)
SDIN1, 2, 3, 4, 5A	mode 3: (DIF[2:0] = 3h	LSB-justified 16 bit)

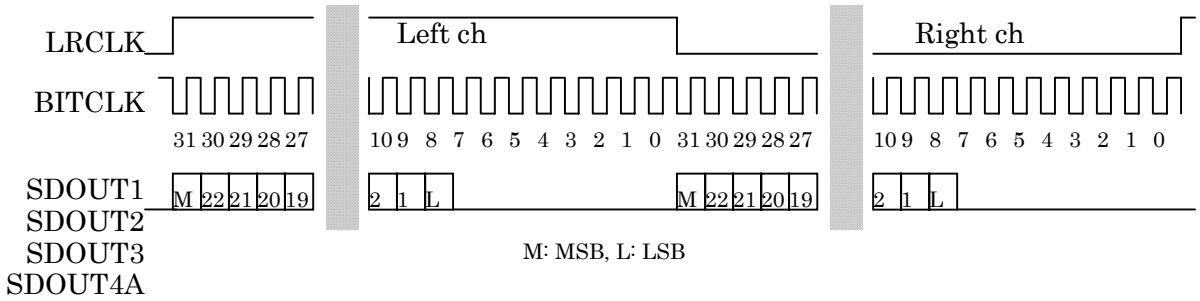


M: MSB, LSB: LSB

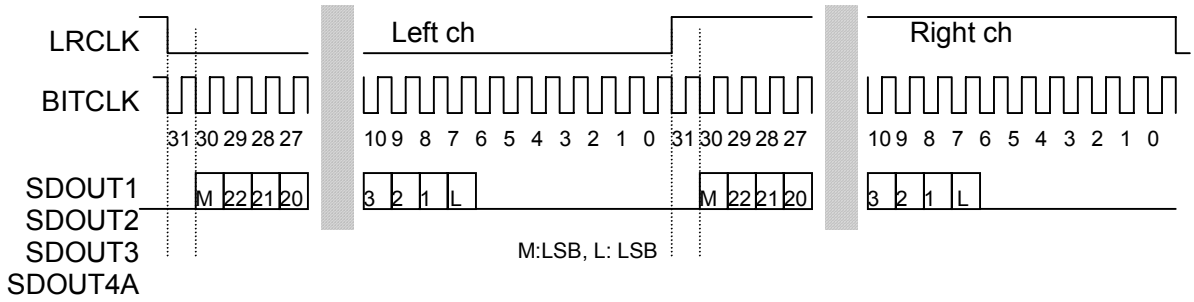
2) I2S Compatible Input Format (DIF[2:0] = 4h)



3) Standard Output Format (DIF[2:0] = 0h, 1h, 2h, 3h)

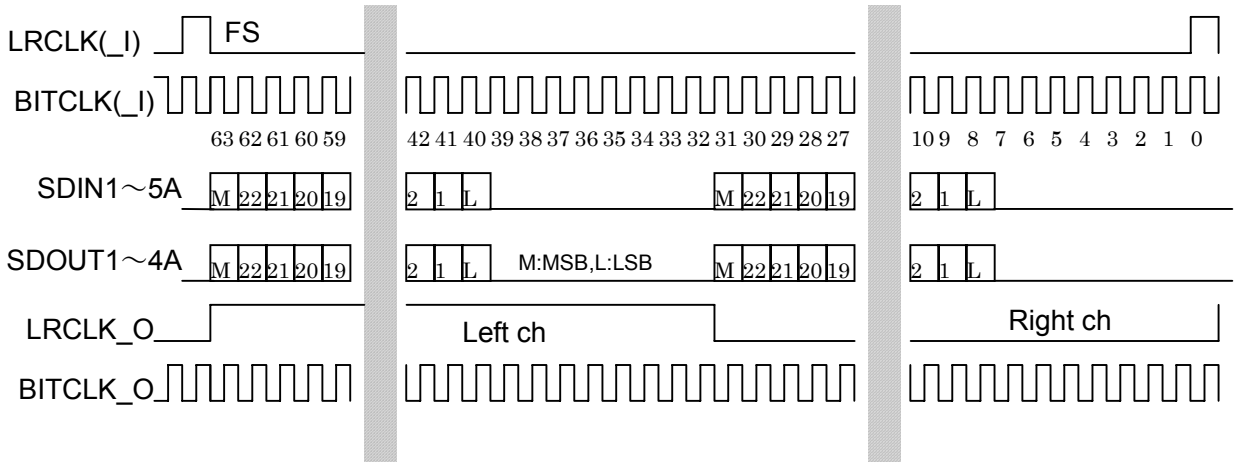


4) I2S Compatible Output Format (DIF[2:0] = 4h)

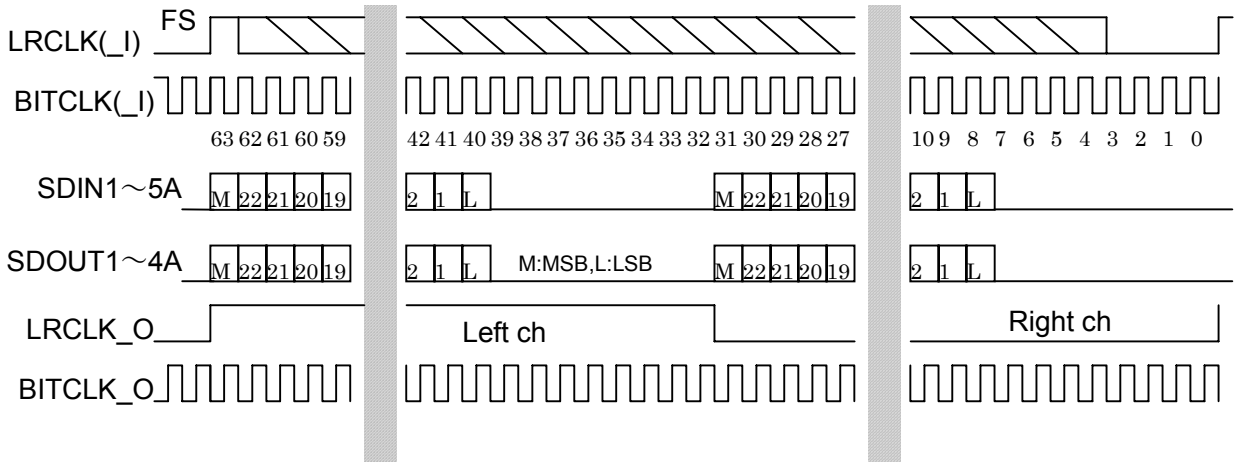


5) PCM mode (DIF[2:0]=5h, 6h)

i) PCM1 SF(Short Frame) mode (BITCLK(_I)=64fs : fs=8kHz ~ 48kHz)



ii) PCM2 LF(Long Frame) mode (BITCLK(_I)=64fs : fs=8kHz ~ 48kHz)



(7) Microprocessor Interface

The microprocessor interface uses 6 control signals, $\overline{RQ}$ (ReQuest Bar), SCLK (Serial data input Clock), SI (Serial data Input), SO (Serial data Output), RDY (ReaDY), DRDY (Data ReaDY).
The AK7750 has 2 types of write and read operations – write / read during reset (usually refers to system reset) and, write / read during normal operation.
During reset, it is possible to write data into the control registers, program RAM, coefficient RAM, offset RAM and to write external conditional jump codes. It is possible to read data from the control registers, program RAM, coefficient RAM and offset RAM.
During normal operation, it is possible to write data into coefficient RAM, offset RAM, and to write external conditional jump codes. It is also possible to read data on the DBUS (Data Bus) via SO and to read data from control registers. Data is input or output in serial form with MSB first.

The interface between the microprocessor and the AK7750 (except for DBUS read operations) is enabled by setting $\overline{RQ}$ to "L" of. Data is taken at the rising edge of SCLK and data is output at the falling edge of SCLK. As for the data format, command code is input first, then address and coefficient data is input or output. Since a single command is completed by setting $\overline{RQ}$ to "H", in order to write a new command, it is necessary to set $\overline{RQ}$ to low again after setting $\overline{RQ}$ to "H".

Contrarily, DBUS data reads are of accomplished by setting $\overline{RQ}$ to "H" (no command code input).
There is a case where SI is used as control signal, depending upon the application. In this case, this pin should be protected spurious noise, as is the case of a normal clock signal..
Command Code table is listed below.

Conditions for use	Code name	Command code		Remark
		WRITE	READ	
RESET Phase	CONT0	60h	70h	For the function of each bit, See the description of Control Registers
	CONT1	62h	72h	
	CONT2	64h	74h	
	CONT3	66h	76h	
	CONT4	68h	78h	
	CONT5	6Ah	7Ah	
	CONT6	6Ch	7Ch	
	CONT7	-	DCh	
	PRAM	C0h	C1h	
	CRAM	A0h	A1h	
	OFRAM	90h	91h	
	External condition jump	C4h	-	
	CRC check (R(x))	B6h	D6h	
	Hands free parameter	E0h	E1h	
RUN phase	CONT0~CONT7	NA	above address	Read available, same as RESET code.
	CRAM rewrite preparation	A8h	-	It needs to do before CRAM rewrite
	CRAM rewrite	A4h	-	
	OFRAM rewrite preparation	98h	-	It needs to do before OFRAM rewrite
	OFRAM rewrite	94h	-	
	External condition jump	C4h	-	Same code as RESET
	CRC check (R(x))	B6h	D6h	Same code as RESET

note: As there are some duplicated codes in use, command codes other than those listed above should not be accessed, as erroneous operation may result. If no communication exists with a microprocessor, set SCLK to "H" and SI to "L".

1) Write during reset phase

a) Control register write (during reset phase)

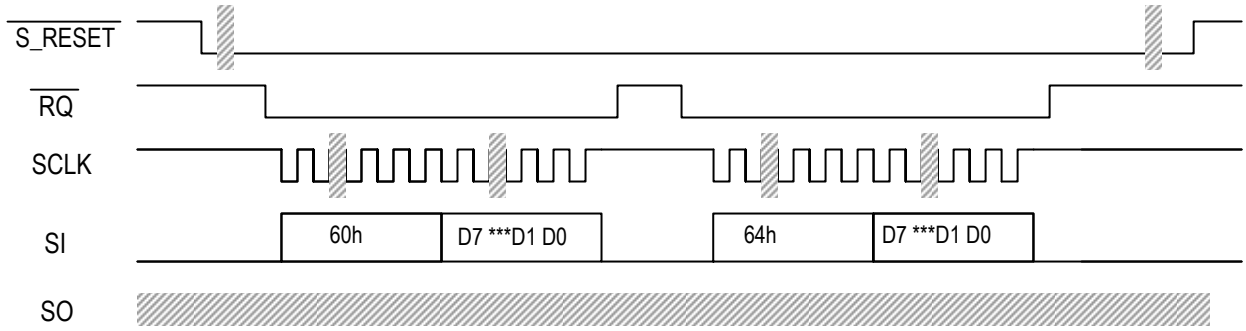
The data consists of 2 bytes used to perform control register write operations (during reset phase). When all data has been entered, the new data is stored in the register at the rising edge of the 16th count of SCLK.

Data transfer procedure

① Command code	60h, 62h, 64h, 68h, 6Ah, 6Ch, B8h
② Control data	(D7 D6 D5 D4 D3 D2 D1 D0)

note) 40h, 44h and 48h are for testing and cannot be used.

For the function of each bit, see the description of Control registers, (section 2).



Note) It must be set always 0 to D0.

Control Registers write operation

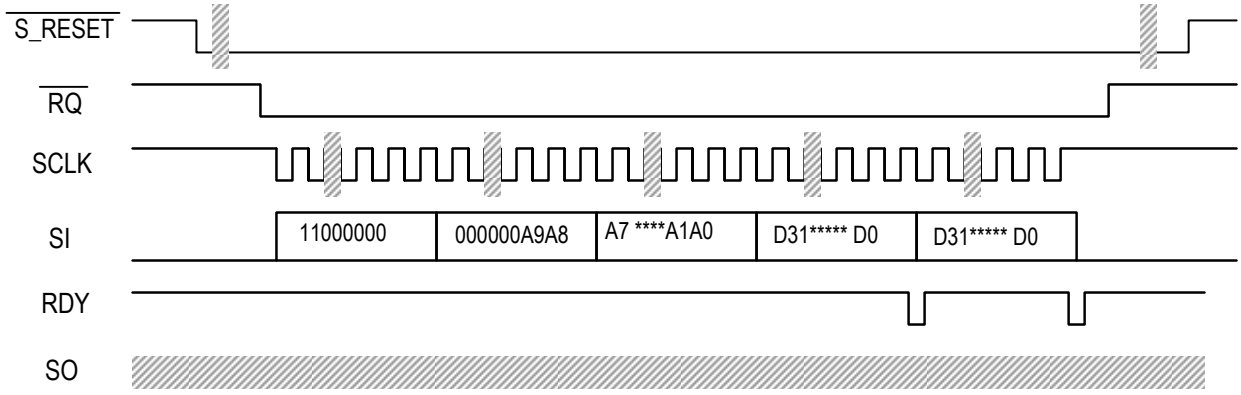
b) Program RAM writes (during reset phase)

Program RAM write operations are performed during the reset phase using 7-bytes of data. When all data has been transferred, the RDY terminal is set to "L". Upon completion of writing into the PRAM, RDY returns “H” to allow the next data bit input. When writing to sequential addresses, input the data without a command code or address. To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L" again and then input the command code, address and data in that order.

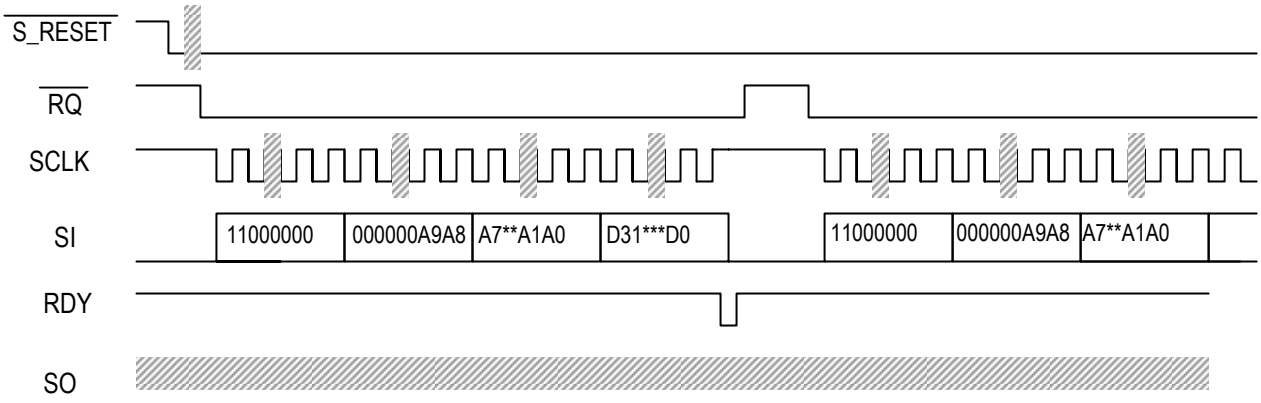
Note) “L” period of RDY is shorter than 1 master clock (20ns) under typical condition

Data transfer procedure

① Command code	C0h (1 1 0 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 A9 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D31 . . . . . D24)
⑤ Data	(D23 . . . . . D16)
⑥ Data	(D15 . . . . . D8)
⑦ Data	(D7 . . . . . D0)



Input of continuous address data into PRAM



Input of discontinuous address data into PRAM

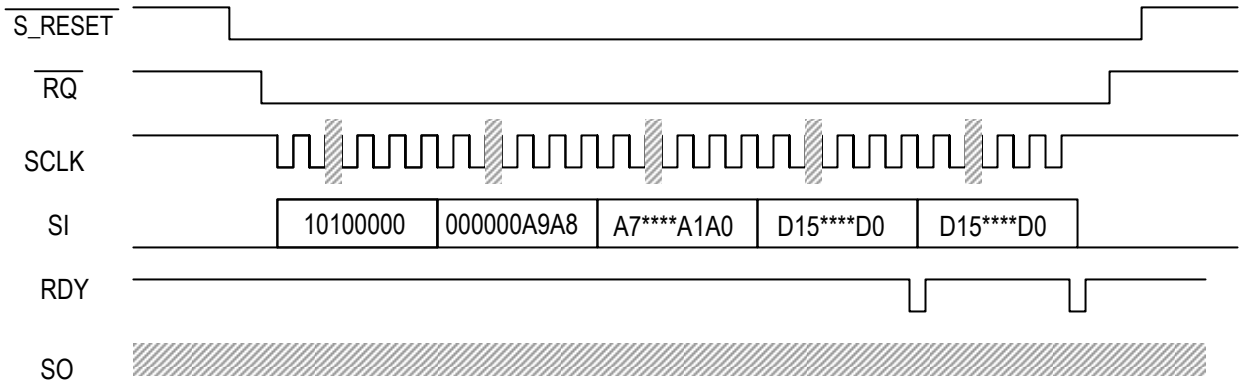
c) Coefficient RAM write (during reset phase)

5 bytes of data are used to perform coefficient RAM write operations (during the reset phase). When all data has been transferred, the RDY terminal goes to "L". Upon completing the CRAM write, RDY goes to "H" to allow the next data to be input. When writing to sequential addresses, input the data as shown below. To write discontinuous data, transition the $\overline{RQ}$ terminal from "H" to "L" and then input the command code, address and data.

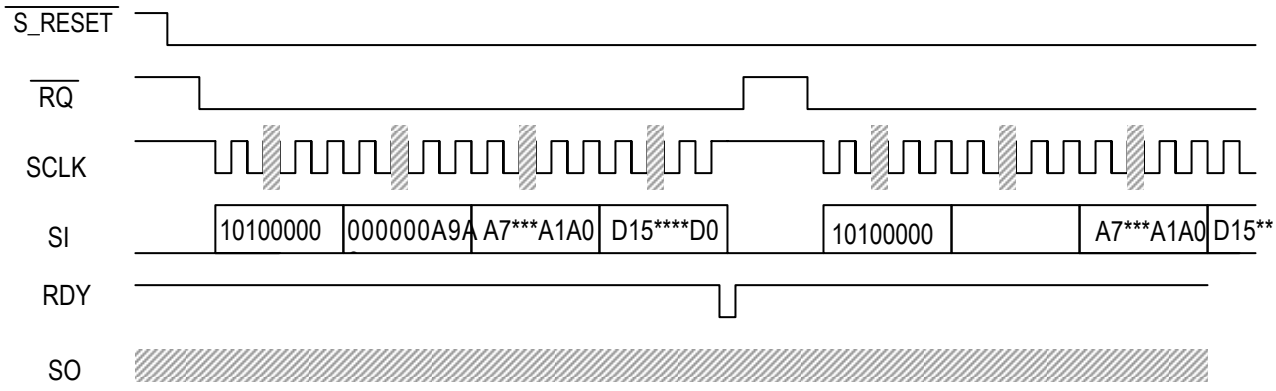
Note) "L" period of RDY is shorter than 1 master clock (20ns) under typical condition

Data transfer procedure

① Command code	A0h	(1 0 1 0 0 0 0 0)
② Address upper		(0 0 0 0 0 0 A9 A8)
③ Address lower		(A7 . . . . . A0)
④ Data		(D15 . . . . . D8)
⑤ Data		(D7 . . . . . D0)



Input of continuous address data into CRAM



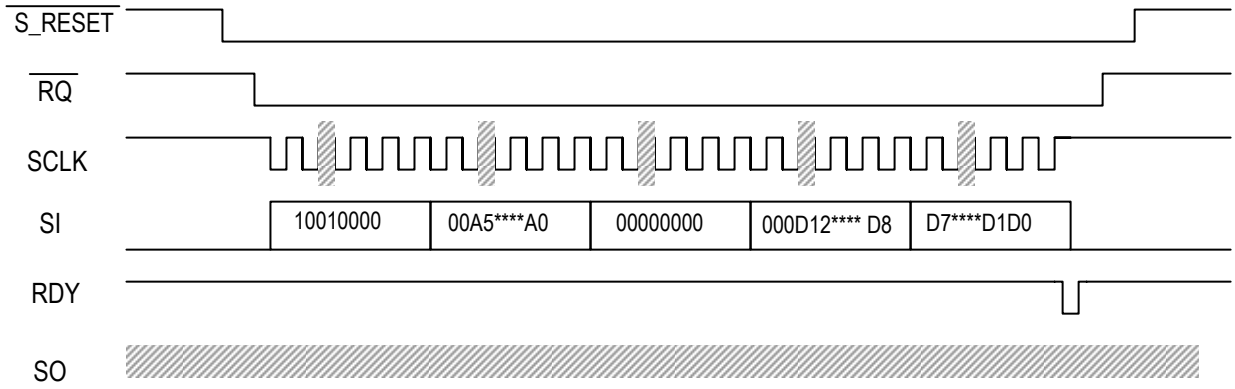
Input of discontinuous address data into CRAM

d) Offset RAM write (during reset phase)

Offset RAM Writes (at reset) are done by writing a command code first, then address and 3 bytes/set data. After the data is transferred, the RDY pin becomes “L” and after writing Offset RAM is completed, it becomes “H” and next data can be ready to input.

Data transfer procedure

① Command code	90h	(1 0 0 1 0 0 0 0)
② Address		(0 0 A5 A4 .. . . A0)
③ Data		(0 0 0 0 0 0 0 0)
④ Data		(0 0 0 0 D11 . . D8)
⑤ Data		(D7 . . . . . . D0)

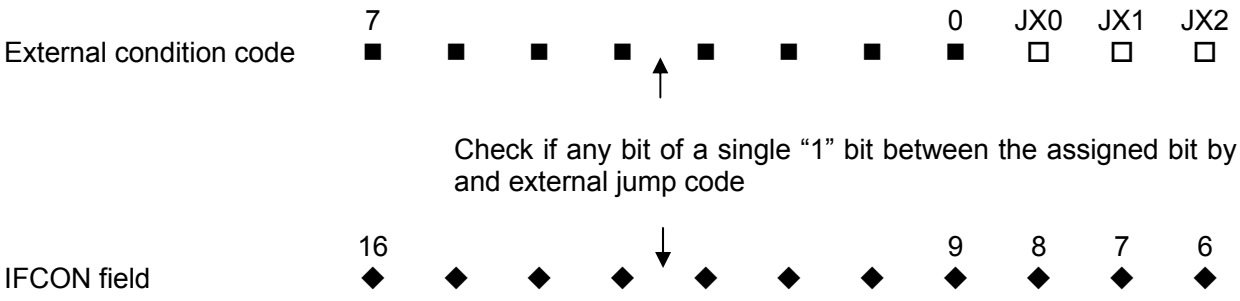


Input of data into OFRAM

e) External conditional jump code write (during reset phase)

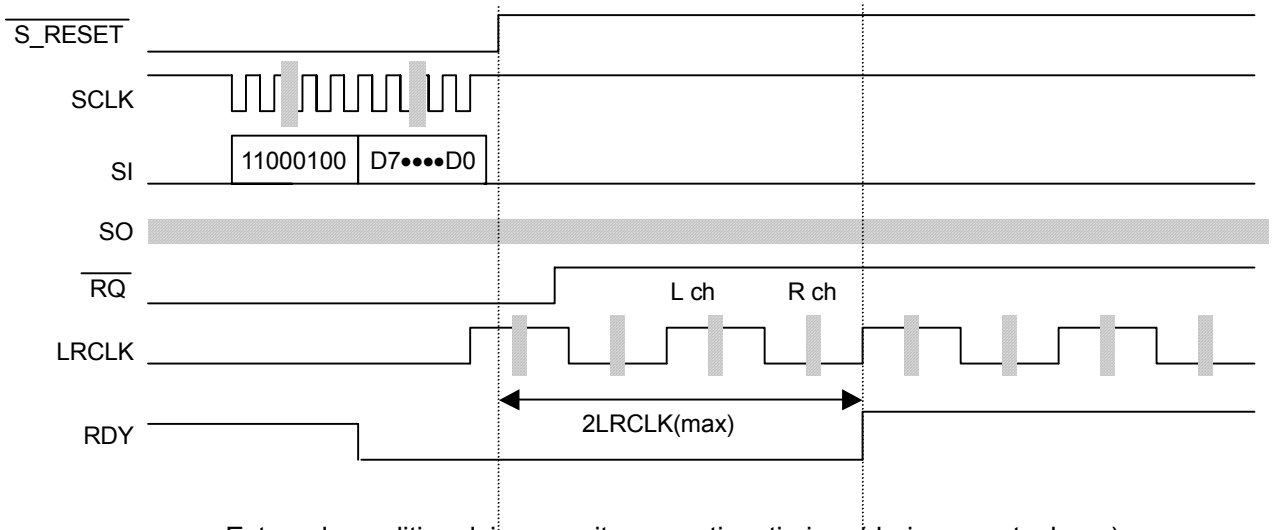
External conditional jump code writes are made after all necessary operations, such as program downloads, etc. are executed. Code writes are done in 2 bytes/set data. It is possible to input during both reset and in normal operation mode. Input data is set at each assigned register at the rising edge of LCRLK. RDY pin becomes “L” . After all data is transferred and it becomes “H” when write operation is finished.
External jump codes are 8-bits long and when any bit among the 11 code bits of JX0, JX1 and JX2 input pins and any single bit of “1” in the IFCON field match, the jump instruction is executed.
When writing data during the reset, it can be executed only before reset is released after completing all data transfers.
Setting $\overline{RQ}$ from “L” to “H” during reset mode writes should be made more than 2 MCLK clocks after reset is released. RDY becomes “H” when the next rising edge of LRCLK is detected.
Write operations from the microprocessor are inhibited until RDY becomes “H”.
The IFCON field is an external condition, written in the DSP program.
This jump code is reset to 00h by setting $\overline{INIT\_RESET}$ to “L”, however, it remains at its previous condition even when $\overline{S\_RESET}$ =”L”.

Note: It should be noted that the LRCLK phase is inverted in the I2S-compatible state.



Data transfer procedure

① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 . . . . . D0)



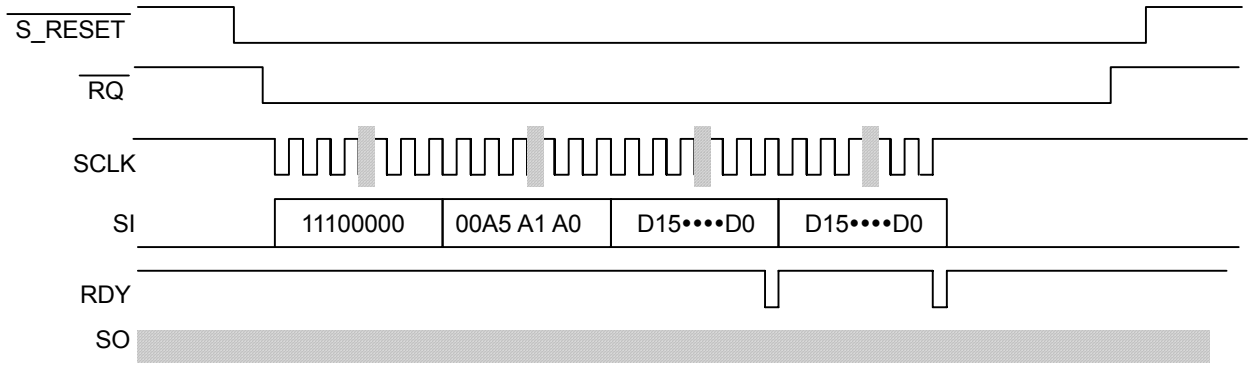
External conditional jump write operation timing (during reset phase)

f) Hands-Free Parameter RAM Write (at reset)

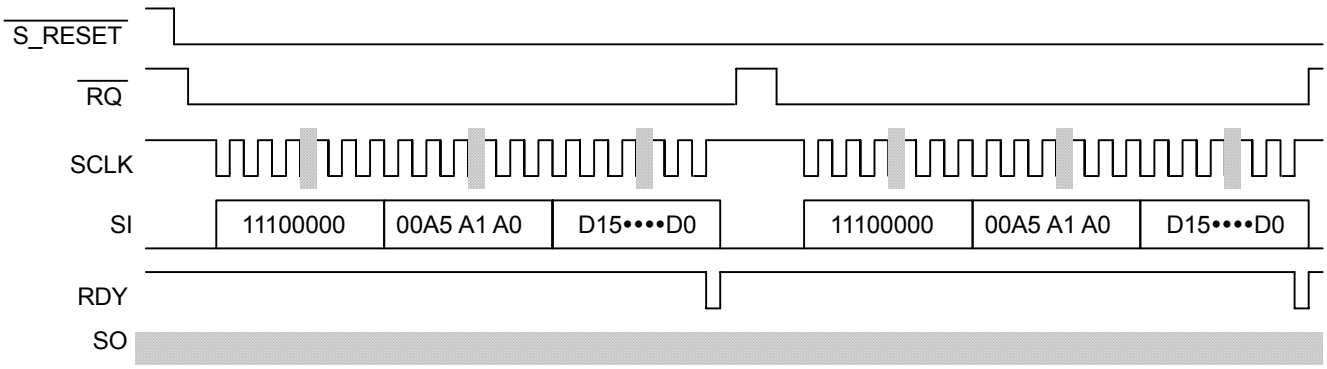
Hands-Free Parameter RAM Write operations (at reset) are executed in 4 bytes/set data.
When all data is transferred, the RDY pin becomes “L”. It becomes “H” after writing into Hands-Free Parameter RAM is completed and next data can be input.
When writing data at the consecutive address locations, input data as is. When writing data at the discontinuous address locations, input command code first, then address and data in this order after setting RQ-N pin from “H” to “L”.

Data transfer procedure

① Command code	E0h (1 1 1 0 0 1 0 0)
② Address	(0 0 A5 . . . . A0)
③ Data	(D15 . . . . . D8)
④ Data	(D7 . . . . . D0)



Input of continuous address data into Hands-free parameter RAM



Input of discontinuous address data into Hands-free parameter RAM

2) Read during reset phase

a) Control register data read (during reset phase)

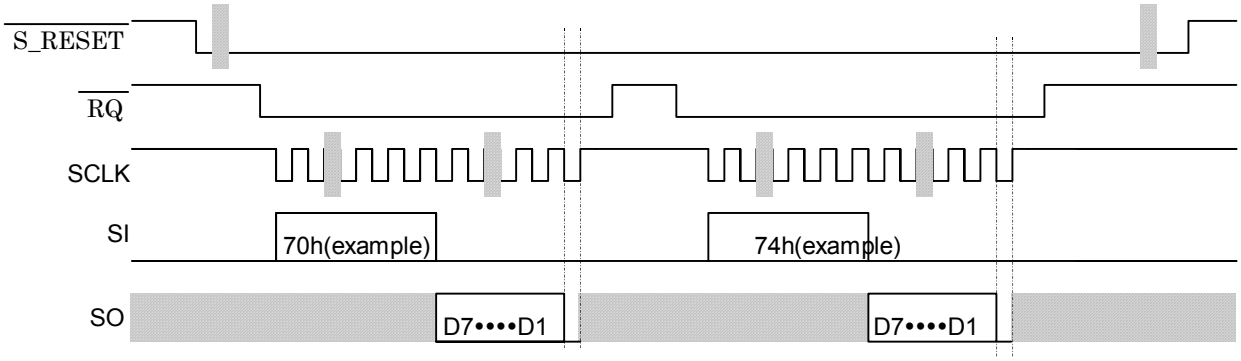
Control Register Read operations (at reset) are executed in 16-bit SCLK clocks.
Control register values D7 ~ D1 are output at the falling edge of SCLK after command code is input. D0 is invalid, ignore this bit.

Data transfer procedure

① Command code	70h, 72h, 74h, 76h, 78h, 7Ah, 7Ch, D8h, DAh, DCh

note) 50h,54h,58h are not usable as they are dedicated for testing.

For each bit function, please refer to section (2) Control Register Settings.



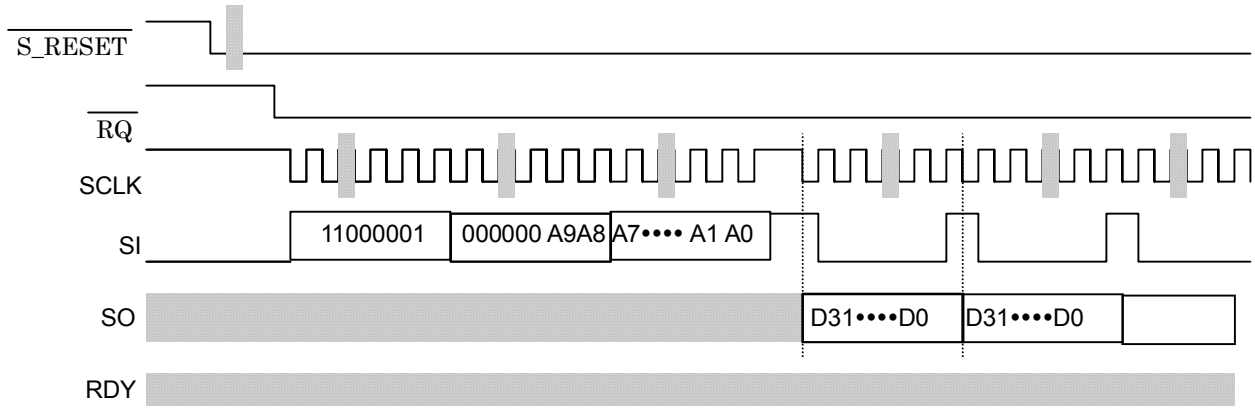
Reading of control register data

b) Program RAM read (during reset phase)

Program RAM reads require inputting a command code and address to be accessed and setting SCLK to fall after setting SI to “H”. The output data is synchronized with the falling edge of SCLK (Ignore RDY signal). When the requested read addresses are in consecutive locations, repeat the above procedure again by setting SI to “H”.

Data transfer procedure

①Command code input C1h (1 1 0 0 0 0 0 1)
②Read address input MSB (0 0 0 0 0 0 A9 A8)
③Read address input LSB (A7 . . . . . A0)



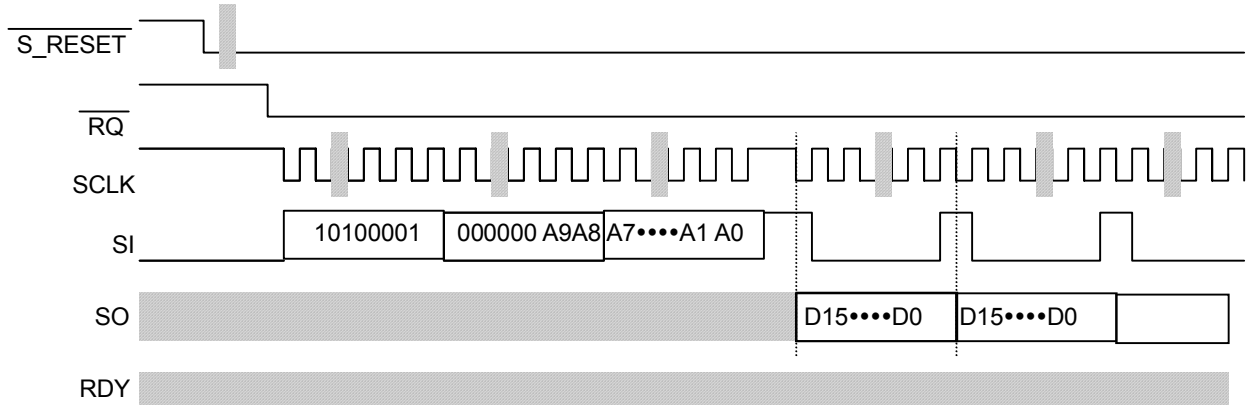
CRAM Data Read

c) Coefficient RAM Read (during reset)

Coefficient RAM reads require inputting a command code and address to be accessed and setting SCLK to fall after setting SI to “H”. Data is output synchronized with the falling edge of SCLK. When the requested read addresses are in consecutive locations, repeat the above procedure again by setting SI to “H”.

Data transfer procedure

① Command code	A1h	(1 0 1 0 0 0 0 1)
② Address upper		(0 0 0 0 0 0 A9 A8)
③ Address lower		(A7 . . . . . A0)



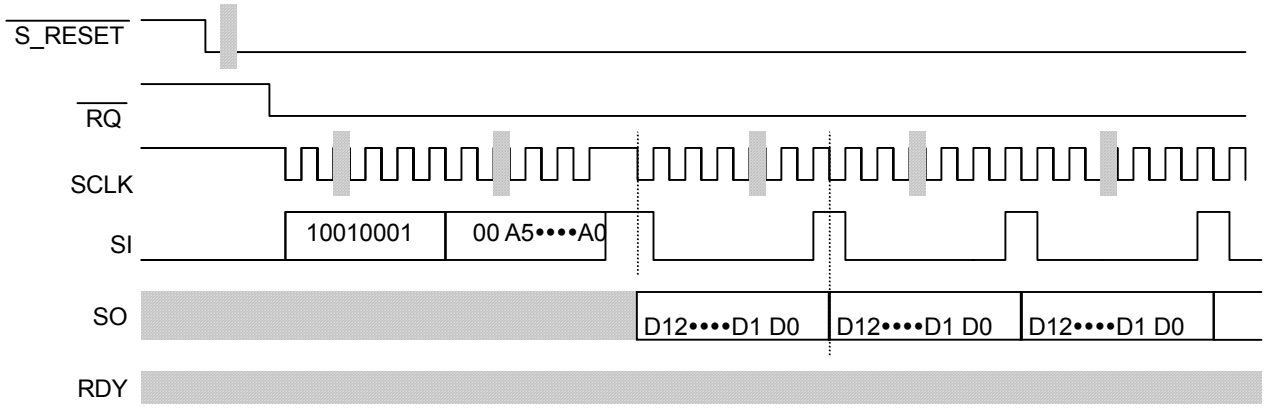
CRAM data read

d) Offset RAM Data Read (during reset)

It is possible to read out the stored Offset RAM data during reset.
Read procedure involves inputting a command code and address to be accessed, and waiting for SCLK to fall after setting SI to “H”. The data is then output in sync with the falling edge of SCLK.

Data transfer procedure

① Command code	91h (1 0 0 1 0 0 0 1)
② Address	(0 0 A5 . . . . A0)



OFRAM data read

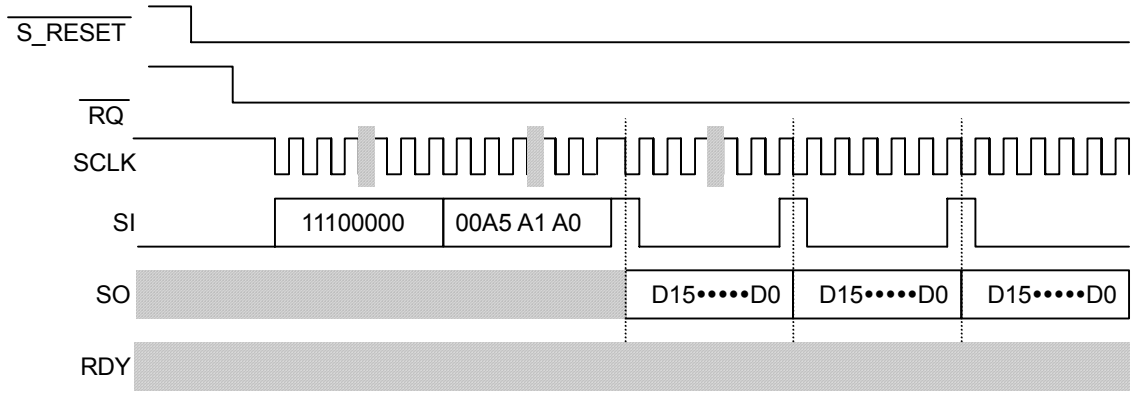
e) Hands-Free Parameter RAM Read (during reset)

Hands-Free program RAM reads require inputting a command code and address to be accessed and waiting for SCLK to fall after setting SI to “H”. The data is then output synchronized with the falling edge of SCLK.
When the requested read addresses are in consecutive locations, repeat the above procedure again by setting SI to “H”.

Read hands-free parameter RAM after writing “1” to HF_RST_N bit and HF bit in CONT5 register as shown in the page 71

Data transfer procedure

① Command code	E1h (1 1 1 0 0 0 0 1)
② Address	(0 0 A5 . . . . A0)



Hands-Free Parameter RAM Read

3) Writing During RUN

a) Coefficient RAM write preparation and write (under RUN condition)

This procedure is used to re-write the Coefficient RAM (CRAM) while a program is being executed. After inputting a command code, data for up to 16 consecutive addresses can be written.
Next, input a write command code and a starting address. Rewriting of the RAM contents is executed whenever a re-written address is assigned.
For example, this is how 5 writes are executed, starting at the Coefficient RAM address of " 10 ":

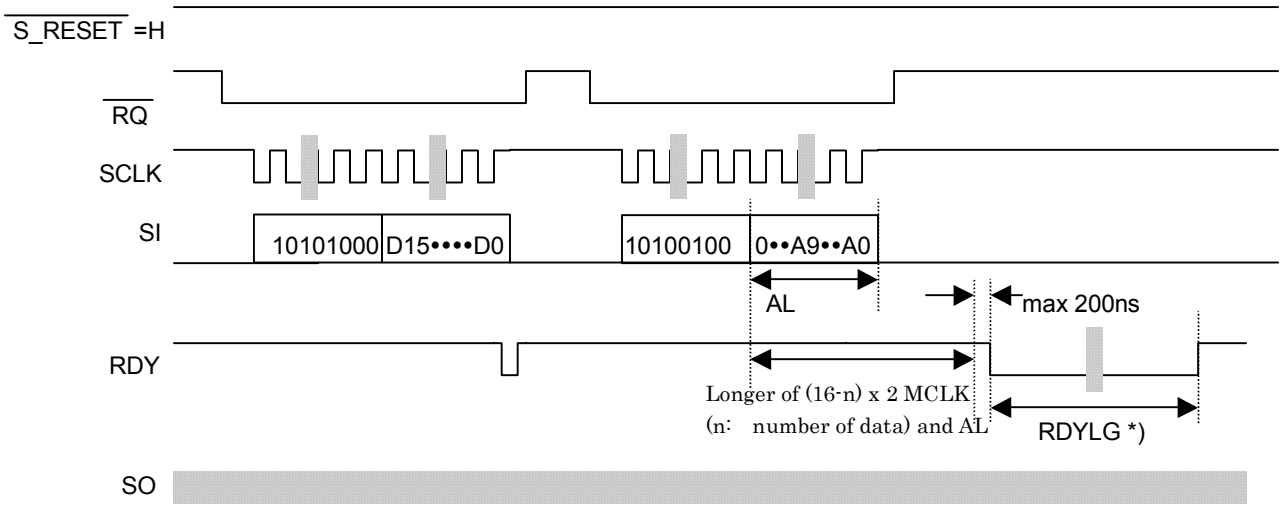
Coefficient RAM execution address	7	8	9	10	11	13	16	11	12	13	14	15
				↓	↓				↓	↓	↓	
write execution location				O	O	↑			O	O	O	

*) Note that address " 13 " is not processed until the data at address " 12 " is re-written.

Data transfer procedure

* Write preparation
① Command code A8h (1 0 1 0 1 0 0 0)
② Data (D15 • • • • • • D8)
③ Data (D7 • • • • • • D0)
* Write operation
① Command code A4h (1 0 1 0 0 1 0 0)
② Address upper (0 0 0 0 0 0 A9 A8)
③ Address lower (A7 • • • • • • A0)

Note) Be sure to follow the procedure of write preparation first, then write. An erroneous operation occurs if write is done without write preparation. "L" period of RDY for the write preparation is shorter than 1 master clock (20ns) under typical condition



*) RDYLG pulse width is 2 LRCLK clock time maximum if a program is so written to re-write a new address within a single sampling time. After this, RDY signal goes high.

CRAM Write Preparation and Write

b) Offset RAM Write Preparation and Write (under RUN condition)

This procedure is used to re-write Offset RAM (OFRAM) while a program is being executed. After inputting a command code, data at up to 16 consecutive addresses to be re-written can be input . Next, input a write command and a starting write address, and the re-write is executed whenever re-written address is assigned. For example, this is how 5 writes are executed, starting at the Offset RAM address of " 10 ":

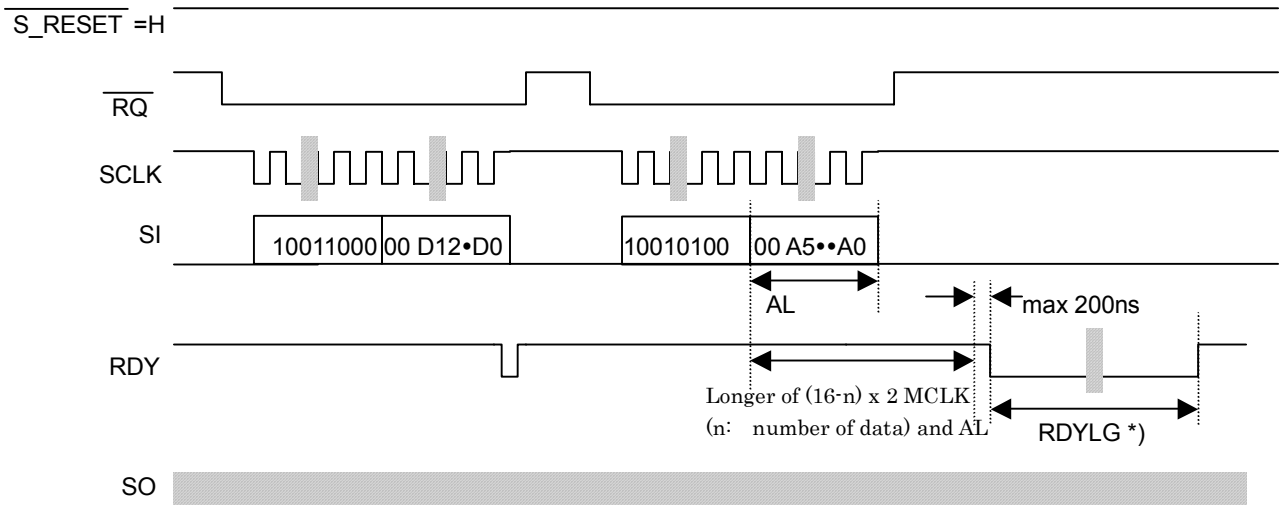
Offset RAM execution address	7	8	9	10	11	13	16	11	12	13	14	15
				↓	↓				↓	↓	↓	
write execution location				O	O	↑			O	O	O	

Be noted that address " 13 " is not processed until data at address " 12 " is re-written.

Data transfer procedure

* Write preparation
① Command code 98h (1 0 0 1 1 0 0 0)
② Data (0 0 0 0 0 0 0 0)
③ Data (0 0 0 D12 • • • D8)
④ Data (D12 • • • • • • D8)
* Write operation
① Command code 94h (1 0 0 1 0 1 0 0)
② Address MSB (0 0 A5 • • • • A0)

Note) Be sure to follow the procedure of write preparation first, then write. An erroneous operation occurs if write is done without write preparation. "L" period of RDY for the write preparation is shorter than 1 master clock (20ns) under typical condition



*) RDYLG pulse width is 2 LRCLK clock time maximum if a program is so written to surely re-write a new address within a single sampling time. After this, RDY signal rises to high.

ORAM Write Preparation and Write

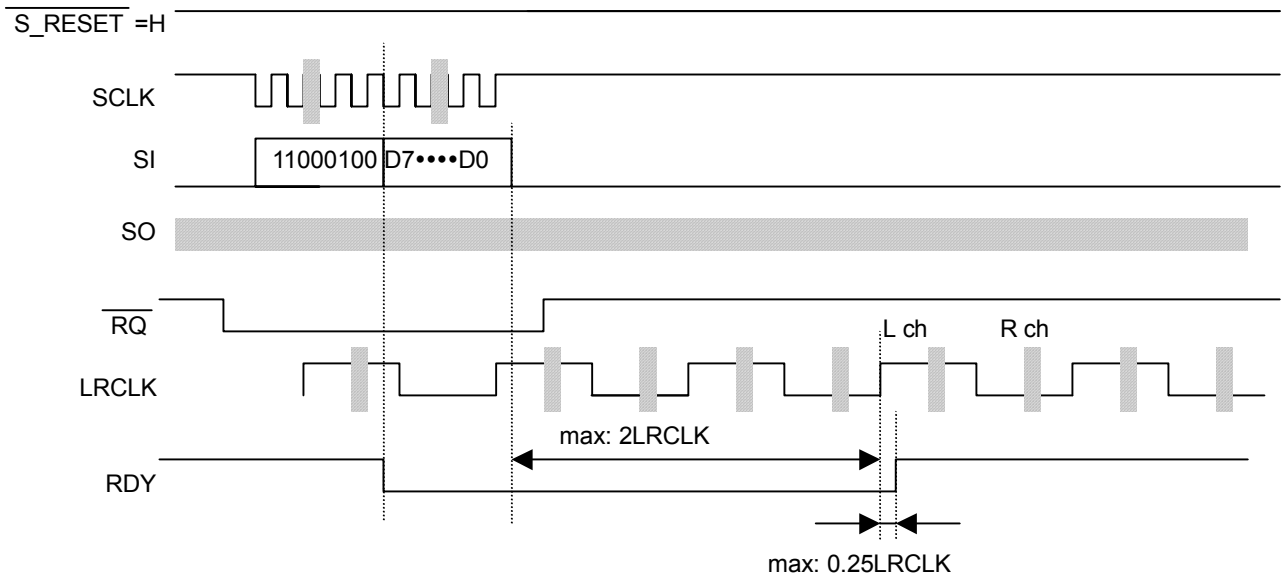
c) External Conditional Jump Code Write (under RUN condition)

External conditional jump code writes are executed in 2 bytes/set data.
It is possible to input during in both reset and normal operation modes. Input data is set to each assigned register at the rising edge of LCRCK.
RDY pin goes “L” after all data is transferred and it becomes “H” when the write operation is completed.
External jump code is 8-bits and when any bit of this code and any single bit of “1“ in the IFCON field matches, a jump instruction is executed.
Write from microprocessor is inhibited until RDY becomes “H”.

Note) please be noted that phase of LRCLK is inverted in case of I2S compatible interface mode.

Data transfer procedure

① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 D6 . . . . . A0)



External Conditional Jump Write Timing (during RUN)

4) Read During RUNNING

a) Control Register read out (during RUN)

It is possible to read out Control Registers in RUN mode. D7 ~ D1 control register values are output at the falling edge of SCLK after a command code is input. As no register exists at D0 location, “0” is always output until the 16th rising edge of SCLK.

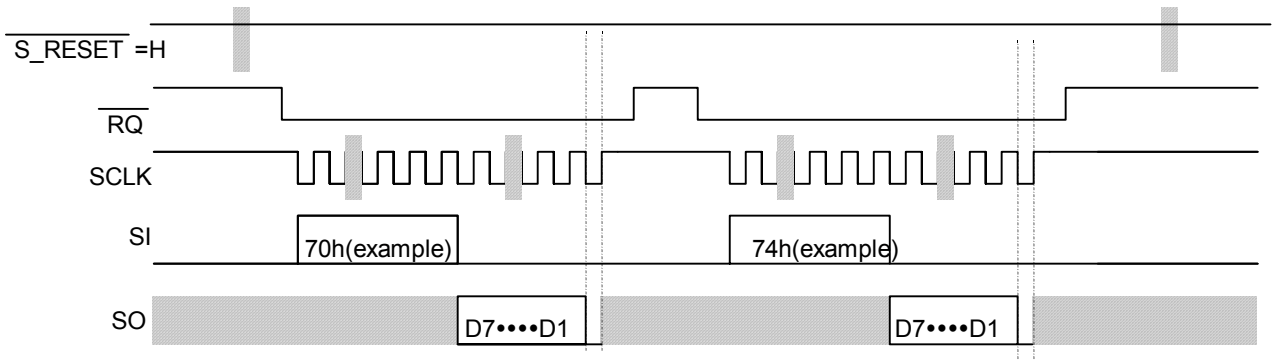
Note) when D0 data is taken at the 16th rising edge of SCLK, it is not necessarily always “0”, so please ignore the D0 value (as it is indeterminate after the 16th rising edge of SCLK).

Data transfer procedure

① Command code 70h,72h,74h,76h,78h,7Ah,7Ch,D8h,DAh,DCh

note) 50h,54h,58h are not used as they are for testing.

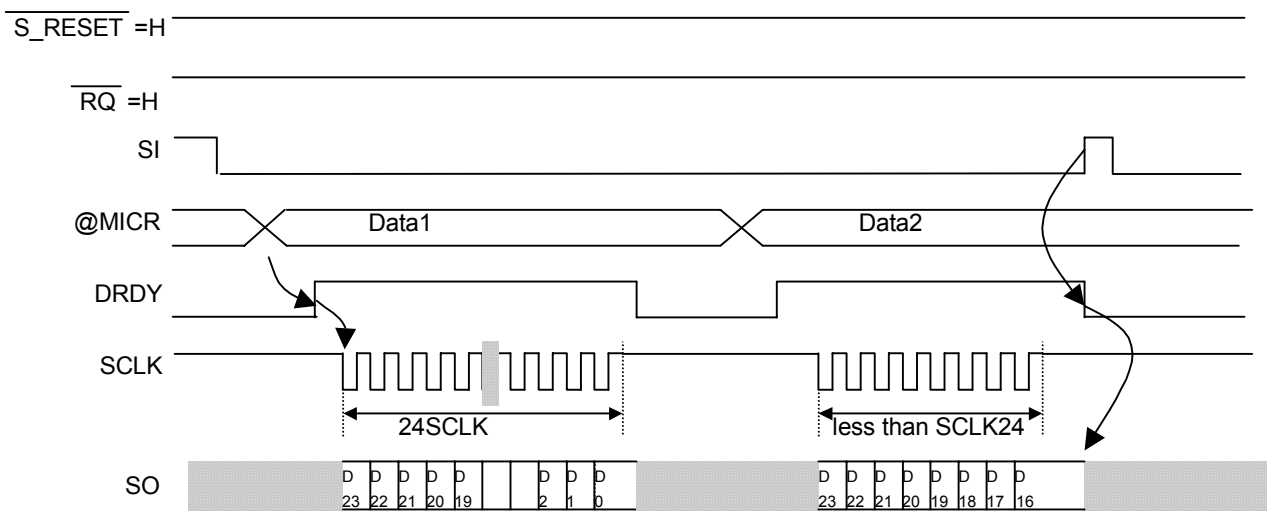
For each Bit function, please refer to section (2) Control Register Settings.



Example of Control Register Read

b) SO Read Out

SO can output data that is on the DSP Data Bus (DBUS).
Data is set using the @ MICR command and specifying a value in the DST field.
When the data is set, DRDY becomes “H” and data is output in sync with the falling edge of SCLK.
By setting SI to “H”, DRDY becomes “L” and waits for the next instruction.
Once DRDY becomes “H”, the @ MICR instruction data that sets DRDY “H” is retained until SI is set to “H” or until 24 bits of data are output by SCLK clock (DRDY becomes “L” after outputting 24 data bits), and no further @MICR instruction is accepted. Output on SO pins is 24-bits long maximum.



SO Read Out (during RUN)

5) Simplified Write Error Check

The AK7750 can easily check whether any error exists in the write data, using Cyclic Codes.
(Note: the main purpose of this is to check erroneous writes due to induced noise etc. caused between microprocessor and DSP. As this is a CRC-based (cyclic redundancy check) check, and as input data is checked before it is written into RAM and register, **it does not guarantee 100 % write error detection**).

Here definitions are made as follows :

- serial data D (x) : SI data being input during the time from $\overline{RQ}$ to fall to $\overline{RQ}$ to rise.
- Generator Polynomial $G(x)=x^{16}+x^{12}+x^5+1$ (default value = 0)
- remainder R (x), when D(X) is divided by G (x)

In order to perform a simplified write error check, perform the following:

1) Transfer serial data D(x) to be checked.
2) Write the remainder R(x) of serial data D(x) to register, using command code B6h.
3) Read out R(x) using command code D6h to check if it is correctly written (CRC check function operates even when no read is performed).
4) If the remainder of the serial data D(x) divided by G(x) is equal to R(x), SO outputs “H” at the rising edge of $\overline{RQ}$ until the following rising edge of $\overline{RQ}$ occurs for next serial data-write. When the SO output is used, as in the case of a read in RUN mode, there is a conflict. Therefore when a CRC check is done, do not execute read operation in RUN mode until the check is completed). If it is not equal to R(x), “L” is output.
5) If other serial data is to be checked, repeat 1) ~ 4) above.

■ Details of Data Transfer Procedure

1) Write the register

Writing remainder data R(x) is executed in 3 bytes/set data (24-bit).

Data translate order.

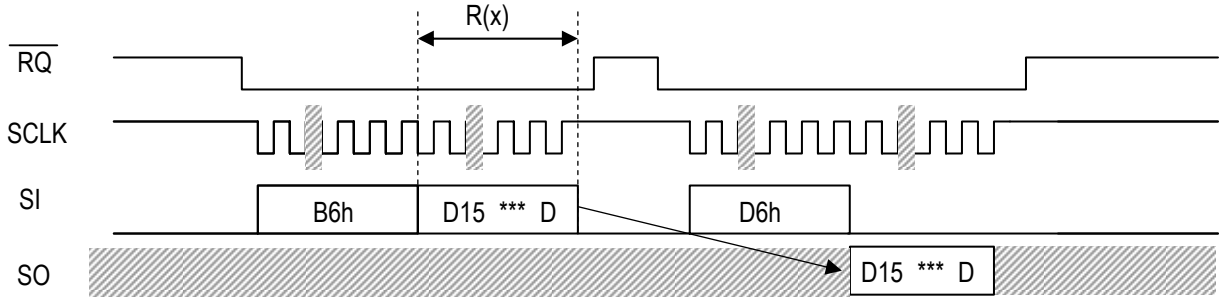
①Command code	B6h
②Upper 8bit of R(x)	(D15 * * * * * * D8)
③Lower 8bit of R(x)	(D7 * * * * * * D0)

2) Read out the register

Reading remainder data R(x) is executed in 3 bytes/set data (24-bit).

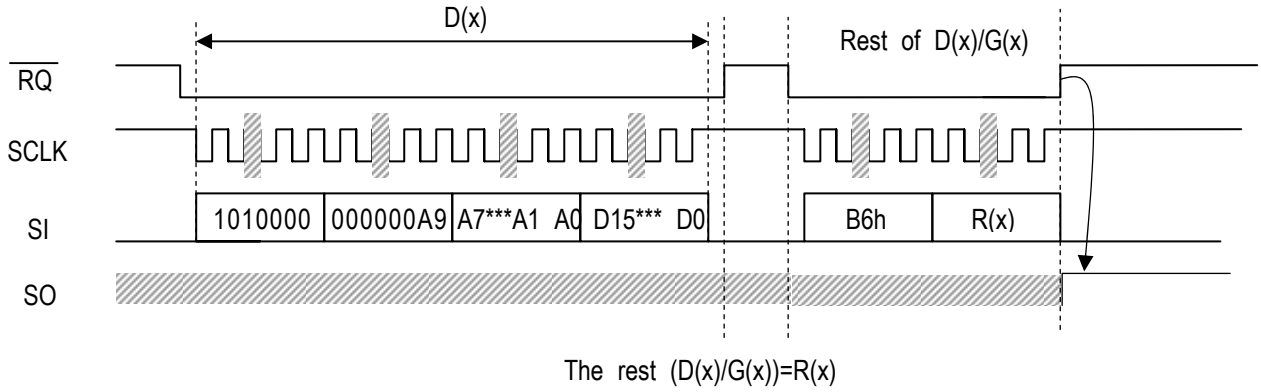
Data translate order

①Command code	D6h
②Upper 8bit of R(x)	(D15 * * * * * * D8)
③Lower 8bit of R(x)	(D7 * * * * * * D0)



Example: Control register writing, reading

3) CRC Check



The rest of D(x)/G(x)=R(x) CRC Check example.

4) Example of the R(x) made from D(x).

Examples	D(X)	R(X)
1	D6ABCDh	1E51h
2	D2A5A5h	0C30h
3	A855557777AAAA0000FFFFh	2297h

(8) ADC high-pass filter

The AK7750 incorporates a digital high-pass filter (HPF) for canceling DC offset in the ADC. The HPF cut-off frequency is about 1 Hz (fs = 48 kHz). This cut-off frequency is proportional to the sampling frequency (fs).

	48kHz	44.1kHz	32kHz	8kHz
Cut-off frequency	0.93Hz	0.86Hz	0.62Hz	0.16Hz

(9) EEPROM Interface

1) Using the EEPROM interface

Since the AK7750 has an integrate EEPROM interface, PRAM, CRAM, OFRAM and Control Register data can be loaded from the EEPROM after an initial RESET.
Use AKM's 64Kbit/12Kbit serial EEPROM, the AK6512C/14C, when using the AK7750..
The data listed in section 2) Program Map, should be written into the EEPROM.

The following operations are required when using the EEPROM.

- Set EESEL pin to "H", (after reaching a proper oscillation when a crystal oscillator is used) and set $\overline{\text{INIT\_RESET}}$ pin to raise "H". Then internal counter starts to run which generates EEPROM control signals $\overline{\text{EECS}}$, EESK and EESI, and EEPROM data is taken from EESO pin.
- After taking all data, EESK and EESI become "L" and $\overline{\text{EECS}}$ to "H". EEST pin rises from "L" to "H", informing that loading has been completed. When EEST becomes "H", interface with microprocessor is enabled with EESEL pin as it stands at "H". When reading is required again, set $\overline{\text{INIT\_RESET}}$ pin to "H" after executing initial reset ($\overline{\text{INIT\_RESET}}$ = "L") with EESEL kept at "H".

  Note that hands-free parameters can not be downloaded via EEPROM interface.

2) Program map

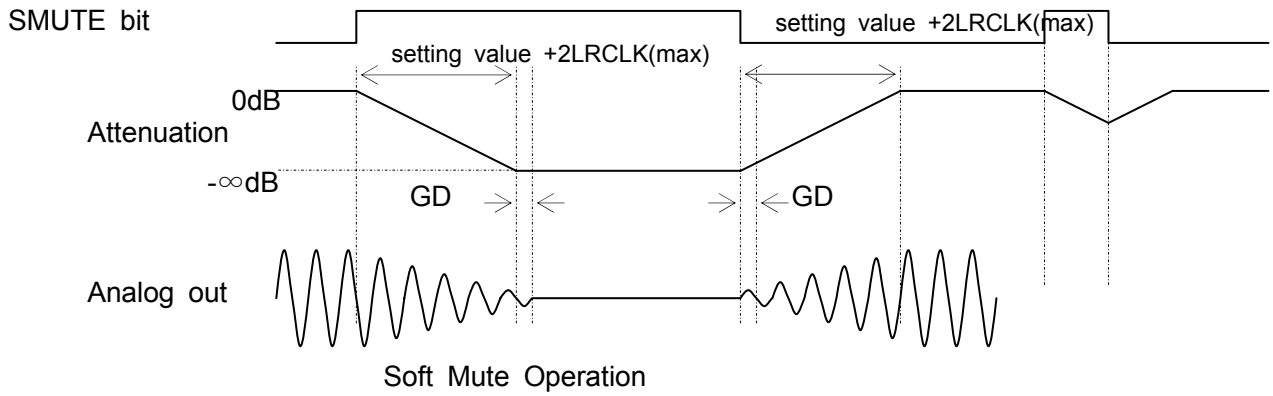
EEPROMADDRESS	DATA	Note
0000h	C0h	PRAM WRITE command code
0001h	00h	PRAM address MSB side
0002h	00h	PRAM address LSB side
0003h	PRAM0 DATA31-24	PRAM address 0 MSB 8bit data
0004h	PRAM0 DATA23-16	PRAM address 0 MSB-1 8bit data
0005h	PRAM0 DATA15-8	PRAM address 0 MSB-2 8bit data
0006h	PRAM0 DATA7-0	PRAM address 0 LSB 8bit data
0007h	PRAM1 DATA31-24	PRAM address 1 MSB 8bit data
●●●●	●●●●	
0BFEh	PRAM766 DATA7-0	PRAM address 766 LSB 8bit data
0BFFh	PRAM767 DATA31-24	PRAM address 767 MSB 8bit data
0C00h	PRAM767 DATA23-16	PRAM address 767 MSB-1 8bit data
0C01h	PRAM767 DATA15-8	PRAM address 767 MSB-2 8bit data
0C02h	PRAM767 DATA7-0	PRAM address 767 LSB 8bit data
0C03h	A0h	CRAM WRITE command code
0C04h	00h	CRAM address MSB side
0C05h	00h	CRAM address LSB side
0C06h	CRAM0 DATA15-8	CRAM address 0 MSB 8bit data
0C07h	CRAM0 DATA7-0	CRAM address 0 LSB 8bit data
0C08h	CRAM1 DATA15-8	CRAM address 1 MSB 8bit data
●●●●	●●●●	
1403h	CRAM1022 DATA7-0	CRAM address 1022 LSB 8bit data
1404h	CRAM1023 DATA15-8	CRAM address 1023 MSB 8bit data
1405h	CRAM1023 DATA7-0	CRAM address 1023 LSB 8bit data
1406h	90h	OFRAM WRITE command code
1407h	00h	OFRAM address
1408h	OFRAM0 DATA23-16	OFRAM address 0 MSB 8bit data
1409h	OFRAM0 DATA15-8	OFRAM address 0 MSB-1 8bit data
140Ah	OFRAM0 DATA7-0	OFRAM address 0 LSB 8bit data
140Bh	OFRAM1 DATA23-16	OFRAM address 1 MSB 8bit data
●●●●	●●●●	
1494h	OFRAM46 DATA7-0	OFRAM address 46 LSB 8bit data
1495h	OFRAM47 DATA23-16	OFRAM address 47 MSB 8bit data
1496h	OFRAM47 DATA15-8	OFRAM address 47 MSB-1 8bit address
1497h	OFRAM47 DATA7-0	OFRAM address 47 LSB 8bit address
1498h ~ 1519A	00h	Reserved
151Ah	60h	CONT0 WRITE command code
151Bh	DATA	CONT0 data
151Ch	62h	CONT1 WRITE command code
151Dh	DATA	CONT1 data
151Eh	64h	CONT2 WRITE command code
151Fh	DATA	CONT2 data
1520h	66h	CONT3 WRITE command code
1521h	DATA	CONT3 data
1522h	68h	CONT4 WRITE command code
1523h	DATA	CONT4 data
1524h	6Ah	CONT5 WRITE command code
1525h	DATA	CONT5 data
1526h	6Ch	CONT6 WRITE command code
1527h	DATA	CONT6 data
1528h	B6h	CRC WRITE command code
1529h	CRC DATA15-8	CRC MSB 8bit data
152Ah	CRC DATA7-0	CRC LSB 8bit data

(10) DAC Soft Mute Operation

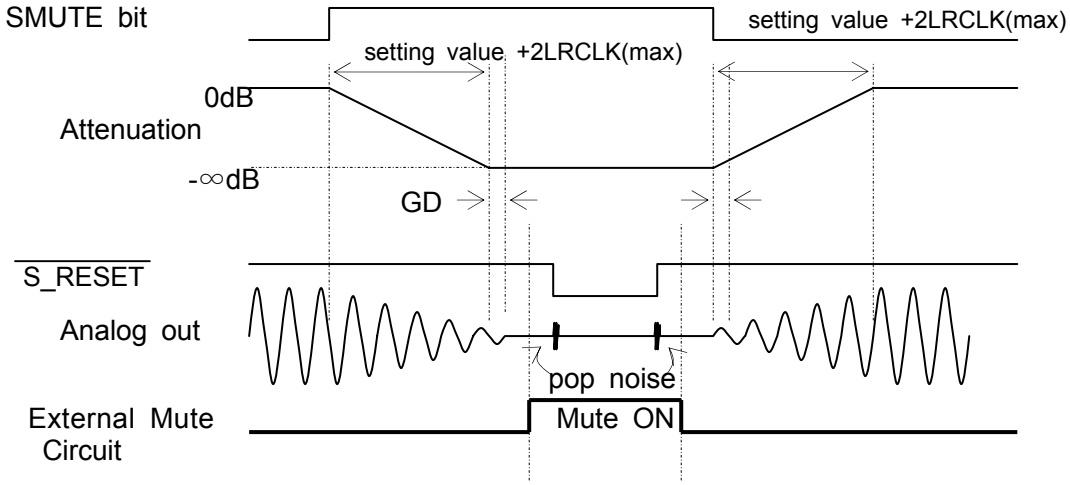
DAC block in the AK7750 includes soft mute circuit.

Soft mute operation is performed at digital domain. When the SMUTE bit goes to “1”, the output signal is attenuated from 0dB level to -∞ level during the LRCLK cycle time that is specified by SF1 bit and SF0 bit in CONT5 register plus additional 2LRCLK cycle time(max). When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to 0dB level by the same cycle. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to 0dB by the same cycle. The soft mute is effective when $\overline{\text{S\_RESET}}$ is “H” (DAC opeates normally) External mute circuit is recommended to suppress the pop noise at the reset.

Attenuation value is initialized by $\overline{\text{INIT\_RESET}}$ ="L", not $\overline{\text{S\_RESET}}$ ="L"



Soft Mute Operation



Example of soft mute control@ $\overline{\text{S\_RESET}}$ ="H"

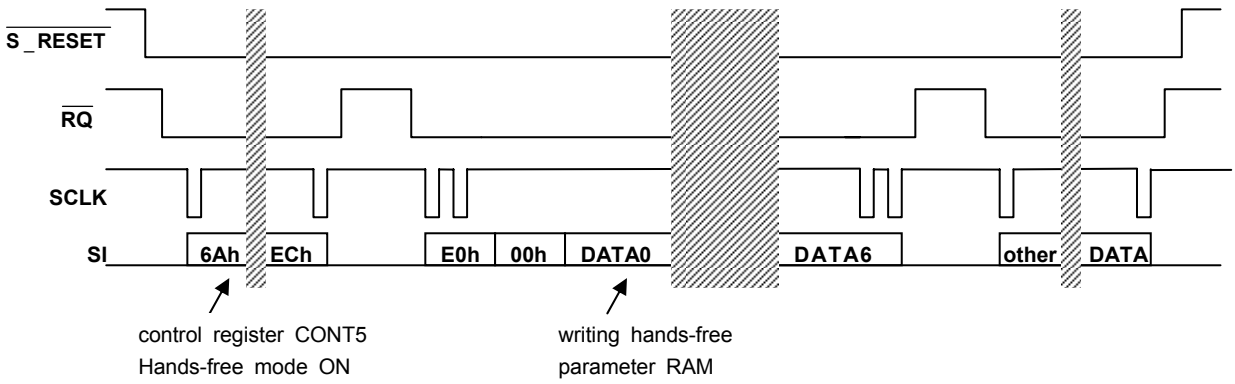
(11) Hands-free mode

The AK7750 has hands-free mode in addition to normal surround mode.
The write “1” to HF_RST_N bit and HF bit in CONT5 register under system reset ($\overline{\text{S\_RESET}}$ =”L”) allows the AK7750 to hands-free operation mode. The AK7750 returns to surround mode by the execution of initial reset or the clear of HF_RESETN bit and HF bit.

The AK7750 can change the attenuation level of noise canceller. If PID bit of CONT5 register is “0”, the default attenuation level is used. If PID bit is “1”, the attenuation level which is stored in the hands-free parameter RAM is used.

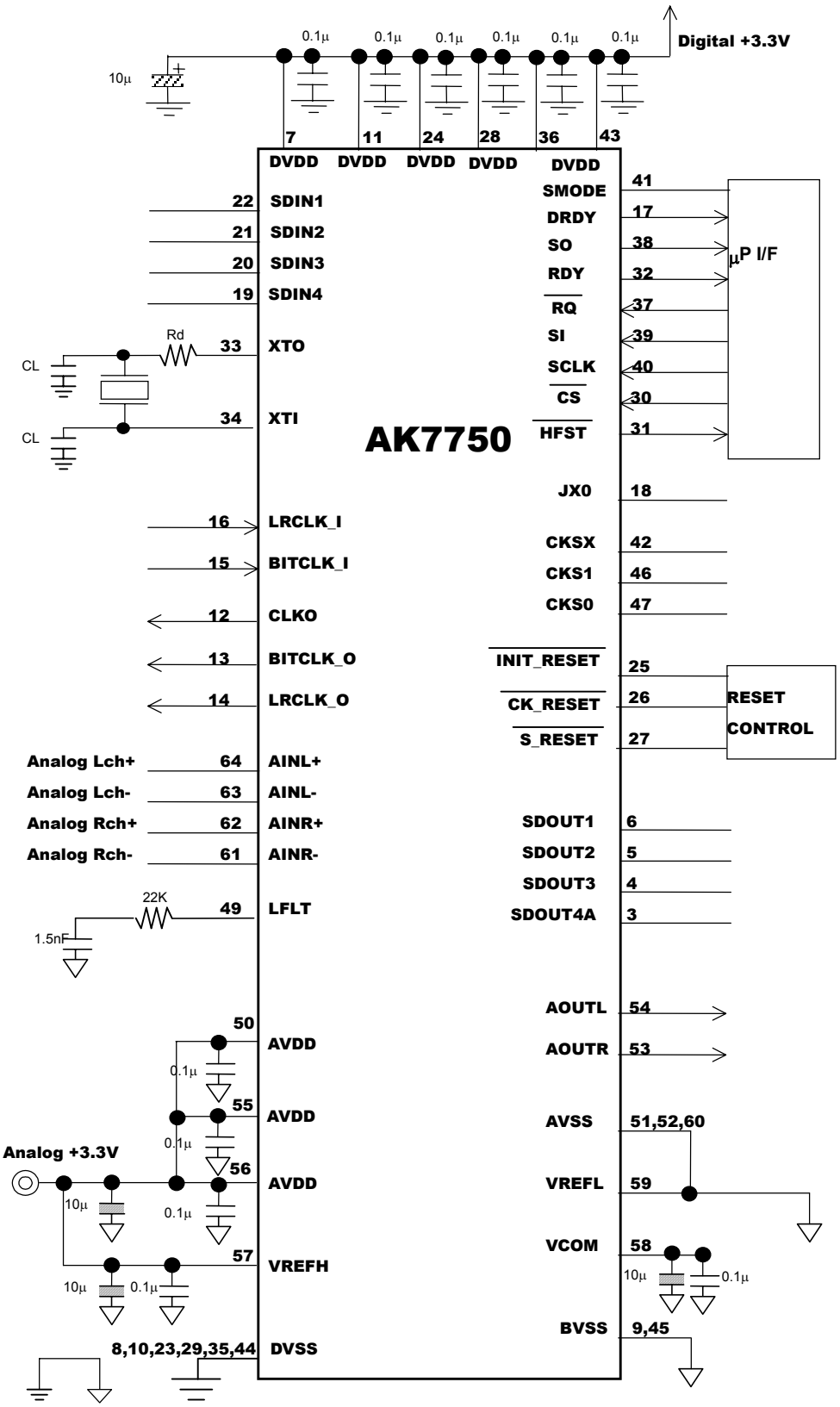
Hands-free parameter must be downloaded to the address AFTER the AK7750 switches to hands-free mode.

Please contact AKM for the detail of hands-free parameter contents.



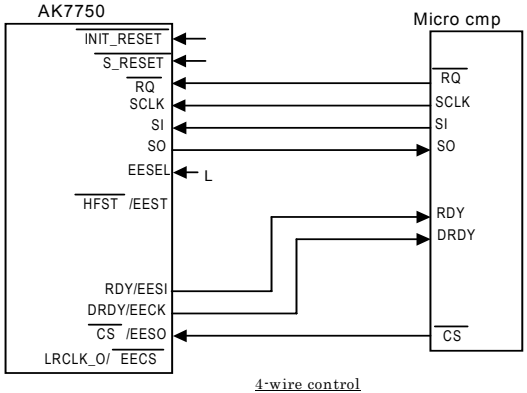
9. System Design

(1) Connection example

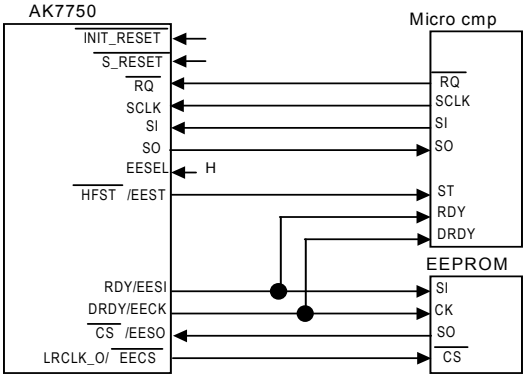


(2) Periphery Circuit

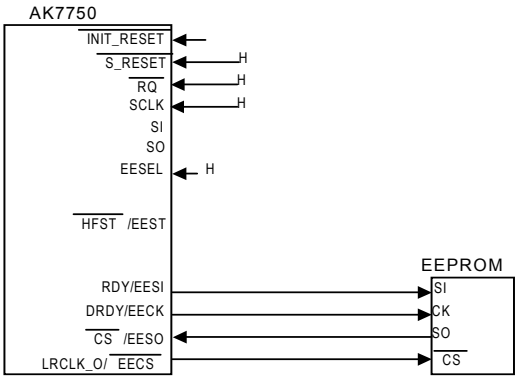
1) Connection with EEPROM



4-wire control



4-wire control + EEPROM



EEPROM only

2) Grounding and Power Supply

When designing with the AK7750, AVDD and DVDD are separately decoupled in order to minimize digital noise. System Analog power supply is fed to AVDD. In general, power supply lines and ground lines are separately wired for the analog and digital portions, and they are connected together near the power supplies (terminals) on the printed circuit board. Small ceramic de-coupling capacitors should be connected as close as possible to the AK7750.

3) Reference Voltage

An input voltage difference between VREFH pin and VREFL pin determines the analog full scale input and output. Normally, AVDD is connected to VREFH and AVSS to VREF.
In order to eliminate high frequency noise, connect a 10 uF electrolytic capacitor and a 0.1 uF ceramic capacitor in parallel between VREFH and AVSS . The ceramic capacitor should be connected as close as possible to this pin. Digital signals, especially clocks should be wired as far as possible from the VREFH and VREFL pins in order to avoid coupling with the AK7750.

The AK7750 common voltage is output on VCOM. Do not use this VCOM common voltage for connection with any external circuits. To eliminate high frequency noise, connect a 10-uF electrolytic capacitor and a 0.1 uF ceramic capacitor between VCOM and AVSS. These capacitors should be placed as close as possible to the VCOM pin.

4) Analog Input

An analog signal is input to the internal modulator through differential input pins for each channel.
The input voltage range is equal to difference in voltage between AIN+ and AIN- (ΔVAIN = (AIN+) – (AIN-)), and equals $\pm$FS = $\pm$(VREFH – VREFL) x 0.4. When VREFH = 3.3 V and VREFL = 0.0 V, input range is $\pm$1.32 V. Output code format is in 2's complement.

In the AK7750, the analog input is sampled at 3.072 MHz when fs = 48 KHz. A digital filter rejects noise ranging from 30 KHz to 3.042 MHz. Noise around the 3.072 MHz periphery band is not rejected. As no audio signals exhibit noise near 3.072 MHz, noise can be sufficiently attenuated using a simple RC filter.

Analog input signal to the AK7750 must be biased as shown in Figure 1

Analog power supply voltage of the AK7750 is + 3.3 V (typ).
Voltages higher than AVDD + 0.3 V & lower than AVSS – 0.3 V and current exceeding 10 mA should not be applied on the analog input pins (AINL+, AINL-, AINR+, AINR-).
Injection of excessive current may destroy the internal protection circuits and may cause a latch-up that results in total device destruction.
Therefore if $\pm$15 V power supplies are used in peripheral analog circuits, the analog input pins must be protected from signals exceeding absolute maximum ratings.

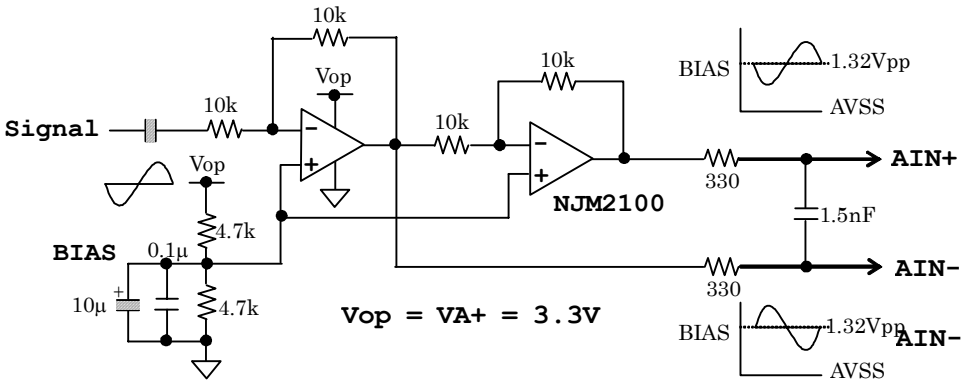


Fig.1 Input Buffer Circuit Example (Differential input)

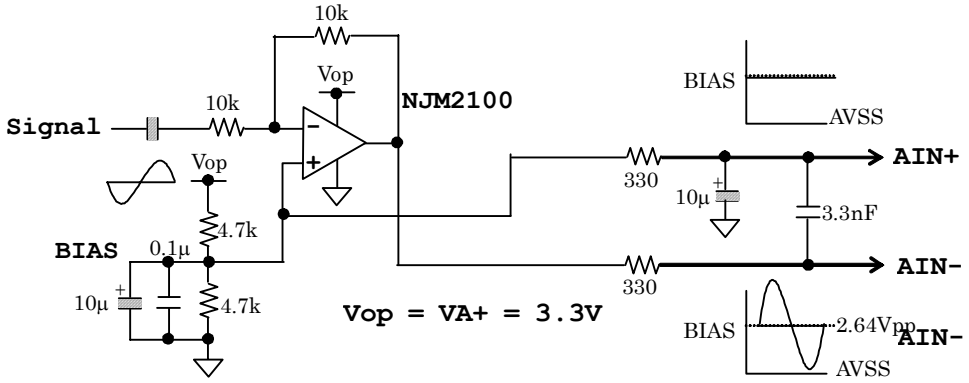


Fig.2 Input Buffer Circuit Example (Single-Ended input)

The AK7750 can also receive single-ended analog signals. In this case, the analog signal is fed to the AIN- input pin (FS = (VREFH – VREFL) x 0.8= 2.64 Vp-p at VREFH = 3.3 V, VREFL = 0.0 V), and a bias voltage is fed to the AIN+ input pin. When 3.3 V OP amps are used in, low-saturation type OP amps are recommended. An electrolytic capacitor connected to AIN+ pin is effective in lowering secondary harmonics (refer to Figure 2).

5) Analog Output

The analog output is single-ended. Output range is 2.00 Vp-p (typ) centered on VCOM.
The Out-of-Band noise (shaping noise) generated by an internal delta-sigma modulator is attenuated by an on-chip switched capacitor filter (SCF) and a continuous time filter (CTF). Therefore it is not necessary to add an external filter for normal use. If ADC without anti-aliasing input filter is connected to DAC's output directly, the spurious noise may be appear. In this case, the insertion of low pass filter that has fo< 20kHz, 2nd order (>12dB/oct) is effective.

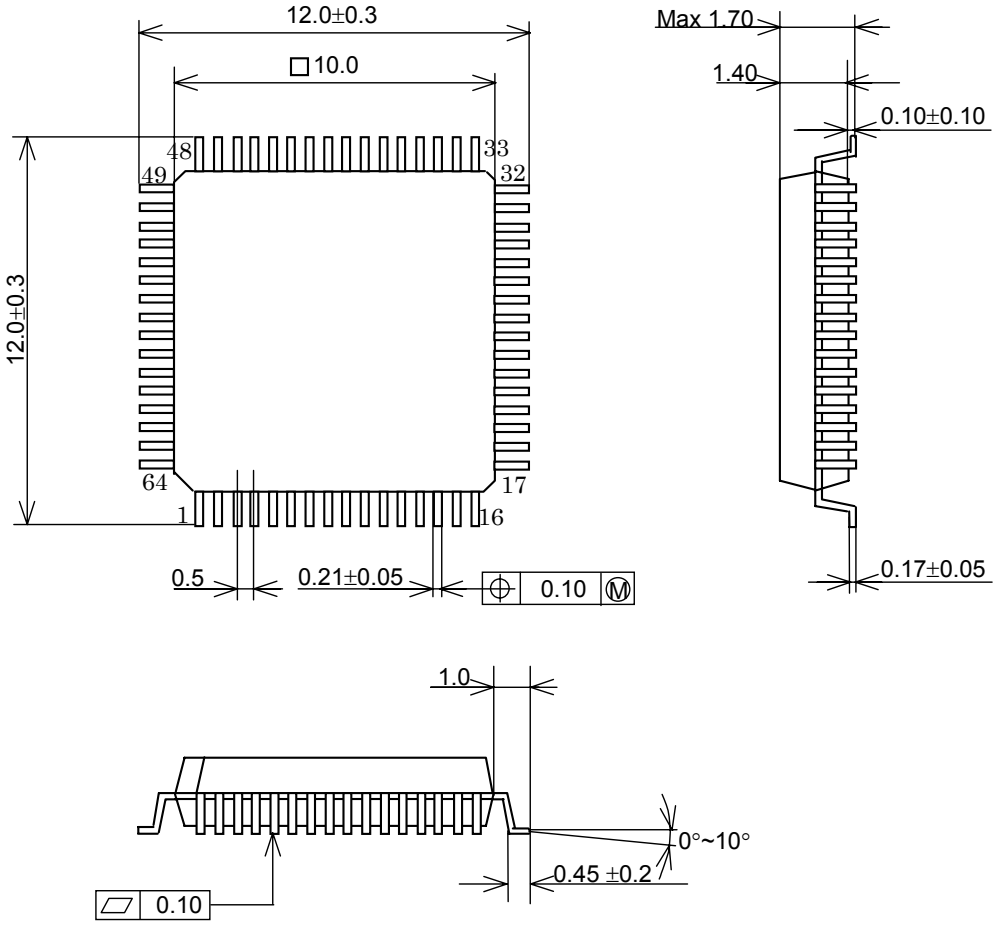
The input code format is in 2's complement. Positive full-scale output corresponds to 7FFFFFh (@ 24 Bit) input code, Negative full scale is 800000h (@ 24 Bit) and VCOM voltage ideally is 000000h (@ 24 Bit).

6) Connection with Digital Circuit

In order to minimize noise caused by Digital circuits, use low voltage logic ICs to connect the digital outputs. Recommended logic families are 74LV, 74LV-A, 74ALVC and 74AVC series ICs.

Package

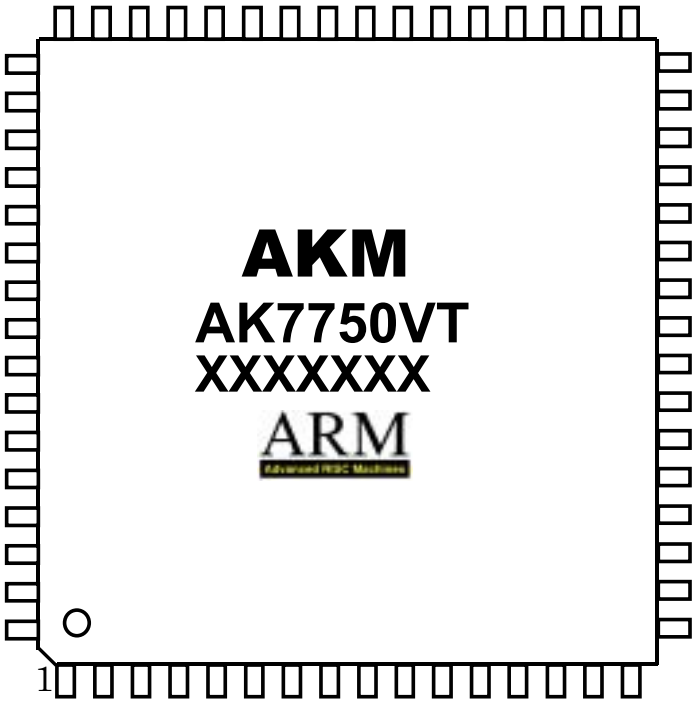
64pin LQFP (Unit: mm)



- Material & Lead finish

Package:	Epoxy
Lead-frame:	Copper
Lead-finish:	Soldering plate (Pb free)

Marking



1) Pin #1 indication
2) ARM Logo
3) Date Code: XXXXXXX(7 digits)
4) Marking Code: AK7750VT
5) Asahi Kasei Logo