PA2423L-EK1

RangeCharger™ 2.4 GHz Bluetooth™ Power Amplifier Evaluation Kit

Application

- Bluetooth™
- USB dongles
- PCMCIA, flash cards
- Access points
- 2.4 GHz cordless telephones

Features

- Easy evaluation of the PA2423L Power Amplifier
- Low Cost Design – 8 components required
- Minimum board space required – 340 mils x 220 mils
- High Output Power – 22.5 dBm
- Schematic and layout ready for production builds
- Lead free 6 pin QFN Package

Order Information

Part Number	Package	Remark
PA2423L	6 pin – QFN	Samples
PA2423L-R	6 pin – QFN	Tape & Reel
PA2423L-EK1	Evaluation Kit	

Product Description

The PA2423L-EK1 evaluation kit provides an easy to use, self-contained system for evaluating the RF performance and DC parameters of the PA2423L amplifier.

The PA2423L evaluation board requires minimal board area and components and in addition, it has been designed to allow the PA2423L to meet the Bluetooth™ Class 1 wireless technology specifications, with particular attention to gain and output power.

Each evaluation kit contains:

- Pre-assembled evaluation board with input & output matching networks. Standard SMA connectors for interconnection to test equipment
- A test report of the delivered board
- A PA2423L datasheet
- A PA2423L-EK1 data sheet

Functional Block Diagram

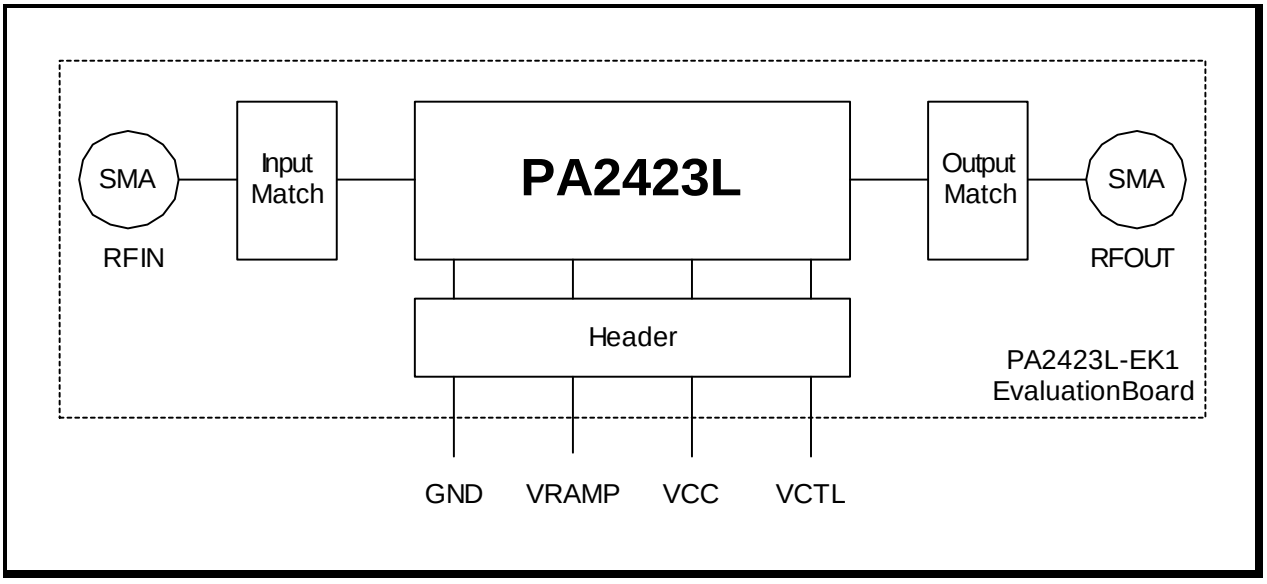


Figure 1: PA2423L-EK1 Evaluation Board Block Diagram

QA011805

Evaluation Board Schematic

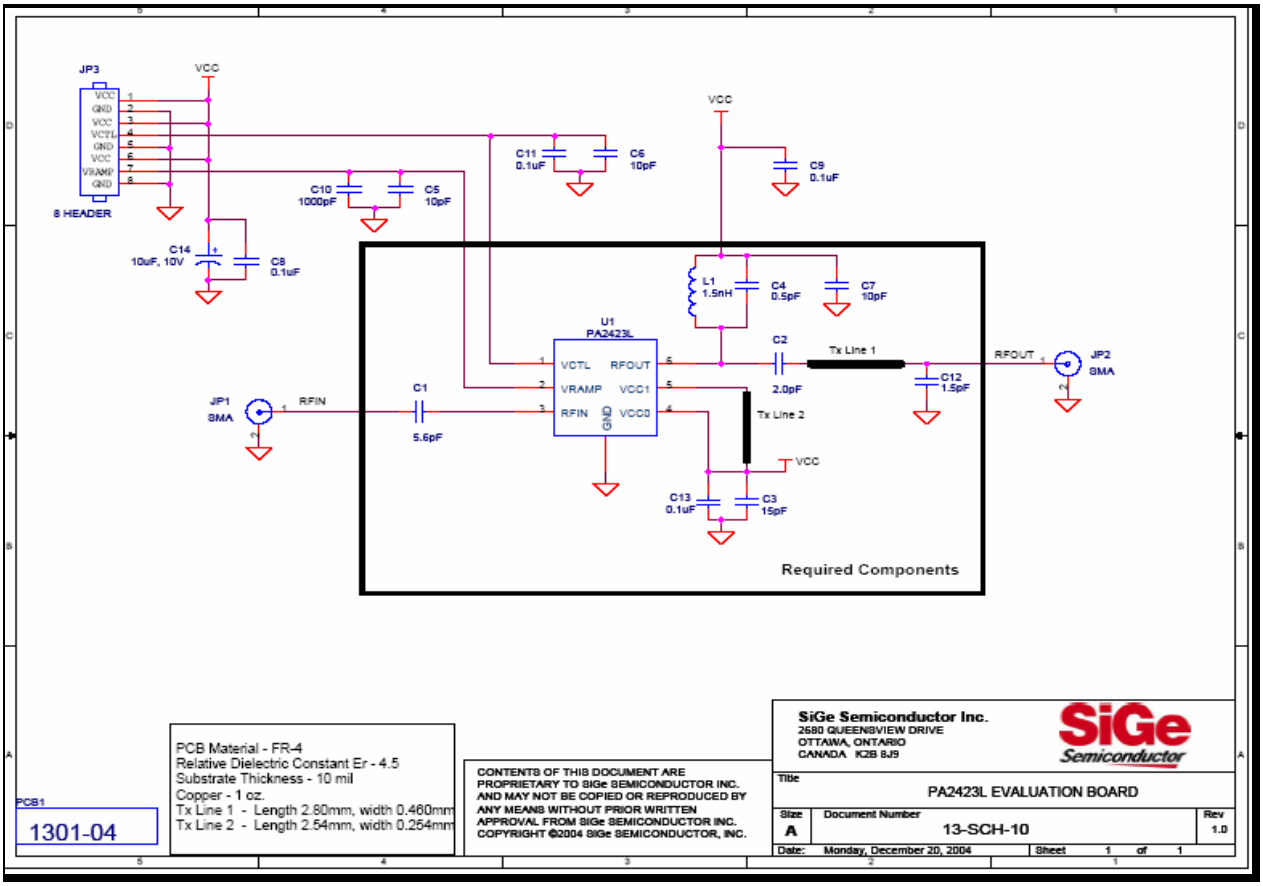


Figure 2: PA2423L Evaluation Board Schematic Diagram

Please Note: The RFOUT connector forms part of the output match of the power amplifier.

Pin	Pin Number	Description	Recommended setting
VCC	1	Supply Voltage	Connect system supply voltage
GND	2	Ground	Connect to system ground
VCC	3	Supply Voltage	Use this VCC to connect to VCTL signal with a shorting link
VCTL	4	Power and Gain Control	Connect to 3.3 V (VCC) for maximum gain and power output. For power control connect to a variable voltage source between 0 V and 3.3 V.
GND	5	Ground	Provided as a ground connection for the VCTL signal.
VCC	6	Supply Voltage	Use this VCC to connect to VRAMP signal with a shorting link
VRAMP	7	PA Enable Pin	0 V – 1.5 V applied = Device Disabled 2 V – VCC applied = Device Enabled
GND	8	Ground	Provided as a ground connection for the VRAMP signal

Table 1: Power and Analog I/O Header (JP3)

Note: It is recommended to use proper engineering connection practices by making RF and digital connections prior to turning on the power supply.

Evaluation Board Bill of Materials

The following components are used in the design of the PA2423L-EK1 evaluation board. As a reference, potential suppliers of these components are provided. SiGe Semiconductor does not endorse any specific vendor. In most cases, similar components from other suppliers will provide satisfactory performance.

The minimum required components, as defined inside the heavy black box in the schematic (Figure 2), are designated as 'required components'. These components are detailed in Table 2. Please note, that all components are dual sourced. Table 3 identifies an alternate supplier for the components.

Item	Reference	Qty	Part	Tolerance	Footprint	Type	Supplier	Supplier Part No
1	C1	1	5.6pF	5%	0402	NPO	Murata	GRP1555C1H5R6DZ01
2	C2	1	2.0pF	5%	0402	NPO	Murata	GRP1555C1H2R0CZ01
3	C3	1	15pF	5%	0402	NPO	Murata	GRP1555C1H150JZ01
4	C4	1	0.5pF	5%	0402	NPO	Murata	GRP1555C1HR50CZ01
5	C5,C6,C7	3	10pF	5%	0402	NPO	Murata	GRP1555C1H100JZ01
6	C8	1	0.1uF	80%/-20%	0603	Y5V	Murata	GRM188F51E104ZA01
7	C9,C13	2	0.1uF	80%/-20%	0402	Y5V	Murata	GRP155F51C104ZA01
8	C10	1	1000pF	10%	0402	X7R	Murata	GRP155R71H102KA01
9	C11	1	0.1uF	10%	0402	X5R	Murata	GRP155R61C104KA01
10	C12	1	1.5pF	5%	0402	NPO	Murata	GRP1555C1H1R5CZ01
11	C14	1	10uF, 10V	20%	-	Tantalum	Panasonic	ECS-T1AX106R
12	JP1,JP2	2	SMA	-	-	-	Johnson	142-0701-886
13	JP3	1	8 HEADER	-	-	-	8 Pin 0.1 inch Header	-
14	L1	1	1.5nH	10%	0402	Multilayer	Toko	LL1005-FHL1N5S
15	PCB1	1	1301-04	-	-	-	SiGe	-
16	U1	1	PA2423L	-	6-QFN	-	SiGe	-

Table 2: PA2423L Bill of Materials

Item	Reference	Qty	Part	Tolerance	Footprint	Type	Alternate Source	Alternate Source Part No
1	C1	1	5.6pF	5%	0402	NPO	Phycomp	0402CG569C9B200
2	C2	1	2.0pF	5%	0402	NPO	Phycomp	0402CG209C9B200
3	C3	1	15pF	5%	0402	NPO	Phycomp	0402CG150J9B200
4	C4	1	0.5pF	5%	0402	NPO	Phycomp	0402CG508C9B200
5	C5,C6,C7	3	10pF	5%	0402	NPO	Phycomp	0402CG100J9B200
6	C8	1	0.1uF	80%/-20%	0603	Y5V	Phycomp	06032F104Z8B20D
7	C9,C13	2	0.1uF	80%/-20%	0402	Y5V	Phycomp	04022F104Z7B20D
8	C10	1	1000pF	10%	0402	X7R	Phycomp	04022R102K9B200
9	C11	1	0.1uF	10%	0402	X5R	-	-
10	C12	1	1.5pF	5%	0402	NPO	Phycomp	0402CG159C9B200
11	C14	1	10uF, 10V	20%	-	Tantalum	-	-
12	JP1,JP2	2	SMA	-	-	-	-	-
13	JP3	1	8 HEADER	-	-	-	-	-
14	L1	1	1.5nH	10%	0402	Multilayer	-	-
15	PCB1	1	1301-04	-	-	-	-	-
16	U1	1	PA2423L	-	6-QFN	-	-	-

Table 3: PA2423L Bill of Materials Alternate Component Supplier

Test Equipment Required

The following test equipment is recommended when using the PA2423L-EK1:

- One pulse generator capable of generating pulses up to 10 kHz, 0 V to 3.3 V.
- Two power supplies capable of delivering 200 mA, 3.6 V for VCTL and VCC.
- One RF signal generator with output signal up to 2.5 GHz, +6 dBm.
- One spectrum analyzer that can measure signals up to 8 GHz.
- Two SMA 3 dB pads.
- Two 20 dB couplers.
- One dual head power meter.

Test Equipment Setup

1) Ensure that all power supplies are OFF and signal generator output is OFF.
2) Set the power meter frequency to 2.45 GHz and apply appropriate offsets compensating for test setup losses.
3) Set the power supply VCC and VCTL voltage to 3.3 V.
4) Connect the evaluation board to the test equipment as shown in Figure 3.
5) Turn ON power supply VCC and VCTL.
6) Pull up VRAMP to VCC by shorting Pin2 and Pin3 of JP3 with the female jumper.
7) Switch the RF output of the signal generator to ON and adjust the signal generator output power to get 0 dBm at the input to the evaluation board.
8) The power meter should measure approximately 22.5 dBm.
9) Sweep the input power level from -25 dBm to 0 dBm to get a P_{OUT} and I_{CC} vs. P_{IN} graph.
10) Pull VRAMP down to GND by shorting Pin1 and Pin2 of JP3 with the female jumper.
11) Measure I_{STDBY} and $|S_{21}|_{OFF}$.
12) With VRAMP pulled up to VCC, observe 2nd and 3rd harmonics generated by PA2423L.
13) Connect the SYNC output of the pulse generator to the trigger input of the spectrum analyzer and oscilloscope. Connect VRAMP to the Pulse Generator with square wave output of 0-VCC pk-pk, use the oscilloscope to set the waveform amplitude. See Figure 4 for the eqipment setup.
14) Reduce span on the spectrum analyzer to 0 Hz, set the oscilloscope and spectrum analyzer trigger to external and reduce sweep time to 50 µsec.
15) With the RBW and VBW set to maximum on the spectrum analyzer (if set too low this will limit the speed of the rising and falling edges) the rising and falling times of the RF output signal pulse can be measured. Rising edge and Falling edges should be <1 µsec.

The RF input signal is applied to the RFIN SMA connector on the application board. It is recommended to keep this signal level below +8 dBm to avoid possible PA damage. The PA output is taken from the board's "RFOUT" SMA connector. The amplifier evaluation board has been designed to interface directly with a 50 Ohm source and load impedance for measurement. The matching components used on the application board are low-loss, high Q components to minimize RF loss.

Note: Applying the wrong polarity to the evaluation board will damage the power amplifier.

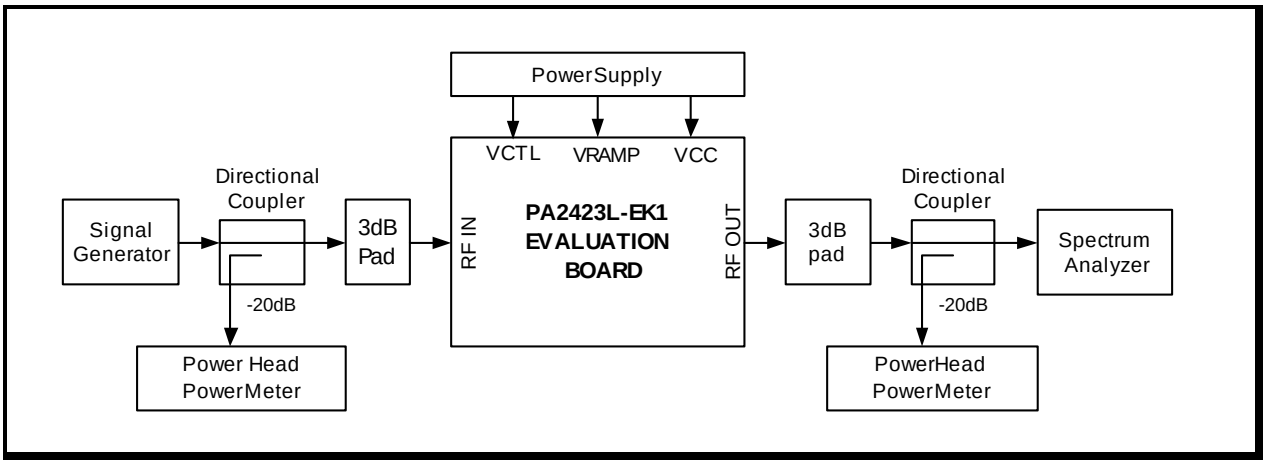


Figure 3: Test Equipment Setup for Static Measurement

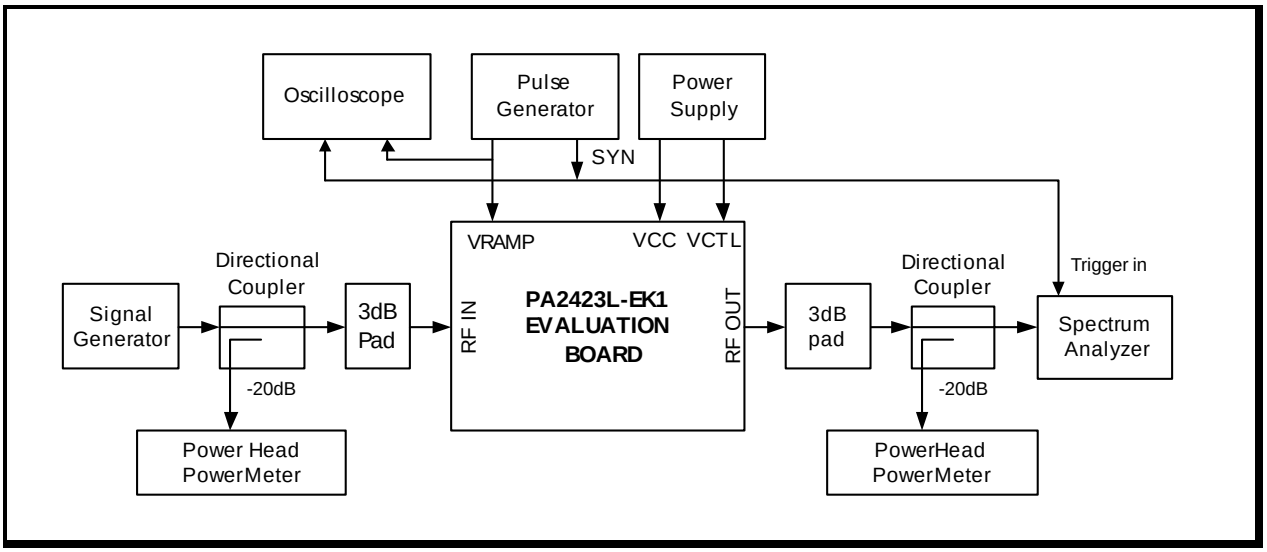


Figure 4: Test Equipment Setup for Dynamic Measurement

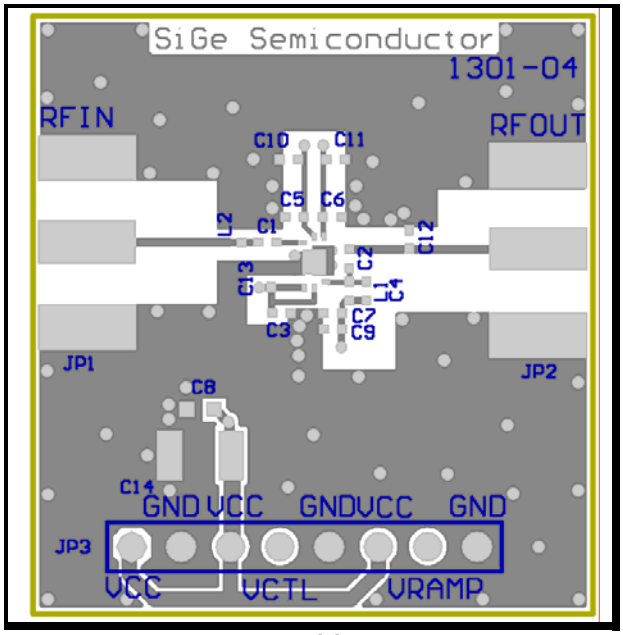
Layout

Optimum layout of the application board is critical; the input and output matching networks are layout dependent and will affect gain, output power, power added efficiency, current consumption and harmonics generation. The connectors do form part of the input and output network. The routing to Vcc1 forms the interstage match for the power amplifier.

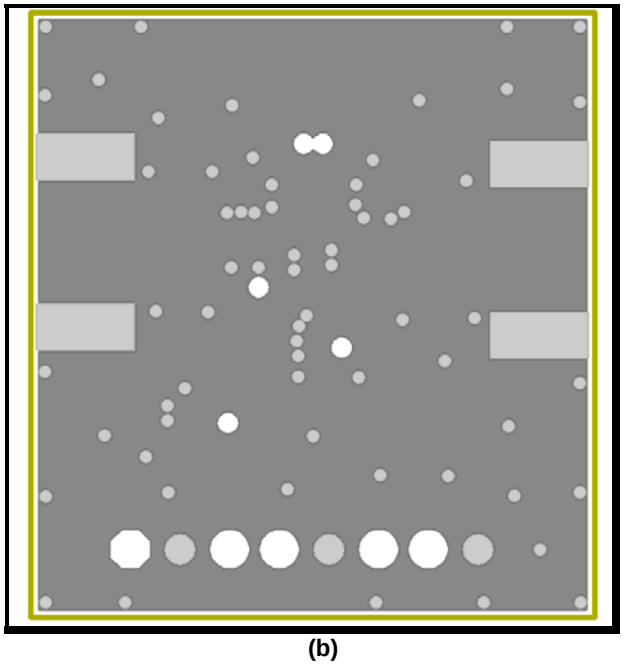
As a reference design, the evaluation board has been optimized from a component and layout perspective to maximize the performance of the PA2423L. Based on the schematic, the layout of the evaluation board is shown in Figure 5. This information is also available as gerber files, for ease of use.

Care should be taken to avoid routing the RF output track next to Vcc1 as this provides feedback around the output stage resulting in a loss in performance. The exposed pad at the bottom of the package is the ground connection for the IC. The ground vias should be placed as close as possible to this pad. All VCC lines should be well decoupled keeping the ground end of the decoupling capacitors as short as possible. The decoupling should avoid a ground return loop to the IC ground.

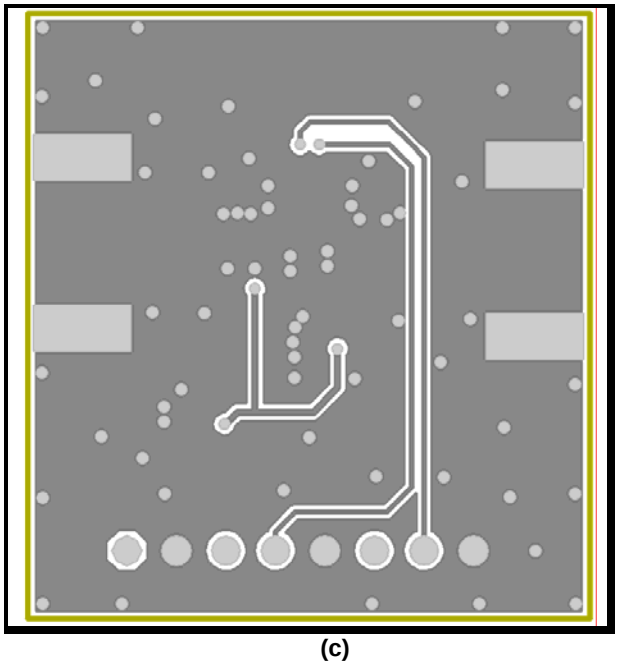
Evaluation Board Layout



(a)



(b)



(c)

Figure 5: PCB Board Layout (a) Top Layer, (b) Middle Layer (Ground Plane) and (c) Bottom Layer (V_{CC} Traces)

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Product Preview
The datasheet contains information from the product concept specification. SiGe Semiconductor, Inc. reserves the right to change information at any time without notification.

Preliminary Information
The datasheet contains information from the design target specification. SiGe Semiconductor, Inc. reserves the right to change information at any time without notification.

Production testing may not include testing of all parameters.