

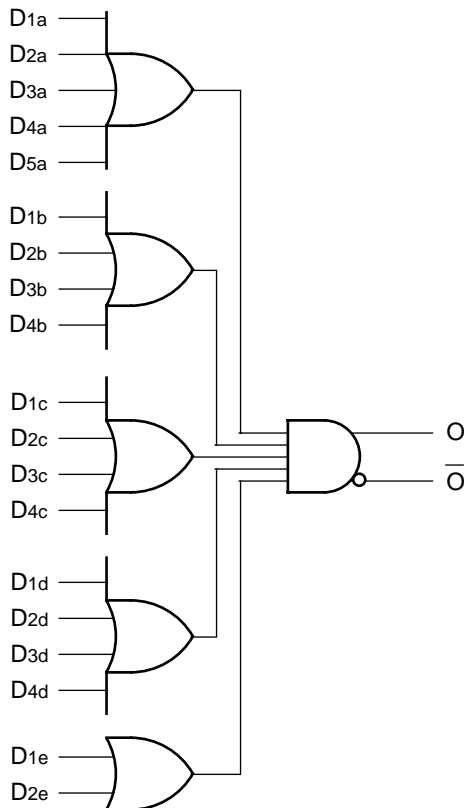
FEATURES

- Max. propagation delay of 800ps
- IEE min. of -55mA
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 70% faster than Fairchild
- 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACk and 28-pin PLCC packages

DESCRIPTION

The SY100S318 is an ultra-fast 5-wide 5, 4, 4, 4, 2 OR/AND gate with both true and complementary outputs, designed for use in high-performance ECL systems. The inputs on this device have 75KΩ pull-down resistors.

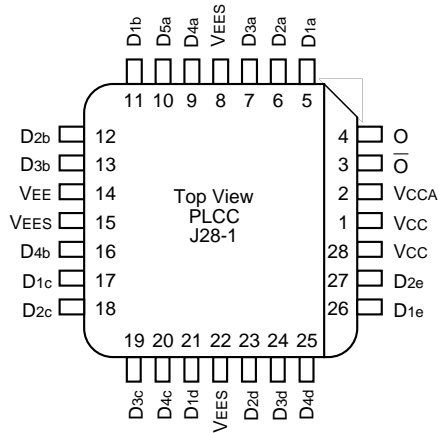
BLOCK DIAGRAM



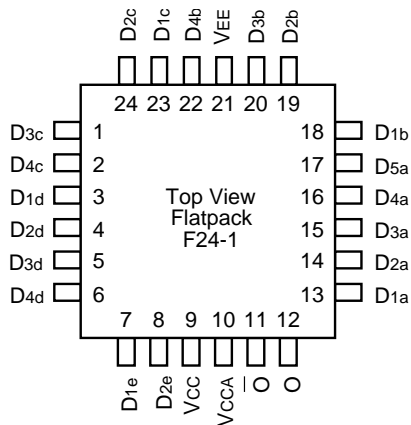
PIN NAMES

Pin	Function
D _{na} – D _{ne}	Data Inputs (n = 1...5)
O – \bar{O}	Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S318FC	F24-1	Commercial	SY100S318FC	Sn-Pb
SY100S318FCTR ⁽¹⁾	F24-1	Commercial	SY100S318FC	Sn-Pb
SY100S318JC	J28-1	Commercial	SY100S318JC	Sn-Pb
SY100S318JCTR ⁽¹⁾	J28-1	Commercial	SY100S318JC	Sn-Pb
SY100S318JZ ⁽²⁾	J28-1	Commercial	SY100S318JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S318JZTR ^(1, 2)	J28-1	Commercial	SY100S318JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

LOGIC EQUATION

$$O = (D1a + D2a + D3a + D4a + D5a) \\ (D1b + D2b + D3b + D4b) \\ (D1c + D2c + D3c + D4c) \\ (D1d + D2d + D3d + D4d) \\ (D1e + D2e)$$

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current, All Inputs	—	—	200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-55	-41	-25	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

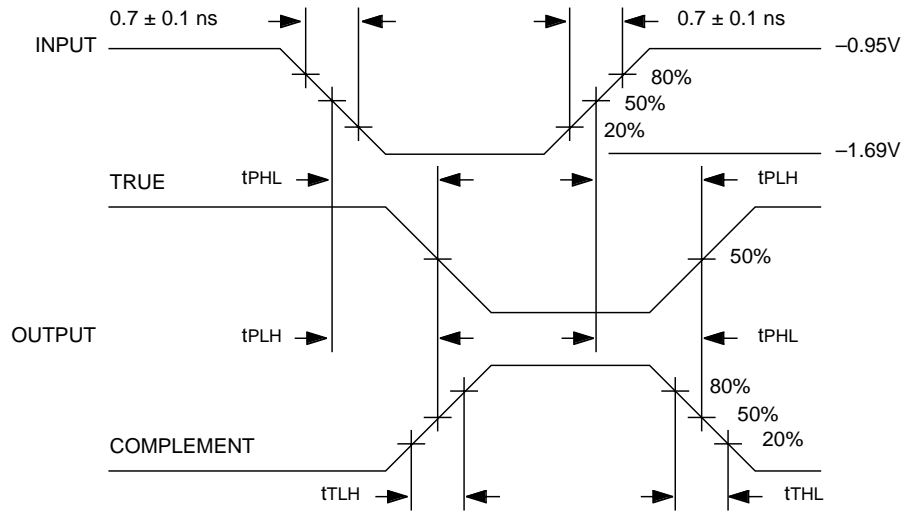
Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	300	900	300	900	300	900	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	200	900	200	900	200	900	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	300	800	300	800	300	800	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	200	900	200	900	200	900	ps	

TIMING DIAGRAM

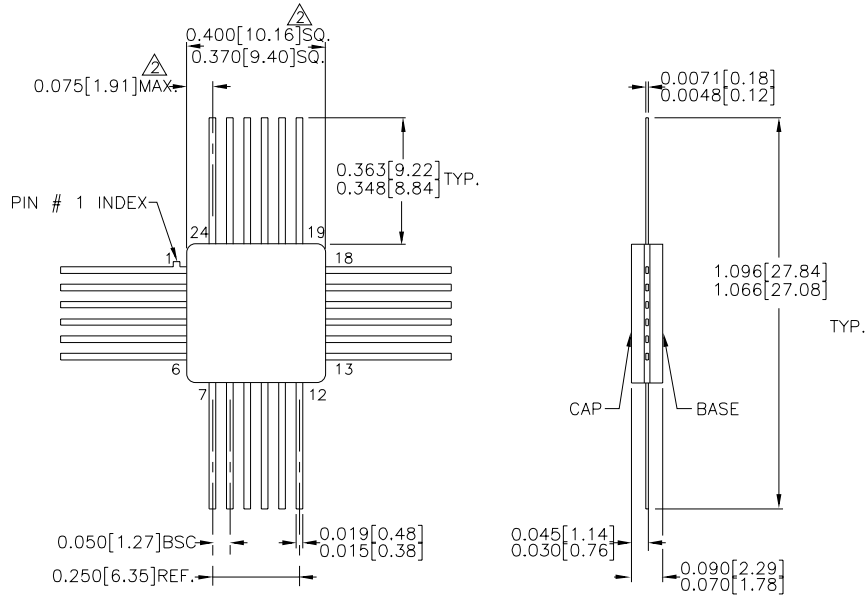


Propagation Delay and Transition Times

Note:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

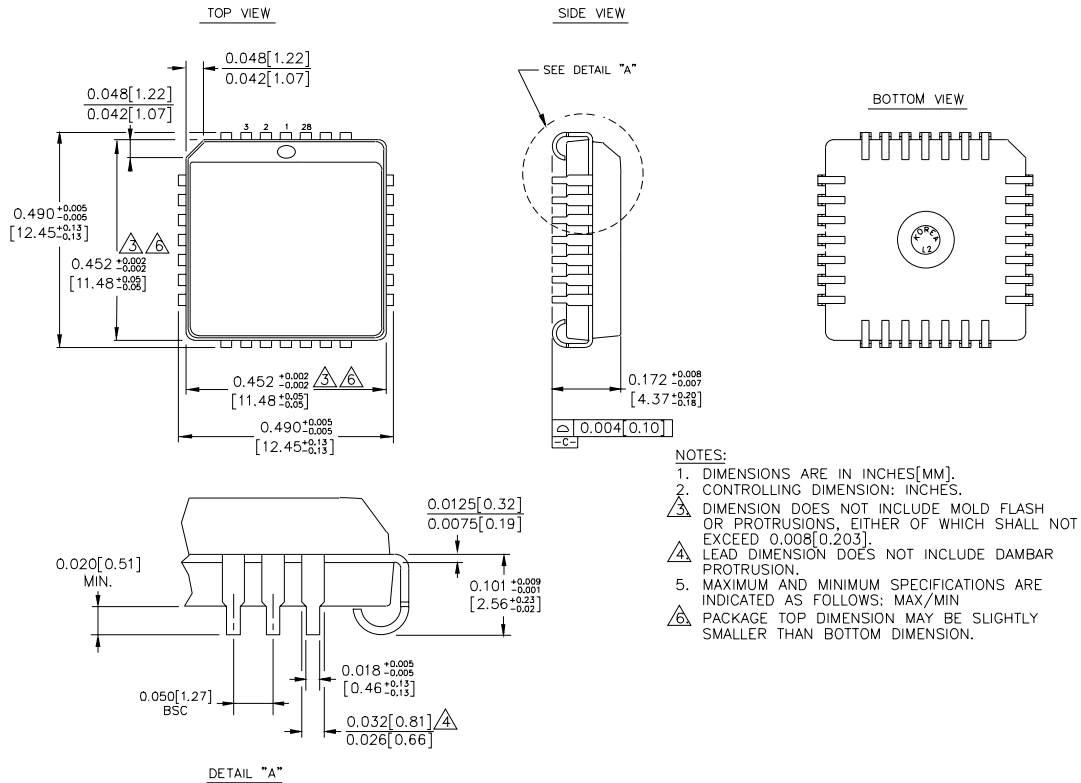
24-PIN CERPACK (F24-1)



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
 2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28-PIN PLCC (J28-1)



Rev. 03

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