



EMIF10-LCD02F3

10 line EMI filter and ESD protection for
LCD and cameras

Main product characteristics:

Where EMI filtering in ESD sensitive equipment is required :

- LCD for Mobile phones
- Computers and printers
- Communication systems
- MCU Boards

Description

The EMIF10-LCD02F3 is a 10 lines highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 flip chip packaging means the package size is equal to the die size.

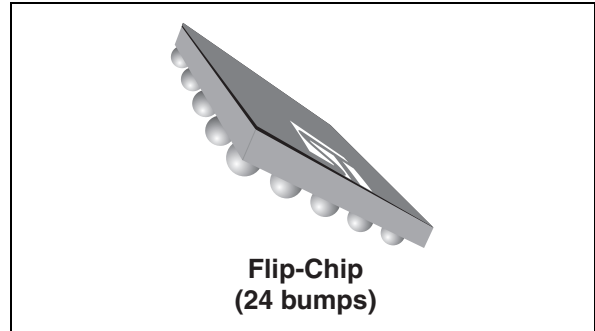
This filter includes ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up 15kV.

Benefits

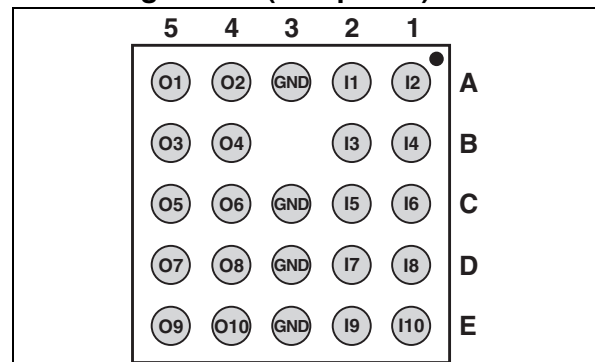
- Lead free package
- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- 400 μm pitch
- Compatible with high speed data rate
- Very low PCB space consuming: $< 4\text{mm}^2$
- Very thin package: 0.60 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging

Order Code

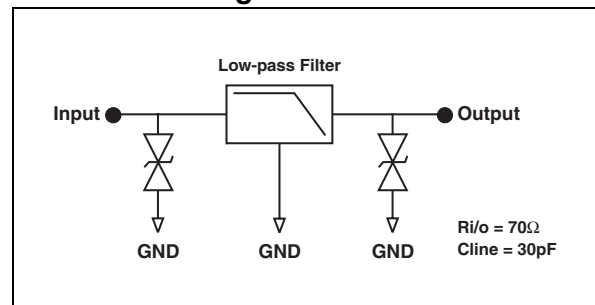
Part Number	Marking
EMIF10-LCD02F3	GY



Pin Configuration (bump side)



Basic Cell Configuration



Complies with the following standards:

IEC61000-4-2:

Level 4 15 kV (air discharge)
 8 kV (contact discharge)

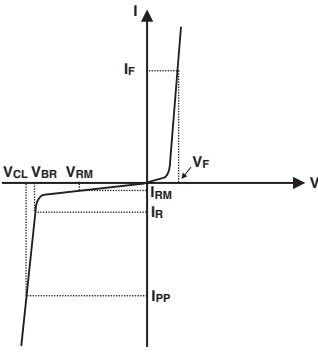
on inputs and outputs

MIL STD 883E - Method 3015-6 Class 3

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_j	Junction temperature	125	$^{\circ}\text{C}$
T_{op}	Operating temperature range	-40 to + 85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

1 Electrical characteristics ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter	
V_{BR}	Breakdown voltage	
I_{RM}	Leakage current @ V_{RM}	
V_{RM}	Stand-off voltage	
V_{CL}	Clamping voltage	
I_{PP}	Peak pulse current	
$R_{I/O}$	Series resistance between Input & Output	
C_{line}	Input capacitance per line	

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1 \text{ mA}$	6	8	10	V
I_{RM}	$V_{RM} = 3\text{V}$		50	200	nA
$R_{I/O}$	Tolerance $\pm 20\%$		70		Ω
C_{line}	$V_{line} = 0\text{V}$, $V_{OSE} = 30 \text{ mV}$, $F = 1 \text{ MHz}$			30	pF

Figure 1. S21(dB) all lines attenuation measurement and Aplanac simulation

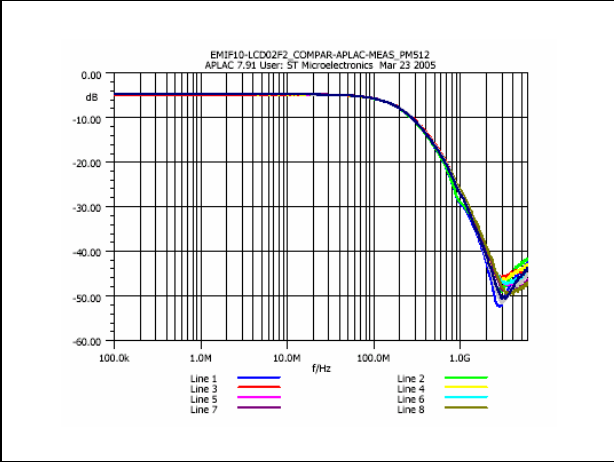


Figure 2. Analog cross talk measurements

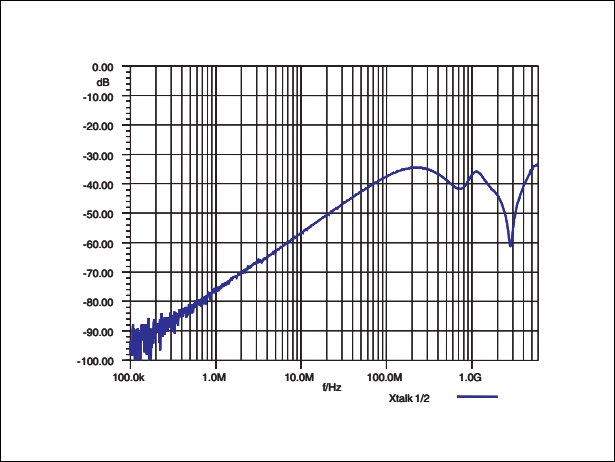


Figure 3. ESD response to IEC61000-4-2 (+15kV air discharge) on one input and on one output

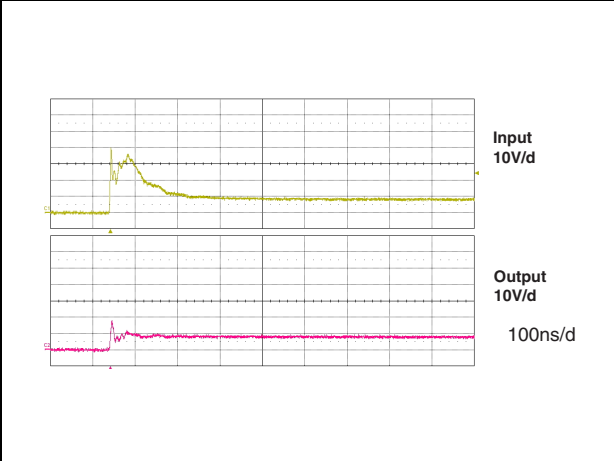


Figure 4. ESD response to IEC61000-4-2 (-15kV air discharge) on one input and on one output

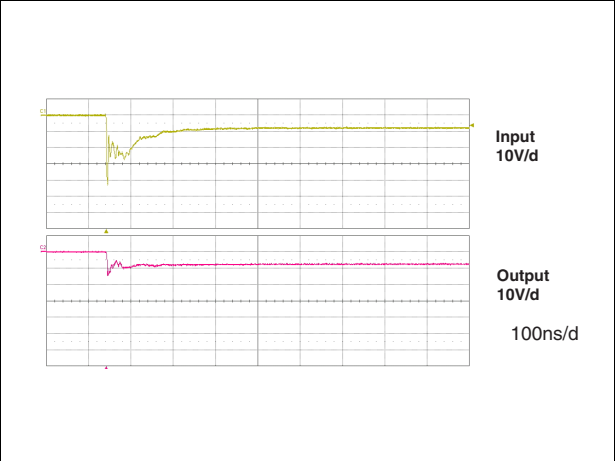
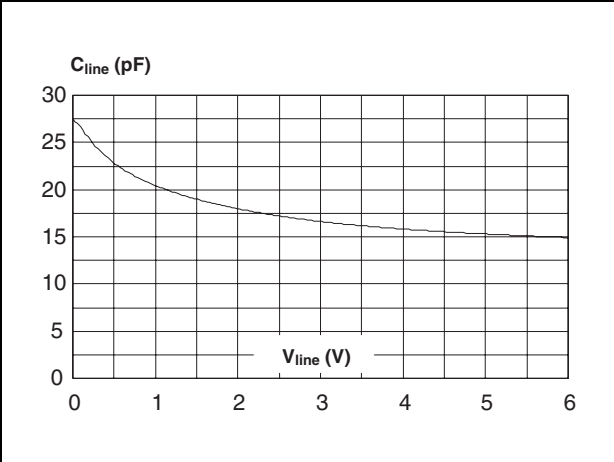


Figure 5. Line capacitance versus applied voltage



2 Aplac model

Figure 6. Device structure (one cell)

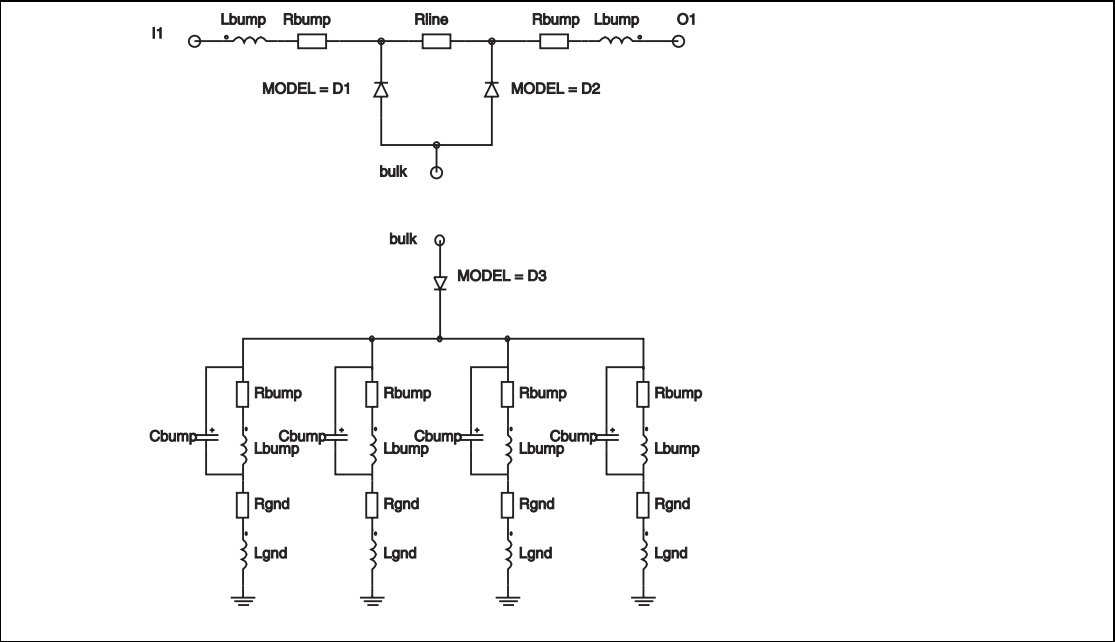
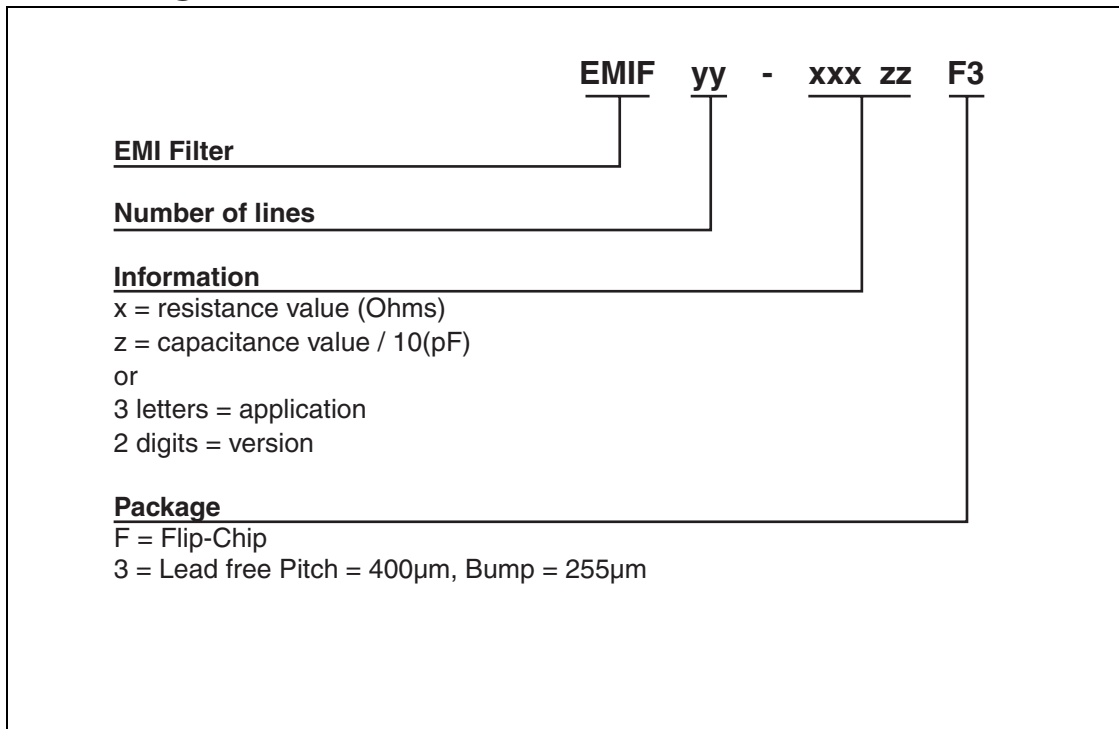


Figure 7. Aplac model variables

aplacvar Rline 70			
aplacvar C_d1 15p			
aplacvar C_d2 15p			
aplacvar C_d3 600p			
aplacvar Ls 950pH			
aplacvar Rs 150m			
aplacvar Lbump 50pH			
aplacvar Rbump 20m			
aplacvar Cbump 150f			
aplacvar Lgnd 50pH			
aplacvar Rgnd 100m			
aplacvar Rsub 10m			
Diode D1			
BV=7			
IBV=1m			
CJO=C_d1			
M=0.28			
RS=0.1			
VJ=0.6			
TT=100n			
Diode D2			
BV=7			
IBV=1m			
CJO=C_d2			
M=0.28			
RS=0.1			
VJ=0.6			
TT=100n			
Diode D3			
BV=7			
IBV=1m			
CJO=C_d3			
M=0.28			
RS=0.01			
VJ=0.6			
TT=100n			

3 Ordering information scheme



4 Package information

Figure 8. Mechanical data

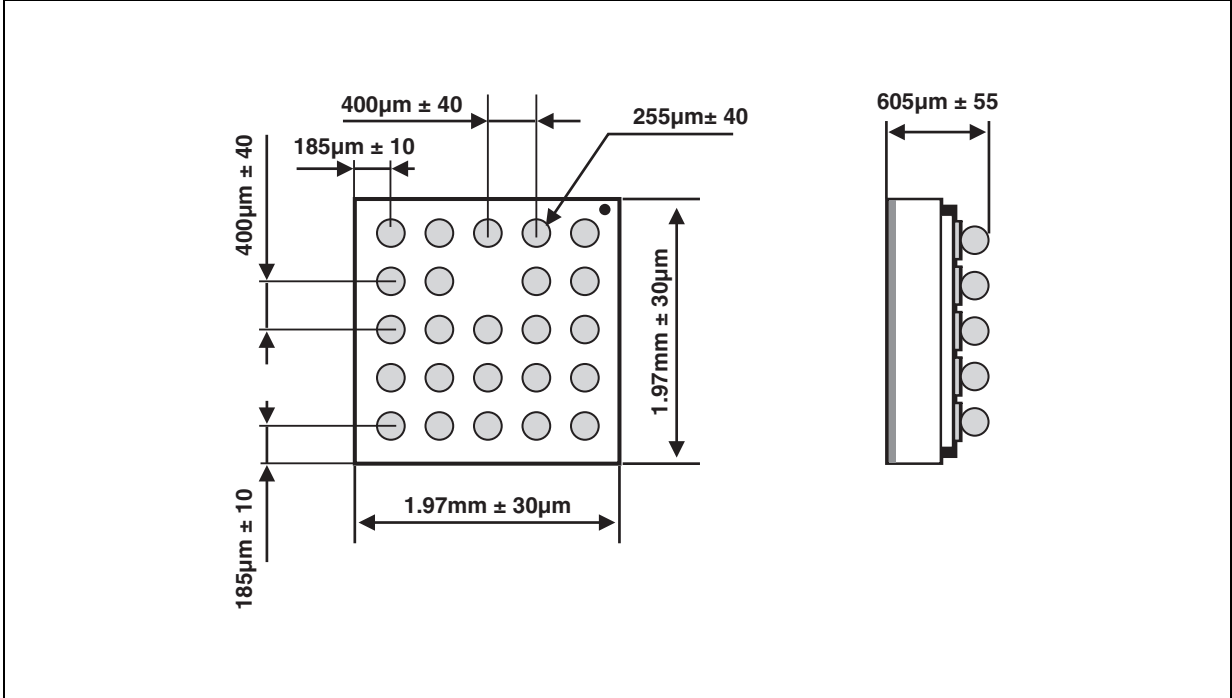


Figure 9. Foot print recommendations

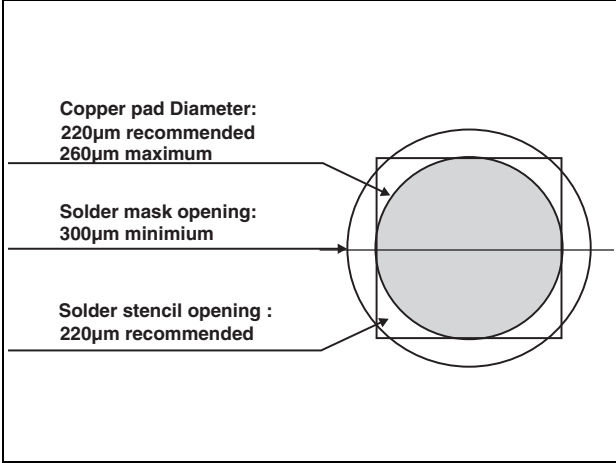
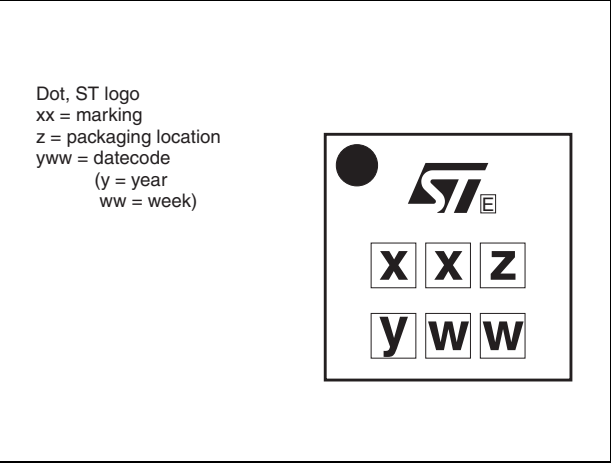
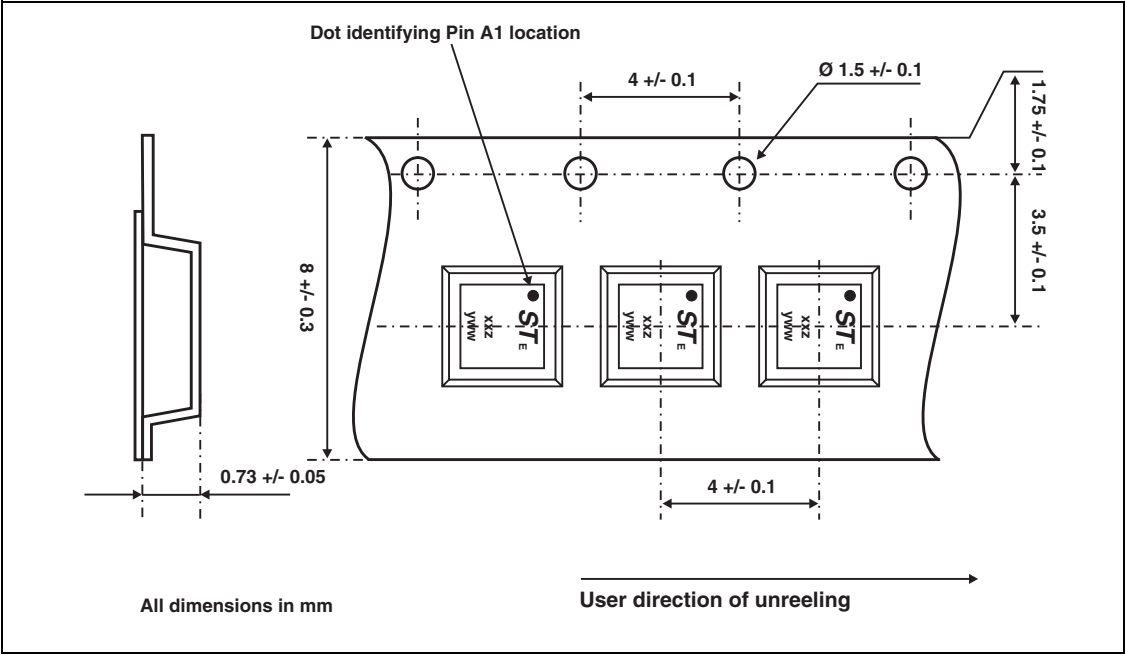


Figure 10. Marking



5 Flip-chip tape and reel specifications



6 Ordering information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-LCD02F3	GY	Flip-Chip	5.0 mg	5000	Tape & reel (7")

7 Revision history

Date	Revision	Changes
11-Jul-2005	1	Initial release.

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