

IRFI3205PbF

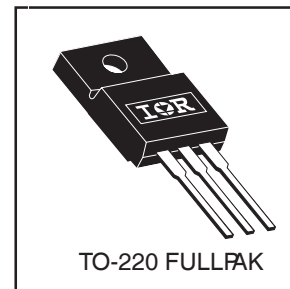
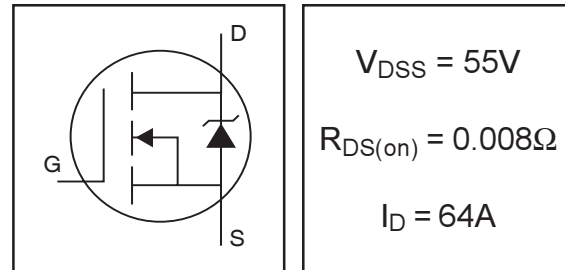
HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated
- Lead-Free

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	64	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	45	
I_{DM}	Pulsed Drain Current ①⑥	390	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	63	W
	Linear Derating Factor	0.42	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑥	480	mJ
I_{AR}	Avalanche Current①⑥	59	A
E_{AR}	Repetitive Avalanche Energy①	6.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

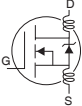
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	2.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient	---	65	°C/W

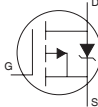
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International
 Rectifier

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	55	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.057	—	V/°C	Reference to 25°C, I _D = 1mA [Ⓞ]
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.008	Ω	V _{GS} = 10V, I _D = 34A ^④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	42	—	—	S	V _{DS} = 25V, I _D = 59A [Ⓞ]
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 55V, V _{GS} = 0V
		—	—	250		V _{DS} = 44V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	170	nC	I _D = 59A
Q _{gs}	Gate-to-Source Charge	—	—	32		V _{DS} = 44V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	74		V _{GS} = 10V, See Fig. 6 and 13 ^{④⑥}
t _{d(on)}	Turn-On Delay Time	—	14	—	ns	V _{DD} = 28V
t _r	Rise Time	—	100	—		I _D = 59A
t _{d(off)}	Turn-Off Delay Time	—	43	—		R _G = 2.5Ω
t _f	Fall Time	—	70	—		R _D = 0.39Ω, See Fig. 10 ^{④⑥}
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	4000	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1300	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	480	—		f = 1.0MHz, See Fig. 5 [Ⓞ]
C	Drain to Sink Capacitance	—	12	—		f = 1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	64	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ^{①⑥}	—	—	390		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 34A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	110	170	ns	T _J = 25°C, I _F = 59A
Q _{rr}	Reverse Recovery Charge	—	450	680	μC	di/dt = 100A/μs ^{④⑥}
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② V_{DD} = 25V, starting T_J = 25°C, L = 190μH
R_G = 25Ω, I_{AS} = 59A. (See Figure 12)
- ③ I_{SD} ≤ 59A, di/dt ≤ 290A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ t = 60s, f = 60Hz
- ⑥ Uses IRF3205 data and test conditions

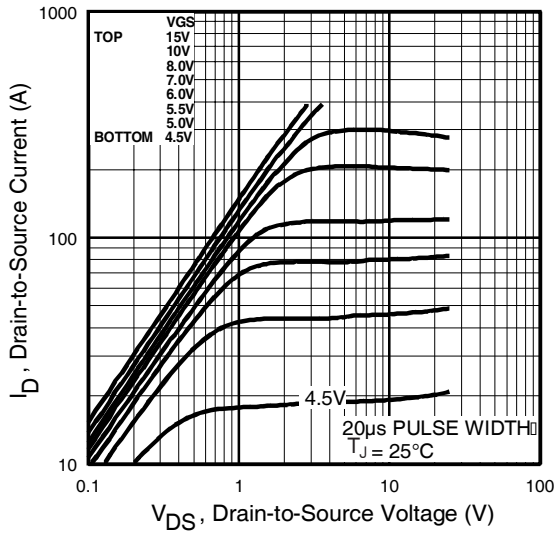


Fig 1. Typical Output Characteristics

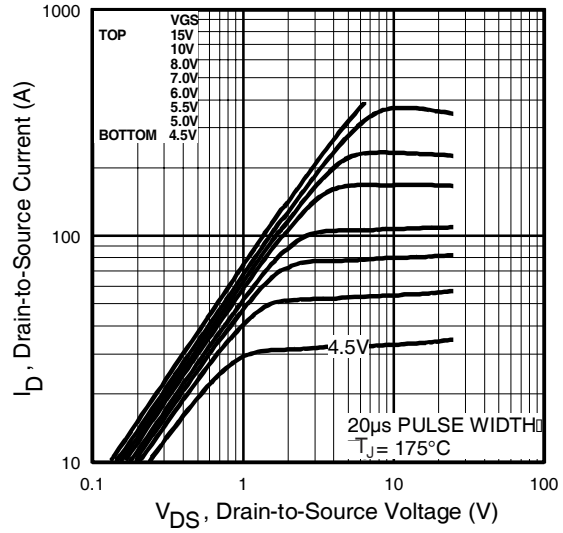


Fig 2. Typical Output Characteristics

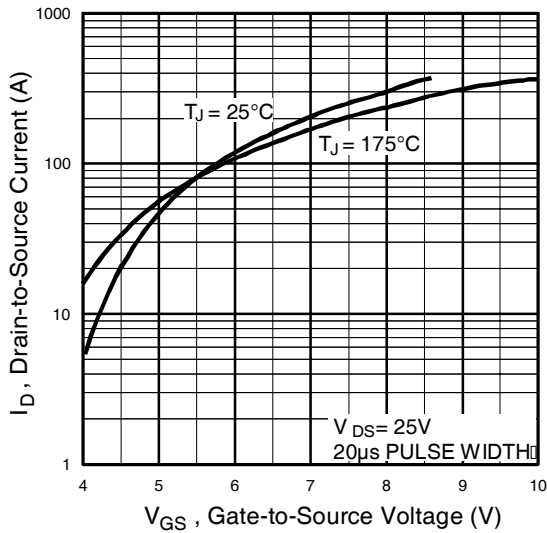


Fig 3. Typical Transfer Characteristics

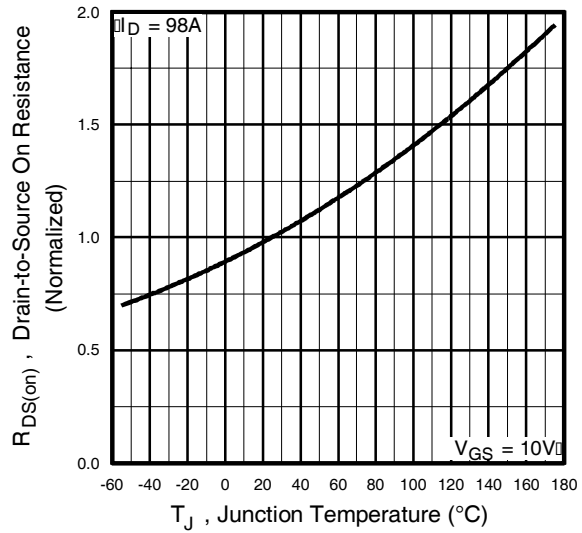


Fig 4. Normalized On-Resistance Vs. Temperature

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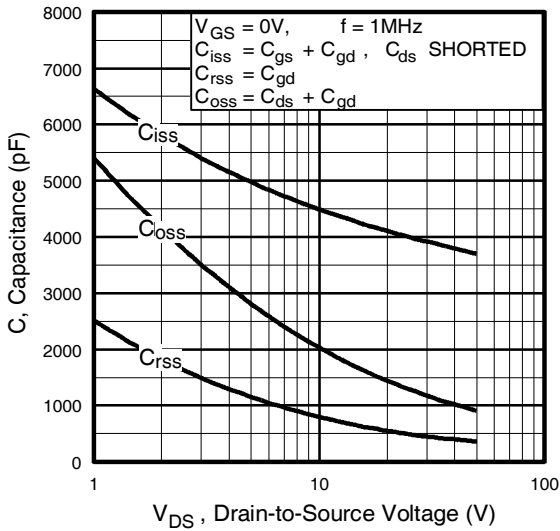


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

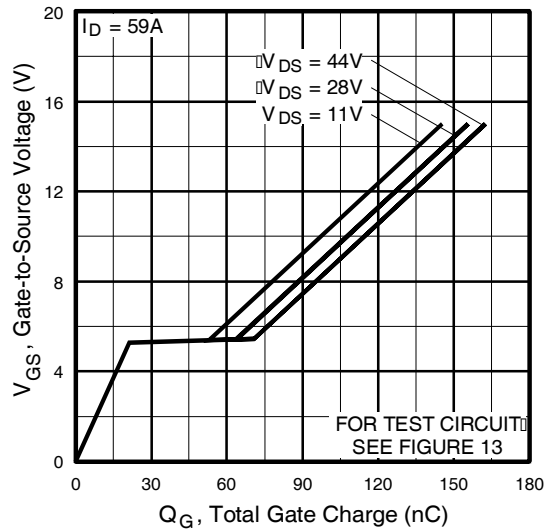


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

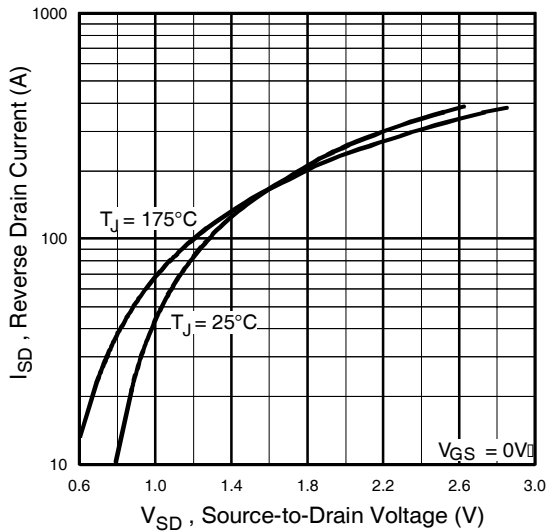


Fig 7. Typical Source-Drain Diode Forward Voltage

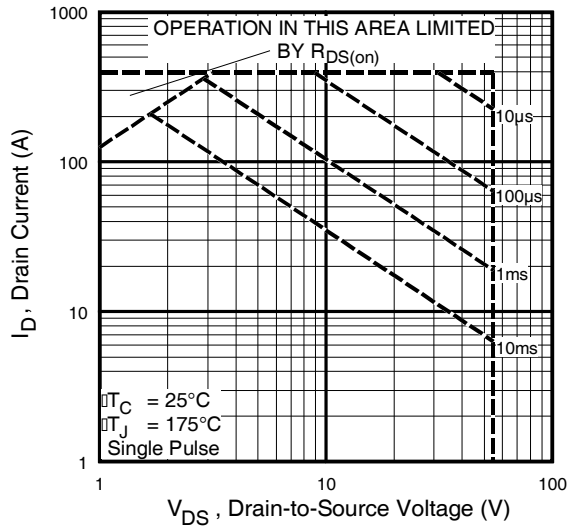


Fig 8. Maximum Safe Operating Area

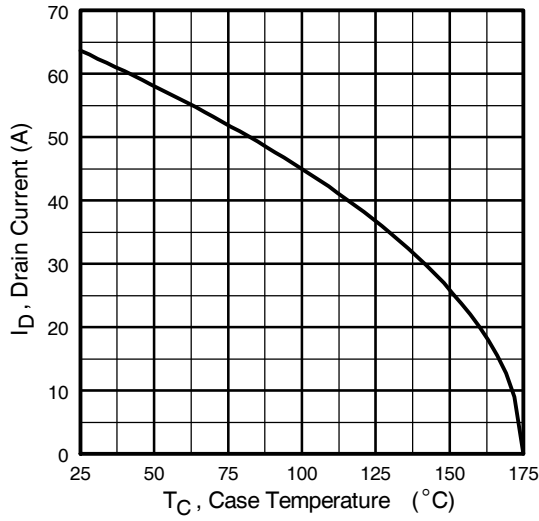


Fig 9. Maximum Drain Current Vs. Case Temperature

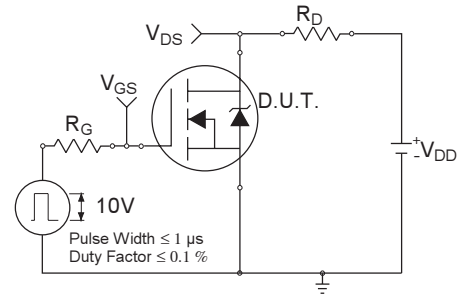


Fig 10a. Switching Time Test Circuit

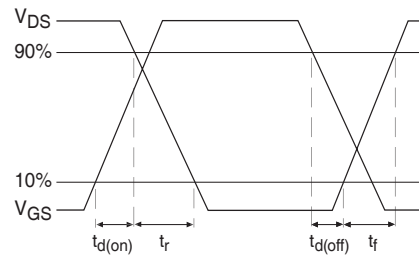


Fig 10b. Switching Time Waveforms

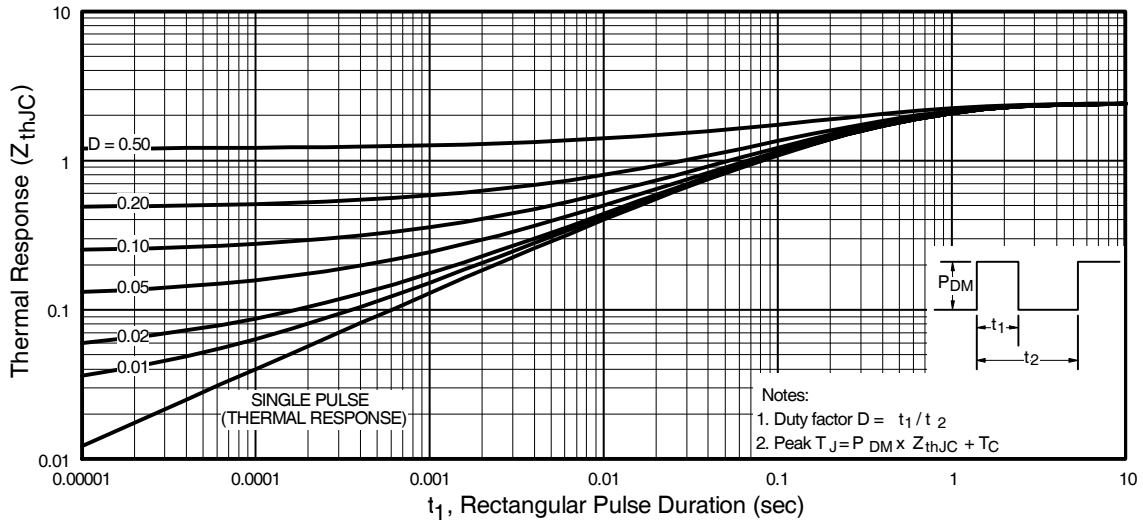


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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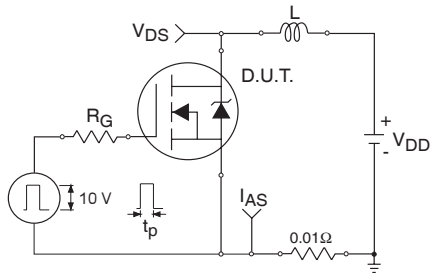


Fig 12a. Unclamped Inductive Test Circuit

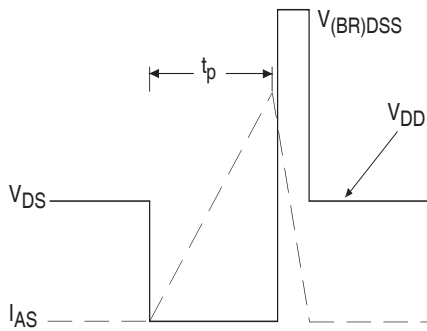


Fig 12b. Unclamped Inductive Waveforms

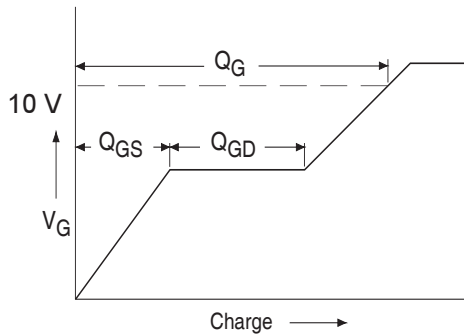


Fig 13a. Basic Gate Charge Waveform

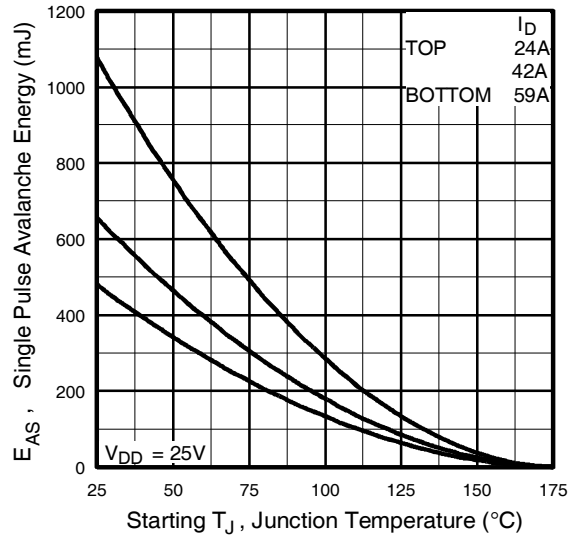


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

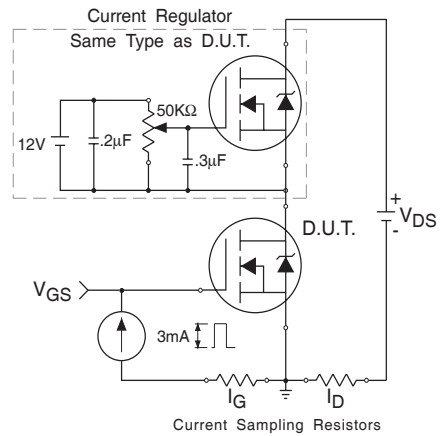
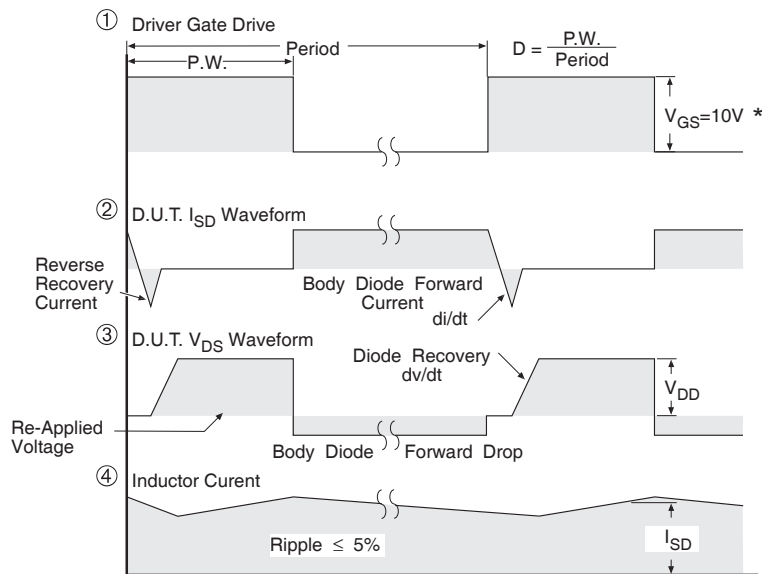
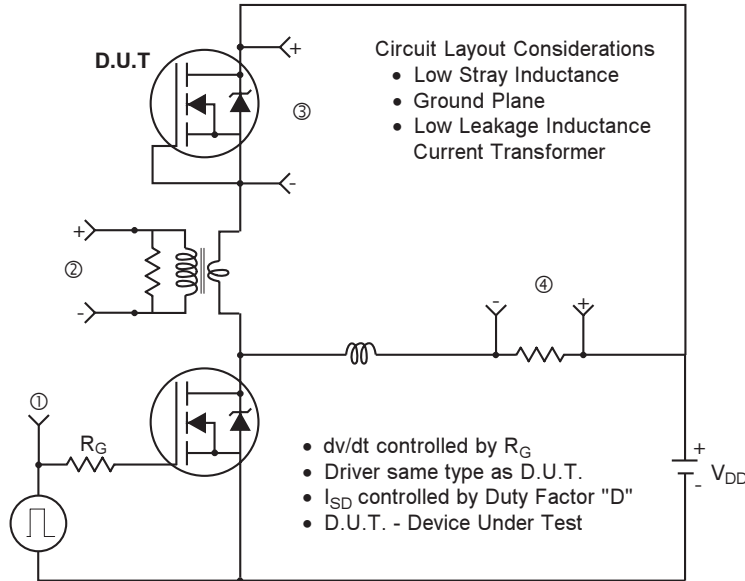


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

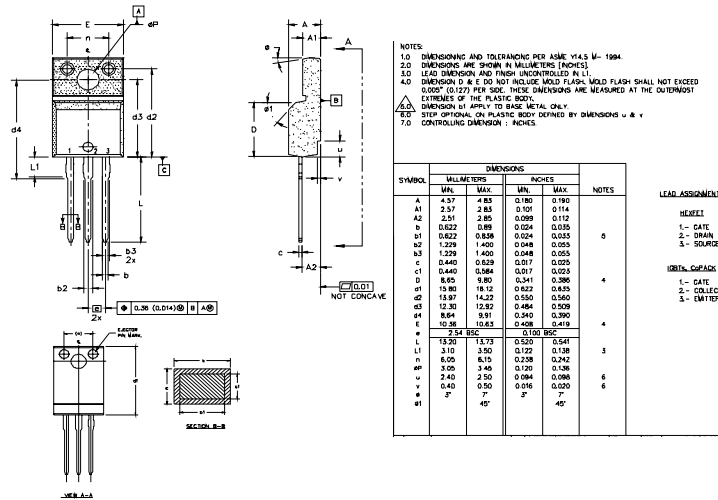
Fig 14. For N-Channel HEXFETS

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TO-220 Full-Pak Package Outline

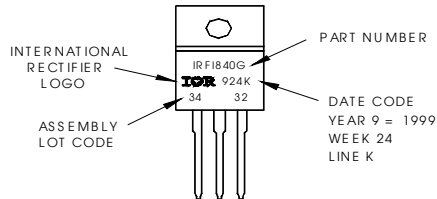
Dimensions are shown in millimeters (inches)



TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



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Note: For the most current drawings please refer to the IR website at:
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