Dual 3.3V PLL Clock Generator

MPC980

DUAL 3.3V PLL CLOCK GENERATOR

The MPC980 is a 3.3V dual PLL clock generator targeted for high end Pentium™ and PowerPC™ 603/604 personal computers. The MPC980 synthesizes processor as well as PCI clocks from a 14.31818MHz external crystal. In addition the device provides two buffered outputs of the 14.31818MHz crystal as well as a 40MHz SCSI clock, a 24MHz floppy clock and a 12MHz keyboard clock. One of the buffered 14.31818MHz outputs can be configured to provide a 16MHz output rather than the second copy of the 14.31818MHz output.

- Provides Processor and System Clocks for Pentium™ Designs
- Provides Processor and System Clocks for PowerPC™ 603/604 Designs
- Two Fully Integrated Phase–Locked Loops
- Cycle–to–Cycle Jitter of ±150ps
- Operates from 3.3V Supply
- 52–Lead LQFP Packaging

FA SUFFIX
52–LEAD LQFP PACKAGE
CASE 848D–03

The processor clock outputs of the MPC980 can be programmed to provide 50, 60 or 66MHz. Under all processor output frequencies the PCI clock outputs will be equal to one half the processor clock outputs. The PCI outputs will run synchronously to the processor clock outputs. There are a total of ten output clocks which can be split into a group of four and a group of six. Either group can be configured as processor or PCI clocks. Each of the outputs can drive two series terminated transmission lines allowing for the driving of up to twelve independent processor loads and eight PCI clock loads. A pin selectable option is available to delay the PCI clock outputs relative to the processor clocks. The amount of delay is a function of the processor clock frequency and varies from 2ns to 6ns.

The output jitter of the the PLL at 66MHz output is ±150ps peak–to–peak, cycle–to–cycle (the worst case deviation of the clock period is guaranteed to be less than ±150ps). The skews between one processor clock and any other processor clock (or one PCI clock to any other PCI clock) is 350ps. The worst case skew between the processor clocks and the PCI clocks is 500ps.

An output enable pin is provided to tristate all of the outputs for board level test. In addition a testing mode is provided to allow for the bypass of the PLL's for board level functional debug.

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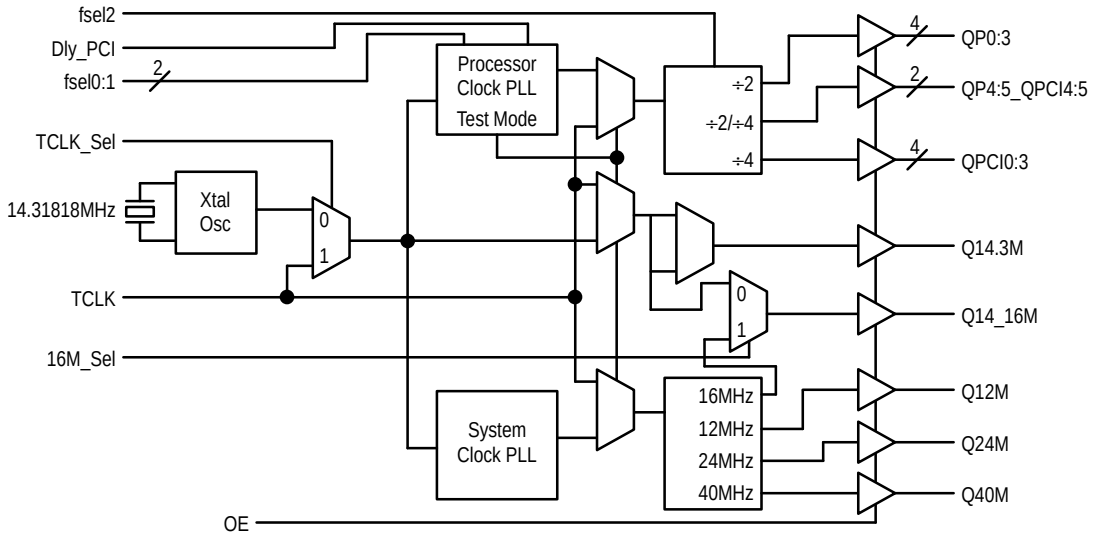


Figure 1. Logic Diagram

Table 1. Pin Descriptions

Pin	Label	Ω	Description
1	VCCA		Analog VCC for System PLL Use Filter (Note 1.)
2	TCLK_Sel	↓ 50K	Sel Ext'l TCLK or Internal Xtal Ref
3	TCLK	None	External LVCMOS Ref Signal
4	Xtal1	None	Xtal Pin 1
5	Xtal2	None	Xtal Pin 2
6	GND		System Ground Input
7	DLY_PCI	↓ 50K	Sets QP & QPI Relationship (See Function Table 2 on page 3.)
8	VCCI		VCC Pin for Internal Circuits
9	fsel0	↑ 50K	Least Bit for QP/QPI Output Funct (See Function Table 1 on page 3.)
10	fsel1	↓ 50K	Most Bit for QP/QPI Output Function (See Function Table 1 on page 3.)
11	fsel2	↓ 50K	Selection of QP/QPI Output Funct (See Function Table 4 on page 3.)
12	VCCA		Analog VCC Proc'ssr PLL Use Filter (Note 1.)
13	GNDA		System Ground Input
14	16M_SEL	↓ 50K	Selects 16MHz / 14MHz for Q14_16M Output
15	Q14_16M		Output for 16MHz / 14MHz Xtal Osc
16	GND0		System Ground Input
17	VCC0		VCC in for the CMOS Outputs
18	Q14M		CMOS Output for 14.3MHz Xtal Osc
19	GND0		System Ground Input
20	QP0		CMOS Output QP0
21	VCC0		VCC in for the CMOS Outputs
22	QP1		CMOS Output QP1
23	GND0		System Ground Input
24	QP2		CMOS Output QP2
25	VCC0		VCC in for the CMOS Outputs
26	GNDI		System Ground Input
27	VCCO		VCC in for the CMOS Outputs
28	QP3		CMOS Output QP3
29	GND0		System Ground Input
30	GND0		System Ground Input
31	QP4_PCI4		CMOS Output QP4_PCI4
32	VCC0		VCC in for the CMOS Outputs
33	QP5_PCI5		CMOS Output QP5_PCI5
34	GND0		System Ground Input
35	GND0		System Ground Input
36	QPCI3		CMOS Output QPCI3
37	VCCO		VCC in for the CMOS Outputs
38	QPCI2		CMOS Output QPCI2
39	GND0		System Ground Input
40	VCCI		VCC for Internal Core Logic
41	GND0		System Ground Input
42	QPCI1		CMOS Output QPCI1
43	VCC0		VCC in for the CMOS Outputs
44	QPCI0		CMOS Output QPCI0
45	GND0		System Ground Input
46	QM12		CMOS Output QM12
47	VCC0		VCC in for the CMOS Outputs
48	Q40M		CMOS Output Q40M
49	GND0		System Ground Input
50	Q24M		CMOS Output Q24M
51	OE	↑ 50K	Select Output State (See Function Table 1 on page 3.)
52	GND0		System Ground Input

1. The filter recommended for the analog power pins is found in Figure 3 in the Applications Information section on page 5.

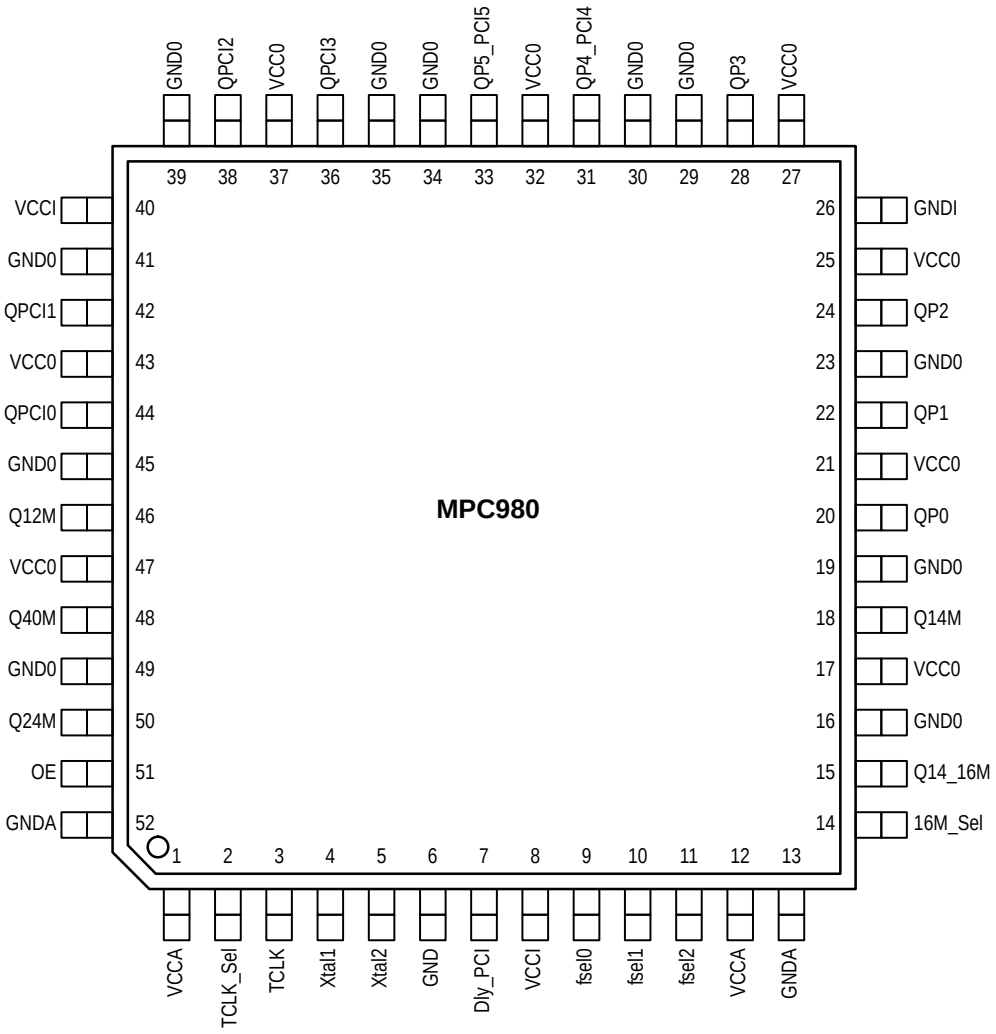


Figure 2. 52–Lead Pinout (Top View)

Function Table 1

OE	fsel0	fsel1	QP	QPCI	Q14M	Q16M	Q24M	Q12M	Q40M
0	X	X	High Impedance	High Impedance	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z
1	0	0	50MHz	25MHz	14.31818	16	24	12	40
1	0	1	60MHz	30MHz	14.31818	16	24	12	40
1	1	0	66MHz	33MHz	14.31818	16	24	12	40
1	1	1	TCLK/2	TCLK/4	TCLK	TCLK/6	TCLK/4	TCLK/8	TCLK/2

Function Table 2

Dly_PCI	QP/QPCI Relationship
0	Synchronous Processor & PCI Clocks
1	PCI Clocks Lag Processor Clocks

Function Table 3

TCLK_Sel	PLL Input Reference
0	Crystal Oscillator
1	TCLK

Function Table 4

fsel2	QP/QPCI Output Configuration
0	6 Processor and 4 PCI Clocks
1	4 Processor and 6 PCI Clocks

Function Table 5

16M_Sel	Q14_16M Output Configuration
0	14.31818MHz to Q14_16M Out
1	16MHz to Q14_16M Out

DC CHARACTERISTICS (T_A = 0° to 70°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{CC}	Power Supply Voltage	3.3–5%	3.3	3.3+5%	V	
V_{IL}	Input LOW Voltage			$0.3V_{CC}$	V	
V_{IH}	Input HIGH Voltage	$0.7V_{CC}$		V_{CC}	V	
V_{OH}	Output HIGH Voltage	V_{CC} –0.4			V	–20mA (Note 1.)
V_{OL}	Output LOW Voltage			0.4	V	+20mA (Note 1.)
C_{IN}	Input Capacitance			4.5	pF	
C_{PD}	Power Dissipation Capacitance		25		pF	
I_{CC}	Quiescent Supply Current			190	mA	
I_{CCA}	PLL Supply Current			20	mA	

1. Output can drive two series terminated 50Ω transmission lines or a single 50Ω line terminated 50Ω into $V_{CC}/2$.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
f_{Xtal}	Input Crystal Frequency			14.31818		MHz	
f_{max}	Maximum Output Frequency	QP QPCI			66 33	MHz	
t_{dc}	Output Duty Cycle		$t_{CYCLE}/2$ –1000	$t_{CYCLE}/2$ ±500	$t_{CYCLE}/2$ +1000	ps	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)	66/33MHz 60/30MHz 50/25MHz			±150 ±200 ±250	ps	
t_{skew}	Output–to–Output Skew	QP to QP QPCI to QPCI QP to QPCI			350 350 500	ps	Rising Edges Only; Dly_PCI = 0
t_{delay}	Time Delay	QP to QPCI	2	$\frac{1}{4f_{QP}}$	$\frac{1}{4f_{QP}} + 1$	ns	Dly_PCI = 1
t_r, t_f	Output Rise/Fall Time		0.05		0.8	ns	1.0 to 1.8V
t_{LOCK}	PLL Lock Time				10	ms	
t_{PZL}, t_{PZH}	Output Enable Time		3		10	ns	50Ω to $V_{CC}/2$
t_{PLZ}, t_{PHZ}	Output Disable Time		4		11	ns	50Ω to $V_{CC}/2$

APPLICATIONS INFORMATION

Using the On–Board Crystal Oscillator

The MPC980 features an on–board crystal Oscillator to allow for seed clock generation as well as final distribution. The on–board Oscillator is completely self contained so that the only external component required is the crystal. As the Oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC980 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The Oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel

resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC980 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an Oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementa–tions a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 2. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental at Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω Max
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MPC980 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC980 provides separate power supplies for the output buffers (VCCO) and the phase–locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC980.

Figure 3 illustrates a typical power supply filter scheme. The MPC980 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC980. From the data sheet the I_{VCCA} current (the current sourced per VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

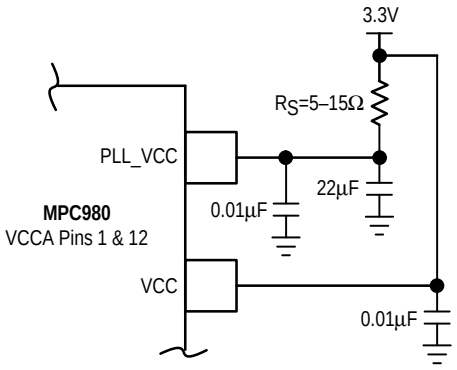


Figure 3. Power Supply Filter

Although the MPC980 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Component Reliability Analysis Information

All inputs and outputs of the MPC980 clock generator are LVCMOS and are not 5V tolerant. The quiescent current is 190mA maximum, so the maximum quiescent power is (190mA) × (3.465V max–V_{CC}) = 658.35mW. Total maximum power must include the dynamic power of the outputs.

$$\text{Dynamic Power/Output} = [\text{Logic Swing Out (volts)}] \times [V_{CC}\ \text{(volts)}] \times [\text{Freq (MHz)}] \times [C_I + C_p\ \text{(pF)}]$$

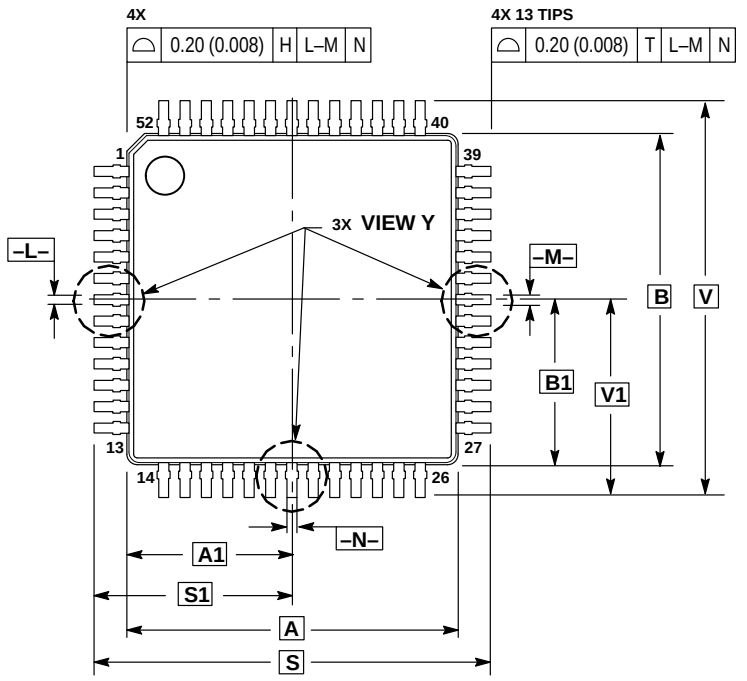
where

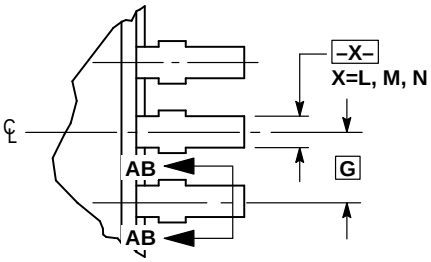
C_L = Load Capacitance
C_P = Output Power Dissipation Capacitance

The MPC980 is packaged in a 52–lead LQFP to optimize board space and power supply distribution. The LQFP package occupies a 12mm x 12mm space on the PCB. The 52–Pin LQFP package has a Θ_{JA} of 64 to 74°C/W in still air and a Θ_{JA} of 42 to 52°C/W in 500lfpm of moving air. The maximum chip temperature for the device is 140°C. The device component count is: NPN Bipolar devices 2,238; NMOS devices 1,313; PMOS devices 281.

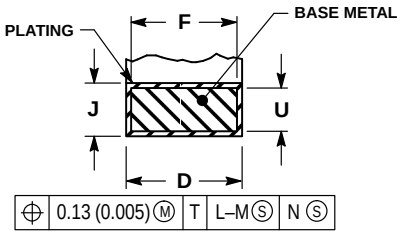
OUTLINE DIMENSIONS

FA SUFFIX
PLASTIC LQFP PACKAGE
CASE 848D-03
ISSUE D

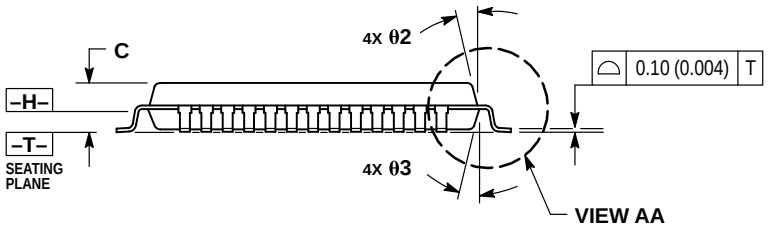


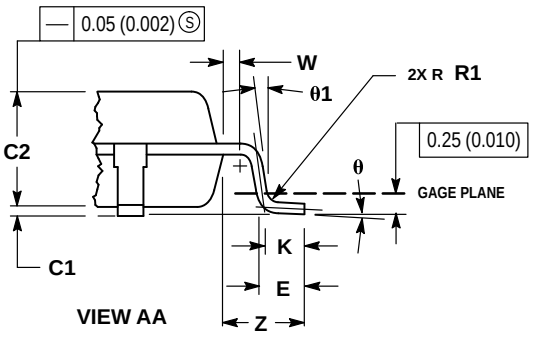


VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	12° REF		12° REF	

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