PMC-Sierra

OCTAL T1/E1/J1 Short Haul Line Interface Device

FEATURES

- Monolithic device which integrates 8 T1/J1 or E1 short haul line interface circuits.
- Software-selectable between T1/J1 and E1 operation on a per-device basis.
- Meets or exceeds T1/J1 and E1 short haul network access specifications including ANSI T1.102, T1.403, T1.408, AT&T TR 62411, ITU-T G.703, G.704 as well as ETSI 300-011, CTR-4, CTR-12 and CTR-13.
- Provides encoding and decoding of B8ZS, HDB3 and AMI line codes.
- Provides clock recovery and line performance monitoring.
- Provides transmit and receive jitter attenuation.
- Provides support for redundancy.
- Provides digitally programmable pulse templates.
- Provides a selectable, per channel independent de-jittered T1 or E1 recovered clock for system timing and redundancy.
- Provides PRBS generators and detectors on each tributary for error

BLOCK DIAGRAM

testing at DS1 and E1 rates as recommended in ITU-T 0.151.

- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- · Provides line and digital loopback modes.
- Supports programmable inband loopback codes.
- Uses line rate system clock.
- Provides an IEEE 1149.1 (JTAG) compliant test access port (TAP) and controller for boundary scan test.
- Provides a microprocessor-readable general purpose input pin and a microprocessor-writable general purpose output pin.

POWER

 Implemented in a low power 3.3 V tolerant 1.8/3.3 V CMOS technology.

PACKAGE

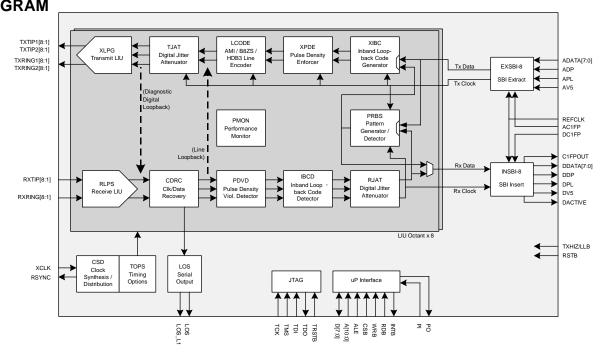
- Available in a high density 288-pin Tape-SBGA (23 mm x 23 mm) package.
- Provides a -40 °C to +85 °C industrial temperature operating range.

SYSTEM INTERFACE

 High-density SBI bus interface. Supports seamless interconnection of up to 11 OCTLIU-SHs to TE-32, TEMAP-84 and AAL1gator-32 using only 27 wires.

RECEIVE SECTION

- Supports T1 signal reception at 772 kHz and E1 signal reception at 1.024 MHz for distances with up to 6 dB of cable attenuation.
- Performs B8ZS or AMI decoding when processing a bipolar DS-1 signal, and HDB3 decoding when processing a bipolar E1 signal.
- Tolerates more than 0.3 UI peak-topeak, high frequency jitter as required by AT&T TR 62411 and Bellcore TR-TSY-000170.
- Detects line code violations, B8ZS/ HDB3 line code signatures, loss of signal, and successive zeroes conditions.
- Supports G.772 compliant nonintrusive protected monitoring points.



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TRANSMIT SECTION

- Generates DSX-1 short haul pulses with programmable pulse shape compatible with AT&T, ANSI and ITU requirements.
- Generates E1 pulses compliant to G.703 recommendations.
- Provides line outputs that are current limited and may be tristated for protection or redundant applications.
- Provides a digital phase locked loop for generation of a low jitter transmit

TYPICAL APPLICATIONS

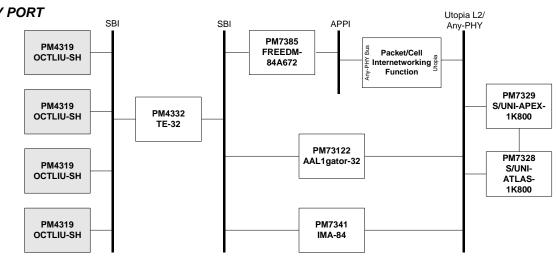
ANY SERVICE ANY PORT

clock complying with all jitter attenuation, jitter transfer, and residual jitter specifications of AT&T TR 62411 and ETSI TBR 12 and TBR 13.

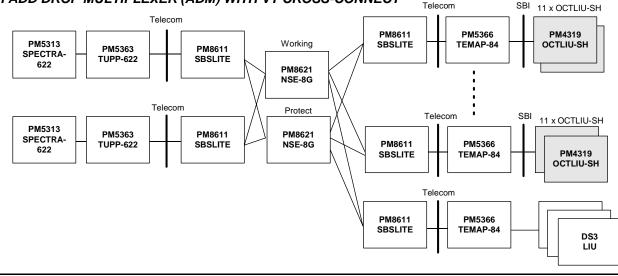
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmit path.
- Supports all ones transmission for alarm indication signal (AIS) generation.

APPLICATIONS

- Add/Drop Multiplexers.
- Edge Router Linecards.
- Multiservice ATM Switch Linecards.
- 3G Wireless Equipment.
- Digital Private Branch Exchanges (PBX).
- Digital Access Cross-Connect Systems (DACS).



SONET/SDH ADD DROP MULTIPLEXER (ADM) WITH VT CROSS-CONNECT



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