

2.5V Drive Pch+SBD MOS FET

US5U29

●Structure

Silicon P-channel MOS FET
Schottky Barrier DIODE

●Features

- 1) The US5U29 combines Pch MOS FET with a Schottky barrier diode in a TUMT5 package.
- 2) Low on-resistance with fast switching.
- 3) Low voltage drive (2.5V).
- 4) Built-in schottky barrier diode has low forward voltage.

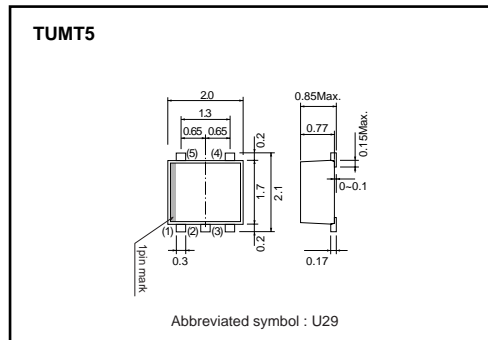
●Applications

Load switch, DC/DC conversion

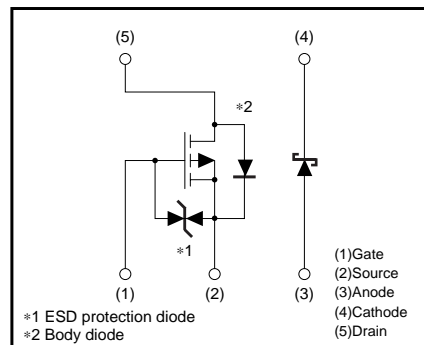
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US5U29		○

●External dimensions (Unit : mm)



●Equivalent circuit



Transistor

●Absolute maximum ratings (Ta=25°C)

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Parameter	Symbol	Limits	Unit	
Drain-source voltage	V _{DSS}	-20	V	
Gate-source voltage	V _{GSS}	±12	V	
Drain current	Continuous	I _D	±1	A
	Pulsed	I _{DP} *1	±4	A
Source current (Body diode)	Continuous	I _S	-0.4	A
	Pulsed	I _{SP} *1	-4	A
Channel temperature	T _{ch}	150	°C	
Power dissipation	P _D *3	0.7	W / ELEMENT	

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Repetitive peak reverse voltage	V _{RM}	25	V
Reverse voltage	V _R	20	V
Forward current	I _F	0.7	A
Forward current surge peak	I _{FSM} *2	3.0	A
Junction temperature	T _j	150	°C
Power dissipation	P _D *3	0.5	W / ELEMENT

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Total power dissipation	P _D *3	1.0	W / TOTAL
Range of Storage temperature	T _{stg}	-55 to +150	°C

*1 Pw≤10μs, Duty cycles≤1% *2 60Hz-1cyc. *3 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

<MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	-	-	±10	μA	V _{GS} =±12V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	-20	-	-	V	I _D =-1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	-	-	-1	μA	V _{DS} =-20V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	-0.7	-	-2.0	V	V _{DS} =-10V, I _D =-1mA
Static drain-source on-starte resistance	R _{DS(on)} *	-	280	390	mΩ	I _D =-1A, V _{GS} =-4.5V
		-	310	430	mΩ	I _D =-1A, V _{GS} =-4V
		-	570	800	mΩ	I _D =-0.5A, V _{GS} =-2.5V
Forward transfer admittance	Y _{fs} *	0.7	-	-	S	V _{DS} =-10V, I _D =-0.5A
Input capacitance	C _{iss}	-	150	-	pF	V _{DS} =-10V
Output capacitance	C _{oss}	-	20	-	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	-	20	-	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	-	9	-	ns	I _D =-0.5A V _{DD} =-15V
Rise time	t _r *	-	8	-	ns	V _{GS} =-4.5V
Turn-off delay time	t _{d(off)} *	-	25	-	ns	R _L =30Ω
Fall time	t _f *	-	10	-	ns	R _G =10Ω
Total gate charge	Q _g *	-	2.1	-	nC	V _{DD} =-15V V _{GS} =-4.5V
Gate-source charge	Q _{gs} *	-	0.5	-	nC	I _D =-1A
Gate-drain charge	Q _{gd} *	-	0.5	-	nC	R _L =15Ω R _G =10Ω

* Pulsed

<Body diode (source-drain)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD}	-	-	-1.2	V	I _S =-0.4A, V _{GS} =0V

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage drop	V _F	-	-	0.49	V	I _F =0.7A
Reverse current	I _R	-	-	200	μA	V _R =20V

Transistor

●Electrical characteristic curves

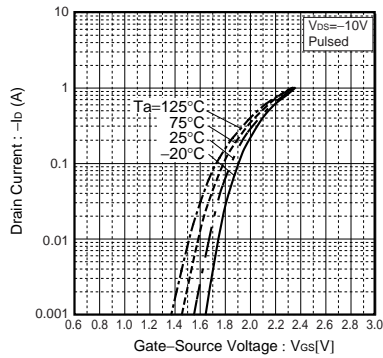


Fig.1 Typical Transfer Characteristics

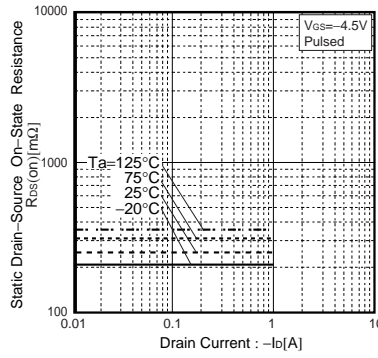


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current (I)

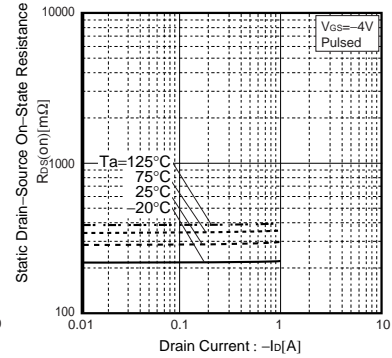


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (II)

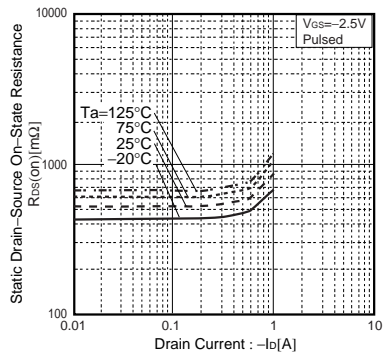


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (III)

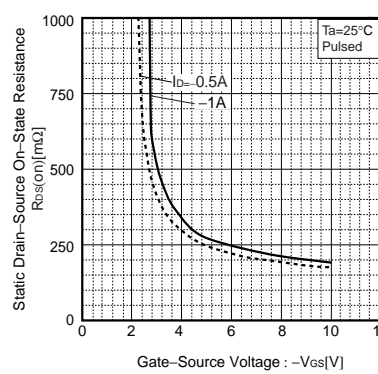


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

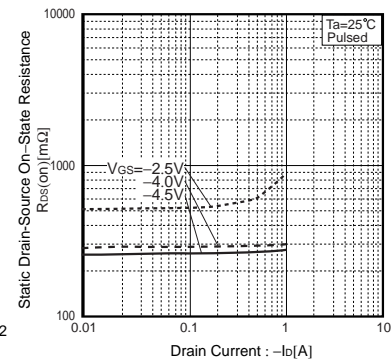


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

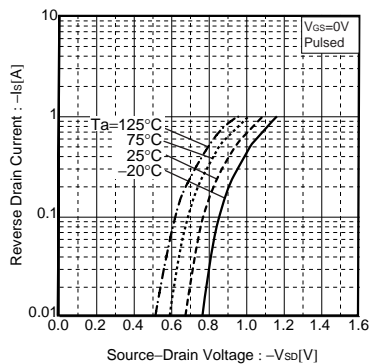


Fig.7 Reverse Drain Current vs. Source-Drain Current

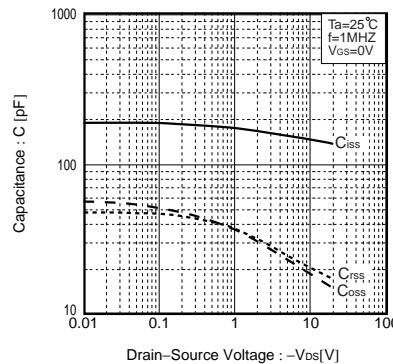


Fig.8 Typical Capacitance vs. Drain-Source Voltage

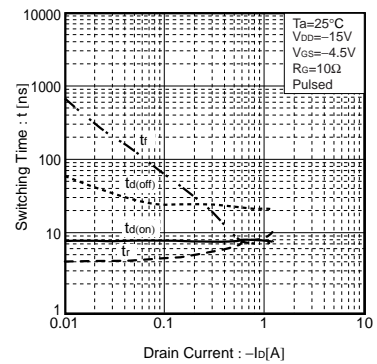
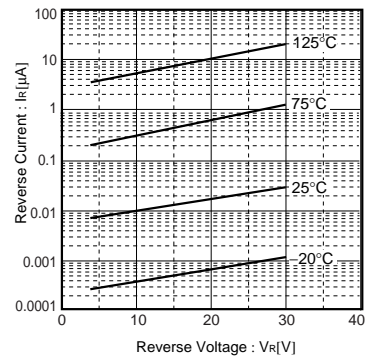
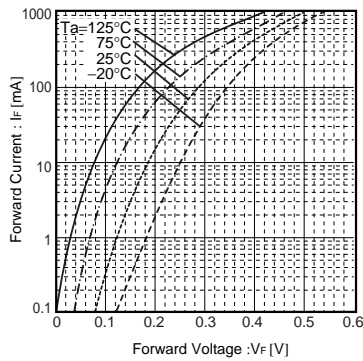
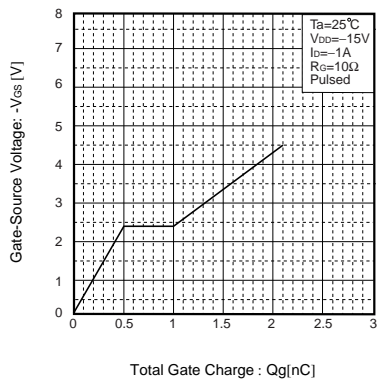


Fig.9 Switching Characteristics

Transistor



●Measurement circuits

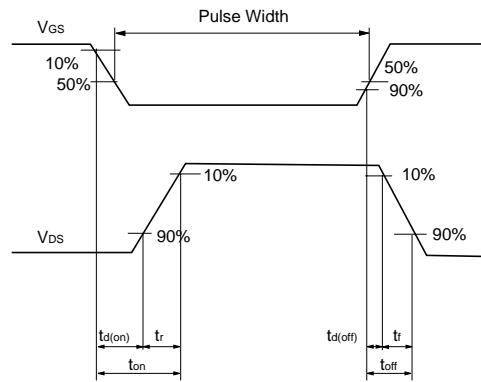
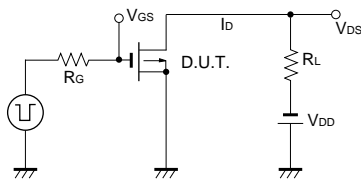


Fig.13 Switching Time Measurement Circuit

Fig.14 Switching Waveforms

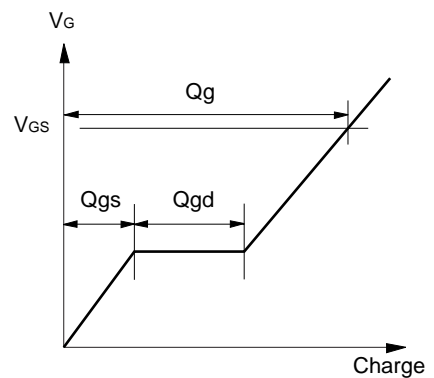
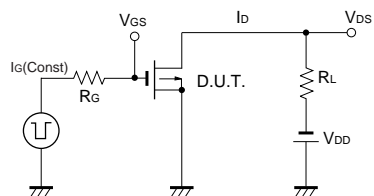


Fig.15 Gate Charge Measurement Circuit

Fig.16 Gate Charge Waveforms

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