YAMAHA

YGV629

VC1

Video Controller 1

■ Outline

YGV629 (Function name: VC1, hereinafter described as VC1) is a VDP (Video Display Processor), which has a pattern rendering function by the sprite method according to the attribute settings and a direct line rendering function. Since various effect functions are included sufficiently in the sprite function and line rendering function, more effective presentation can be realized.

Since VC1 can display the bit map image with free display resolution, NTSC to SVGA, on any screen size of monitor, OSD display control for various display units can be made.

And, VC1 includes a line buffer as a VRAM, so the system can be built with a little part. In addition, pattern memory can be connected directly, so that the amount of the control program can be reduced.

■ Features

□Display Function

- Pattern rendering by the sprite method according to the attribute settings, and OSD display by the direct line rendering according to the attribute settings.
- Two display layers: Sprite display layer and Line display layer, up to 341 can be displayed. However, for the line display layer, up to 1 layer can be displayed.
- Alpha-blending function between layers.

□Sprite Plane Function

- Sprite display of the field on the screen, up to 341
- Size 8×8 to 512×512 dots, independent selection (horizontal & vertical) possible. (in 8 dots)
- 2, 16, 32, 64, or 256 palette colors in 64k colors, 64k-color natural picture display by 16-bit RGB
- Reverse function in right to left or up and down
- Scaling function
- Alpha-blending function in pixels
- Anti-aliasing function at the outline part

YAMAHA CORPORATION

YGV629 CATALOG
CATALOG No.: LSI-4GV629A50
2006.05

□Line Rendering Function

- Line display of the field, up to 510
- Displayable color: 32768 colors (RGB555) or palette index (10-bit) designation
- Line width: 1 dot to 16 dots available (in dots)
- Anti-alias rendering available

□Display Resolution

- Display monitor interface timing generation for NTSC, PAL, QVGA, Wide QVGA, VGA, Wide VGA, and SVGA
- Example of the supported resolution: 320×240, 400×240, 640×480, 800×480, 800×600, etc.
- External Synchronizing Function

□External Memory

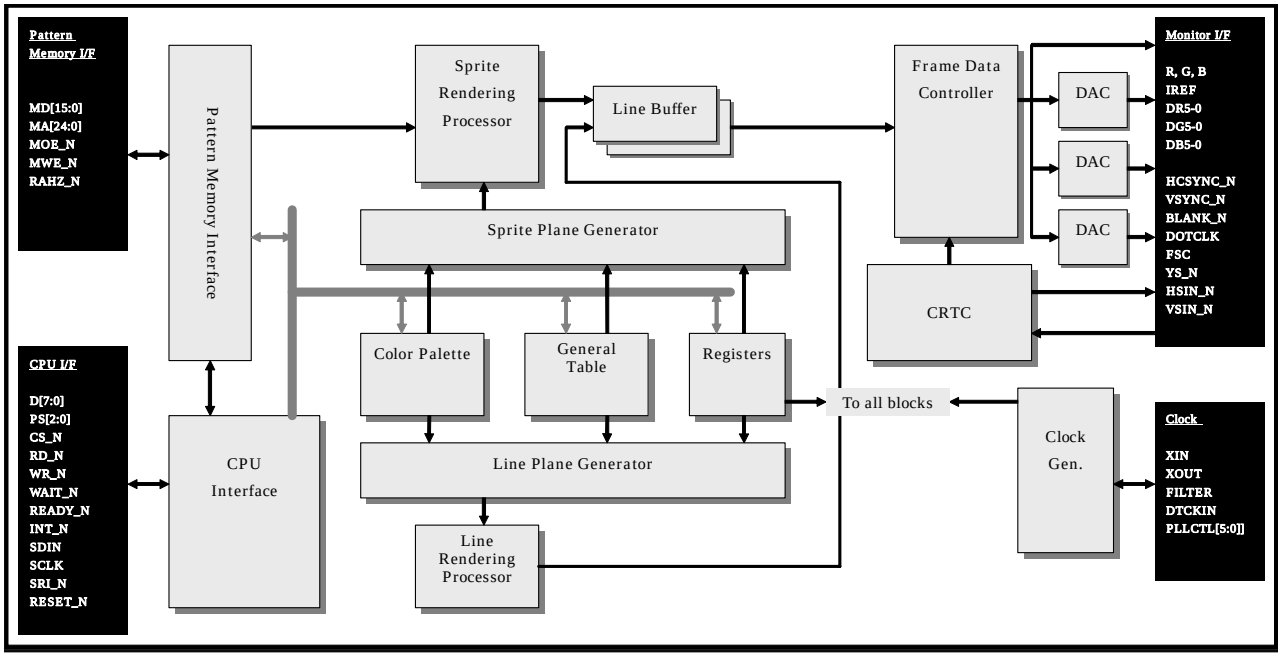
- Pattern memory up to 256M bits
- Mask ROM[i], SRAM, and NOR type flash-memory connection
- Access timing settings by the period of the system clock
- Bus width 8-bit/16-bit selection

□Others

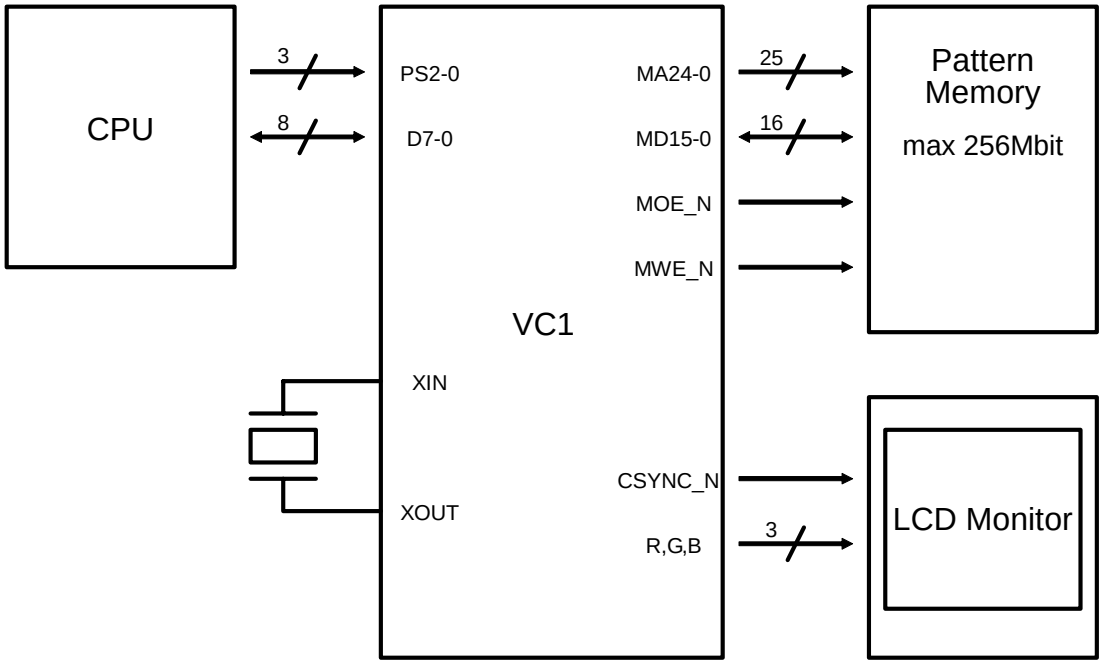
- 8-bit parallel interface and serial interface supported
- Indirect mapping to the built-in register and table through the access port.
- Analog RGB output and Digital RGB data output, with 6 bits DAC for each R,G, and B
- 144 pin plastic LQFP, pin lead plating is Pb-free. (YGV629-VZ)
- CMOS, 3.3V single power supply

[i] Timing-compatible ROM (OTPROM, EPROM, etc.) also can be connected.

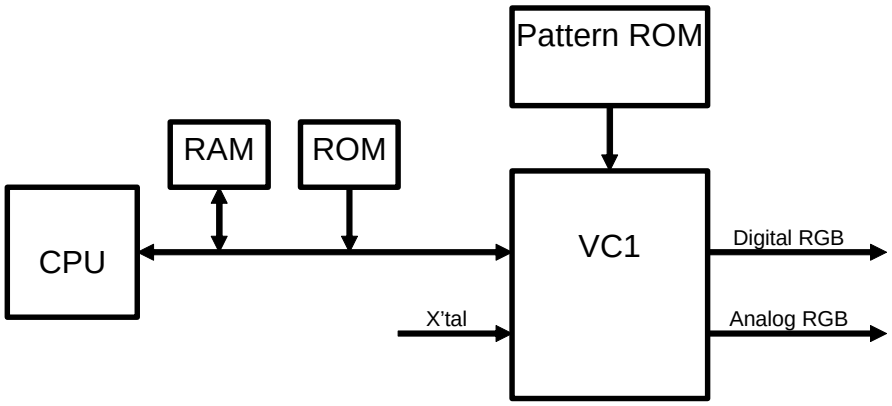
■ Block Diagram



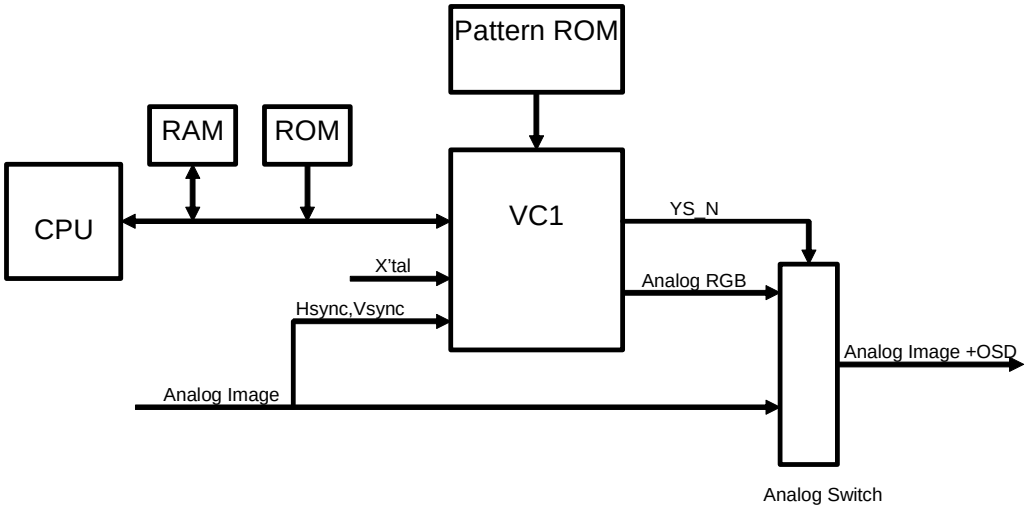
■ Examples of System Composition



・Stand-alone system



・OSD to the Analog Image



■ Pin Table

Pin Name	No.	I/O	Function	Level	5Tr	Drive
CPU Interface						
D7-0	8	I/O	CPU Data Bus	LVCMOS	○	4mA
PS2-0	3	I	CPU Port Selection	LVCMOS	○	
CS_N	1	I	Chip Select	LVCMOS	○	
RD_N	1	I	Read Pulse	LVCMOS	○	
WR_N	1	I	Write Pulse	LVCMOS	○	
WAIT_N	1	OT	CPU Bus Wait	LVCMOS	○	4mA
READY_N	1	OT	CPU Bus Ready	LVCMOS	○	4mA
INT_N	1	Od	Interrupt	LVCMOS	○	4mA
SER_N	1	I	CPU Interface Selection	LVCMOS	○	
SCS_N	1	I	Serial Interface Chip Select	LVCMOS	○	
SDIN	1	I	Serial Interface Data Input	LVCMOS	○	
SDOUT	1	OT	Serial Interface Data Output	LVCMOS	○	4mA
SCLK	1	I	Serial Clock Input	LVCMOS	○	
RESET_N	1	I	Reset	LVCMOS	○	
Pattern Memory Interface						
MD15-0	16	I/O	Pattern Memory Data Bus	LVCMOS	○	4mA
MA24-0	25	OT	Pattern Memory Address Bus	LVCMOS	○	4mA
MOE_N	1	OT	Pattern Memory Output Enable	LVCMOS	○	4mA
MWE_N	1	OT	Pattern Memory Write Pulse	LVCMOS	○	4mA
RAHZ_N	1	I	Pattern Memory High Impedance Switching	LVCMOS	○	
Monitor Interface						
R,G,B	3	O	Analog Image Output	Analog		
IREF	1	-	DAC Reference Power Supply	Analog		
DR5-0	6	O	Digital Image R Output	LVCMOS		4mA
DG5-0	6	O	Digital Image G Output	LVCMOS		4mA
DB5-0	6	O	Digital Image B Output	LVCMOS		4mA
VSYNC_N	1	O	Vertical Synchronizing Signal Output	LVCMOS		4mA
HCSYNC_N	1	O	Horizontal Synchronizing / Composite Synchronizing Signal Output	LVCMOS		4mA
VSIN_N	1	I	Vertical Synchronizing Input	LVCMOS	○	
HSIN_N	1	I	Horizontal Synchronizing Input	LVCMOS	○	
BLANK_N	1	O	Display Timing Output	LVCMOS		4mA
FSC	1	O	Sub-carrier Clock	LVCMOS		4mA
YS_N	1	O	YS Output	LVCMOS		4mA
DOTCLK	1	O	Dot Clock Output	LVCMOS		4mA
Clock						
XIN	1	I	Reference Clock Input			
XOUT	1	O	X'tal connection pin			
DTCKIN	1	I	Display system Clock Input	LVCMOS	○	
DTCKS_N	1	I	Display system Clock Selection	LVCMOS	○	
FILTER	1	-	PLL Filter Connection	Analog		
PLLCTL5-0	6	I	PLL Control	LVCMOS	○	

Od: open drain output, OT: 3-state output, 5Tr: 5V Tolerant, Drive: driving capability

Note) VC1 has no built-in pull up resistor. Pull up the pins externally as necessary.
The tolerant attribute is an attribute of the input buffer, output buffer that can become the high-impedance state, and bi-directional buffer, and indicates it can endure the 5V signal.

Pin Name	No.	I/O	Function	Level	5Tr	Drive
Power Supply						
VDD	11	-	Digital Power Supply			
VSS	14	-	Digital VSS			
PLLVDD	1	-	Power Supply for PLL			
PLLVSS	1	-	VSS for PLL			
AVDD	1	-	Power Supply for DAC			
AVSS	1	-	VSS for DAC			
LSI Test Pin						
XTEST2-0	3	I	Test Pin	LVCMOS	○	
Others						
NC	4	-	No connection Pin. Connect nothing.			

Od: open drain output, OT: 3-state output, 5Tr: 5V Tolerant, Drive: driving capability

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■ Pin Assignment Table

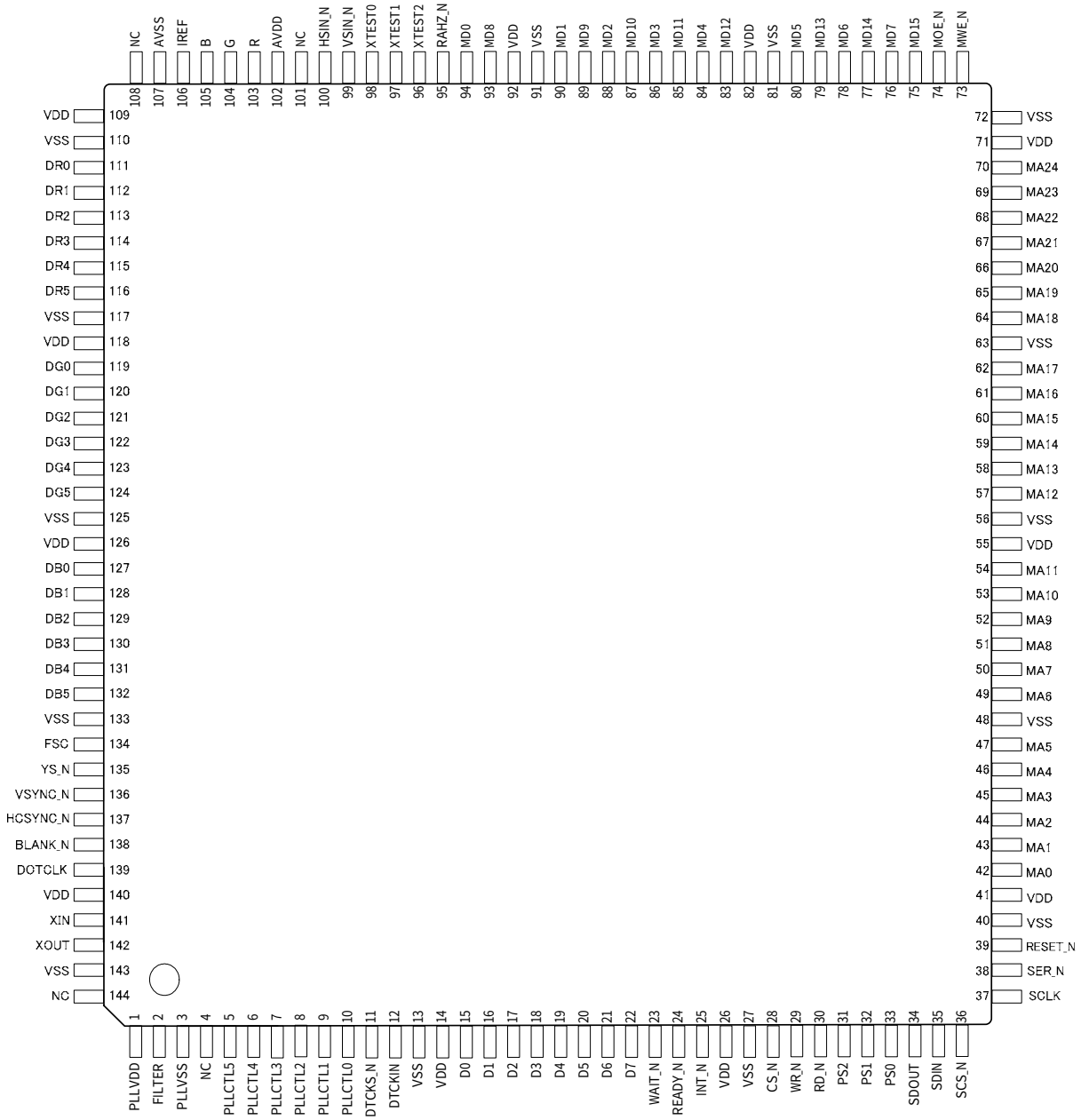
No	Pin Name	I/O	No	Pin Name	I/O	No	Pin Name	I/O	No	Pin Name	I/O
1	PLLVDD		37	SCLK	I	73	MWE_N	OT	109	VDD	
2	FILTER	A	38	SER_N	I	74	MOE_N	OT	110	VSS	
3	PLLVSS		39	RESET_N	I$	75	MD15	I/O	111	DR0	O
4	NC		40	VSS		76	MD7	I/O	112	DR1	O
5	PLLCTL5	I	41	VDD		77	MD14	I/O	113	DR2	O
6	PLLCTL4	I	42	MA0	OT	78	MD6	I/O	114	DR3	O
7	PLLCTL3	I	43	MA1	OT	79	MD13	I/O	115	DR4	O
8	PLLCTL2	I	44	MA2	OT	80	MD5	I/O	116	DR5	O
9	PLLCTL1	I	45	MA3	OT	81	VSS		117	VSS	
10	PLLCTL0	I	46	MA4	OT	82	VDD		118	VDD	
11	DTCKS_N	I	47	MA5	OT	83	MD12	I/O	119	DG0	O
12	DTCKIN	I	48	VSS		84	MD4	I/O	120	DG1	O
13	VSS		49	MA6	OT	85	MD11	I/O	121	DG2	O
14	VDD		50	MA7	OT	86	MD3	I/O	122	DG3	O
15	D0	I/O	51	MA8	OT	87	MD10	I/O	123	DG4	O
16	D1	I/O	52	MA9	OT	88	MD2	I/O	124	DG5	O
17	D2	I/O	53	MA10	OT	89	MD9	I/O	125	VSS	
18	D3	I/O	54	MA11	OT	90	MD1	I/O	126	VDD	
19	D4	I/O	55	VDD		91	VSS		127	DB0	O
20	D5	I/O	56	VSS		92	VDD		128	DB1	O
21	D6	I/O	57	MA12	OT	93	MD8	I/O	129	DB2	O
22	D7	I/O	58	MA13	OT	94	MD0	I/O	130	DB3	O
23	WAIT_N	OT	59	MA14	OT	95	RAHZ_N	I	131	DB4	O
24	READY_N	OT	60	MA15	OT	96	XTEST2	I	132	DB5	O
25	INT_N	Od	61	MA16	OT	97	XTEST1	I	133	VSS	
26	VDD		62	MA17	OT	98	XTEST0	I	134	FSC	O
27	VSS		63	VSS		99	VSIN_N	I	135	YS_N	O
28	CS_N	I	64	MA18	OT	100	HSIN_N	I	136	VSYNC_N	O
29	WR_N	I	65	MA19	OT	101	NC		137	HCSYNC_N	O
30	RD_N	I	66	MA20	OT	102	AVDD		138	BLANK_N	O
31	PS2	I	67	MA21	OT	103	R	AO	139	DOTCLK	O
32	PS1	I	68	MA22	OT	104	G	AO	140	VDD	
33	PS0	I	69	MA23	OT	105	B	AO	141	XIN	I
34	SDOUT	OT	70	MA24	OT	106	IREF	A	142	XOUT	O
35	SDIN	I	71	VDD		107	AVSS		143	VSS	
36	SCS_N	I	72	VSS		108	NC		144	NC	

NC indicates a no-connection pin. Make an open state electrically.

The meaning of each symbol for I/O is as follows.

I: Input, I$: Schmitt trigger input, I/O: Input Output, O: Output, Od: Open drain output,
OT: 3-state output, AO: Analog output, A: Analog pin

Pin Assignment



< Top View >

■ Pins Functions

A 3.3V supply voltage is supplied to VC1. Therefore, the interface between peripheral circuits uses LVCMOS (3.3V) for input/output. However, input pins, input/output pins, tri-state output pins, and an open-drain pin except XIN, XOUT, and the analog pins can interface with the 5V TTL level compatible device because they have 5V voltage tolerance.

Use the independent resistors for each pin, when pulling up or down the input pin and the input output pin externally. However, the common resistor can be used between the input pins when pulling up or down the input signal to the input pin. And, when pulling down the tolerant pin, connect to the ground level, through a resistor with 7kΩ or lower.

■ Power Supply

VC1 needs a 3.3V single power supply. There is a dedicated analog power supply pin for the built-in PLL and DAC as well as the digital power supply pin.

There is no restriction for the procedure to turn on the power supplies. Please power on or power off the power supplies so that the time difference from the first power supply to the last one becomes within 1 second.

- **VDD** (Power supply Pin No.14, 26, 41, 55, 71, 82, 92, 109, 118, 126, 140)
- **VSS** (Power supply Pin No.13, 27, 40, 48, 56, 63, 72, 81, 91, 110, 117, 125, 133, 143)
  Power supply pins for the internal digital circuit.
  Supply 3.3V to the VDD pin, and supply the ground level to the VSS pin.

- **PLLVDD** (Power supply Pin No.1)
- **PLLVSS** (Power supply Pin No.3)
  Analog Power supply pin for the built-in PLL
  Supply 3.3V to the PLLVDD pin, and supply the ground level to the PLLVSS pin.

- **AVDD** (Power supply Pin No.102)
- **AVSS** (Power supply Pin No.107)
  Analog Power supply pin for the built-in DAC

■ System Reset

VC1 must be reset in the power-on.

- **RESET_N** (Schmitt trigger input Pin No.39)
  Reset pin. Input the power-on-reset signal. The reset signal with the given time must be input after the power-on.
  The pin is low active. The pin uses a schmitt trigger type buffer.

■ Clock

Supply two clocks of the display system clock and the reference clock to the VC1 separately.
The display system clock becomes the original of a clock (dot clock) that is used for outputting monitor scan timing and display data.
The reference clock becomes the original of a clock (system clock) that is used for the process except the above.
The system clock and dot clock can be generated from the reference clock by supplying only the reference clock to VC1.

- **XIN** (Input Pin No.141)
- **XOUT** (Output Pin No.142)
  The reference clock input pin. Reference clock of the built-in PLL is input.

- **DTCKIN** (Input Pin No.12)
  Display system clock input pin. Input a clock which becomes the original of a clock (dot clock) that is used for outputting monitor scan timing and display data.

- **DTCKS_N** (Input Pin No.11)
  Display system clock selection pin. The signal selects a pin to input the display system clock.

- **PLLCTL5-0** (Input Pin No.5-10)
  PLL control pin. The pins set the multiplication number of the system clock that is generated in the built-in PLL to the reference clock.

- **FILTER** (Analog Pin No.2)
  A filter connection pin for the built-in PLL that is used for the system clock oscillation.

■ CPU Interface

Each CPU interface pin is used for the interface with the host CPU. The host CPU can control VC1 as an external I/O device.
The CPU interface of VC1 can select the 8-bit parallel interface or the serial interface. And, since its access timing is asynchronous interface, connection to various CPUs is possible.

- **D7-0** (Input Output Pin No.15-22)
  CPU data bus pin. The data bus pins are connected to the CPU external bus when 8-bit parallel interface is selected.

- **PS2-0** (Input Output Pin No.31-33)
  Selection pin for the internal port.
  Connect the pins to the CPU external address bus when 8-bit parallel interface is selected.

- **CS_N** (Input Pin No.28)
  Chip-select input pin. Input the chip-select signal to the pin when 8-bit parallel interface is selected.

- **RD_N** (Input Pin No.30)
  Read pulse input pin.
  The strobe signal for the data read (from CPU to VC1) is input when using in 8-bit parallel interface.

- **WR_N** (Input Pin No.29)
  Write pulse input pin. The strobe signal for the data write (from CPU to VC1) is input when using in 8-bit parallel interface.

- **WAIT_N** (3-state output Pin No.23)
  CPU bus wait pin. The bus wait request signal to CPU is output from this pin when using in 8-bit parallel interface.

- **READY_N** (3-state output Pin No.24)
  CPU bus ready pin. The bus ready signal to CPU is output from this pin when using in 8-bit parallel interface.

- **INT_N** (Open drain output Pin No.25)
  Interrupt signal output pin. An interrupt request signal to CPU is output.

- **SER_N** (Output Pin No.38)
  CPU interface selection pin.
  This pin selects which to select as a CPU interface from the serial interface or the 8-bit parallel interface.

- **SCS_N**(Input Pin No.36)
  Serial interface chip select input pin.
  The chip-select signal is input when using in the serial interface. SDIN pin and SCLK pin becomes valid

- **SDIN** (Input Pin No.35)
  Serial data input pin.
  Data is input when using in serial interface.

- **SDOUT** (3-state output Pin No.34)
  Serial data output pin. Data is output when using in serial interface.

- **SCLK** (Input Pin No.37)
  Serial clock input pin. A clock is input when using in serial interface.

■ Pattern Memory Interface

Each pin of the pattern memory interface is used as the interface with the pattern memory, which is connected to the VC1 local bus. Mask-ROM, NOR type flash-memory, and SRAM, etc. can be connected to the pattern memory.

- **MD15-0** (Input Output Pin No.75-80, 83-90, 93, 94)
  Pattern memory data bus pin. These pins are connected to the data bus of the pattern memory.

- **MA24 - 0**(3-state output Pin No.42-47, 49-54, 57-62, 64-70)
  Pattern memory address bus pin. These pins are connected to the address bus of the pattern memory.

- **MOE_N**(3-state output Pin No.74)
  Pattern memory output enable pin. The output enable signal to the pattern memory is output.

- **MWE_N**(3-state output Pin No.73)
  Pattern memory write pulse output pin. The write enable signal to the pattern memory is output.

- **RAHZ_N** (Input Pin No.95)
  Pattern memory high-impedance switching pin.

■ Monitor Interface

Each pin of the monitor interface is used for the interface with the external monitor. Since the display data is output in both of analog and digital signal, use them according to the specification of the external monitor interface.

- **R** (Analog output Pin No.103)
- **G** (Analog output Pin No.104)
- **B** (Analog output Pin No.105)
  Analog RGB output pin. Analog signals: R, G, and B of the display data is output.

- **IREF** (Analog Pin No.106)
  A pin for the DAC reference power supply. The reference current for DAC is input.

- **DR5-0** (Output PinNo.111-116)
- **DG5-0** (Output PinNo.119-124)
- **DB5-0** (Output PinNo.127-132)
  Digital RGB output pin.

- **VSYNC_N** (Output Pin No.136)
  Vertical synchronizing signal output pin. The vertical synchronizing signal is output in synchronization with DOTCLK.

- **HCSYNC_N** (Output Pin No.137)
  Horizontal synchronizing signal / composite synchronizing signal output pin.
  The horizontal synchronizing signal or composite synchronizing signal is output in synchronization with DOTCLK.

- **VSIN_N** (Input Pin No.99)
  Vertical synchronizing signal input pin.
  The external vertical sync for the reset of the internal vertical counter is input.

- **HSIN_N** (Input Pin No.100)
  Horizontal synchronizing signal input pin. The external horizontal sync for the reset of the internal horizontal counter is input.

- **BLANK_N** (Output Pin No.138)
  Display timing output pin. A signal that indicates the blank interval is output in synchronization with DOTCLK.

- **FSC** (Output Pin No.134)
  Sub-carrier clock output pin. The sub-carrier clock, which is used in the video encoder is output.

- **YS_N** (Output Pin No.135)
  YS signal output pin. YS signal is output in synchronization with DOTCLK when superimpose is performed.

- **DOTCLK** (Output Pin No.139)
  Dot clock output pin. Dot clock is output from this pin.

■ LSI Test

For each pin for the LSI test, be sure to observe the way of signal input, which is regulated here strictly.

- **XTEST2-0** (Input Pin No.96-98)
  Teat mode setting pin for VC1 test. Be sure to use under the following settings.

Pin Name	XTEST2	XTEST1	XTEST0
Input Level	H	H	H

■ Others

- **NC** (Pin No.4, 101, 108, 144)
  Non connection pin. Nothing is connected.

■ Electrical Characteristics

- Absolute Maximum Ratings

Items	Symbol	Rating	Unit	Note
Power Supply (VDD pin)	VDD	-0.5 to +4.6	V	1
DAC Power Supply (AVDD pin)	AVDD	-0.5 to +4.6	V	1
PLL Power Supply (PLLVDD pin)	PLLVDD	-0.5 to +4.6	V	1
Input Pin Voltage (5V tolerant pin)	V_I	-0.5 to +5.5	V	1
Input Pin Voltage (Except the above)	V_I	-0.5 to VDD+0.5(≤4.6 Max.)	V	1
Output Pin Voltage (Including the 5V tolerant pin and the input Output pin)	V_O	-0.5 to +5.5	V	1
Output Pin Voltage (Except the above)	V_O	-0.5 to VDD+0.5(≤4.6 Max.)	V	1
Input Pin Current	I_I	-20 to +20	mA	
Output Pin Current	I_O	-20 to +20	mA	
Storage Temperature	T_{stg}	-50 to +125	℃	

Note1) A value based on the reference of V_{SS}(GND)=0V.

- Recommended Operating Condition

Items	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply (VDD pin)	VDD	3.0	3.3	3.6	V	1
DAC Power Supply (AVDD pin)	AVDD	3.0	3.3	3.6	V	1
PLL Power Supply (PLLVDD pin)	PLLVDD	3.0	3.3	3.6	V	1
Operating Ambient Temperature	T_{OP}	-40		+85	℃	

Note1) A value based on the reference of V_{SS}(GND)=0V.

- Consumption Current

Items	Conditions	Symbol	Min.	Typ.	Max.	Unit	Note
Total Power Consumption	C_L=20pF V_{IL}=GND V_{IH}=VDD	P_D			1023	mW	1
Consumption Current							
VDD		I_{VDD}			200	mA	1
PLLVDD		I_{PVD}			4	mA	1
AVDD		I_{AVD}			80	mA	1

Note1) Consumption Current value and Power consumption value are the values under the recommended operating condition.

- DC Characteristics

Items	Symbol	Min.	Typ.	Max.	Unit	Note
Low level Input Voltage (XIN pin)	V_{IL}	-0.3		VDD×0.3	V	1
Low level Input Voltage (Except XIN pin)	V_{IL}	-0.3		0.8	V	1
High level Input Voltage (XIN pin)	V_{IH}	VDD×0.7		VDD+0.3	V	1
High level Input Voltage (Except XIN pin)	V_{IH}	2.0		5.5	V	1
Built-in DAC recommended operating condition						
Power Supply Voltage (AVDx pin)		3.0	3.3	3.6	V	1
Reference Current (IREF pin)			-9.38		mA	
Output Load (R,G,B)			37.5		Ω	

Note1) A value based on the reference of V_{SS}(GND)=0V

Items	Conditions	Symbol	Min.	Typ.	Max.	Unit	Note
Low level Output Voltage (Except XOUT pin)	I_{OL}=100μA	V_{OL}	0		0.2	V	1
	I_{OL}=2mA	V_{OL}	0		0.4	V	1
High level Output Voltage (Except XOUT pin)	I_{OH}= -100μA	V_{OH}	VDD-0.2		VDD	V	1
	I_{OH}= -2mA	V_{OH}	2.4		VDD	V	1
Input leak Current		I_{LI}	-10		+10	μA	
Output leak Current		I_{LO}	-25		+25	μA	

Note1) A value based on the reference of V_{SS}(GND)=0V

Items	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_I			10	pF
Output Pin Capacitance	C_O			10	pF
Input Output Pin Capacitance	C_{IO}			10	pF

- AC Characteristics

Measurement Conditions

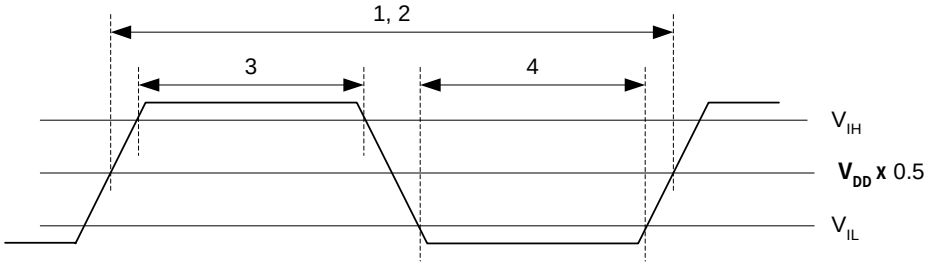
- Input Voltage: 0V to VDD
- Input Transition Time: 1ns (Transition time is regulated between VDD×0.2 and VDD×0.8)
- Measurement Reference Voltage: Input V_{IL} or V_{IH}
  Output VDD×0.5 [V]
- Output Load Capacitance: 20pF

- Clock Input

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	XIN Input Clock Frequency	f_{XIN}	6		40	MHz	
	XIN Clock Cycle Time	t_{XIN}	25		166	ns	
2	DTCKIN Input Clock Frequency	f_{DTCKIN}			40	MHz	
	DTCKIN Clock Cycle Time	t_{DTCKIN}	25			ns	
3	XIN, DTCKIN Clock High Level Pulse Width	t_{whCLK}	7.5			ns	
4	XIN, DTCKIN Clock Low Level Pulse Width	t_{wlCLK}	7.5			ns	
5	SYCLK(PLL Out) Clock Cycle Time	t_{SYCLK}	12.5		16.6	ns	1
6	DCLK Clock Cycle Time	t_{DCLK}	25			ns	2

Note1) SYCLK is an internal clock generated in the PLL. t_{SYCLK} is a regulation to the value that is found by the following formula, to the input clock to XIN pin.
$t_{SYCLK} = t_{XIN} \times k \div n \quad (1 \le k \le 4, \quad 1 \le n \le 16)$

Note2) DCLK is a Dot Clock that is used inside.



- Reset Input

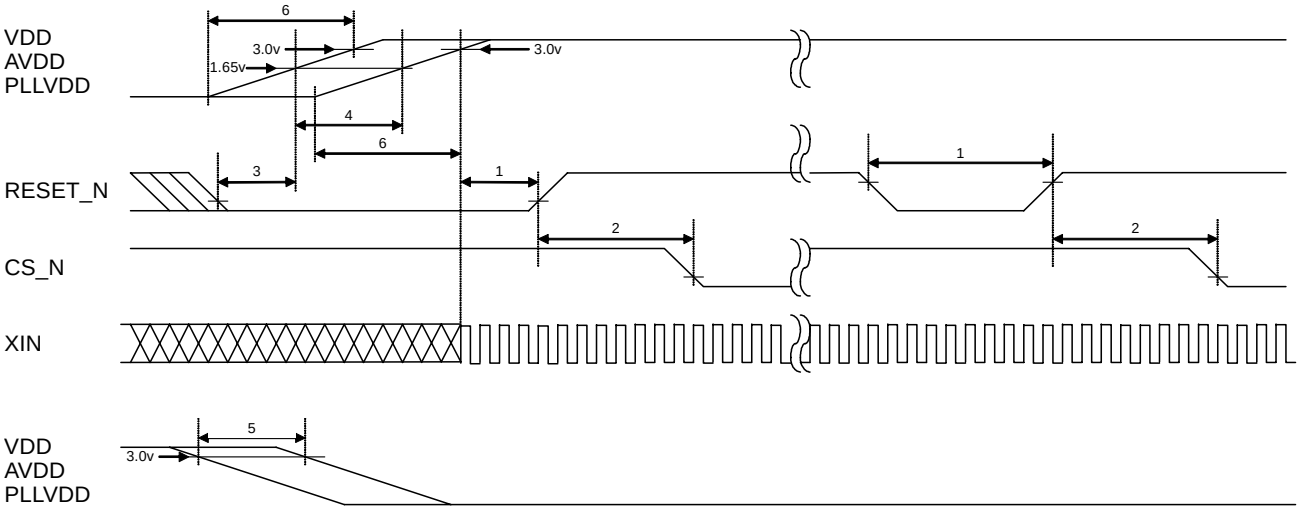
No.	items	Symbol	Min.	Typ.	Max.	Unit	Note
1	RESET_N pin Input Time	t_{wRES}	10			µs	1
2	RESET_N CPU access stand-by time after Negation	t_{wAW}	10			ms	
3	RESET_N Setup Time	t_{sRES}	0			ns	2
4	Time difference in power-on	t_{VSKWR}			1	S	3
5	Time difference in power-off	t_{VSKWF}			1	S	4
6	Power supply rise time	t_{VRISE}			200	ms	

Note1) The time is defined from a point where the latest VDD reached at 3.0 V and the clock to XIN pin became stable.

Note2) This is a specification to the VDD that rose fastest.

Note3) We recommend all the power supplies be powered on at the same time. Time difference in excess of 1 second may have an influence on reliability of the LSI.

Note4) We recommend all the power supplies be powered off at the same time. Time difference in excess of 1 second may have an influence on reliability of the LSI.



- CPU Interface

・Parallel Interface

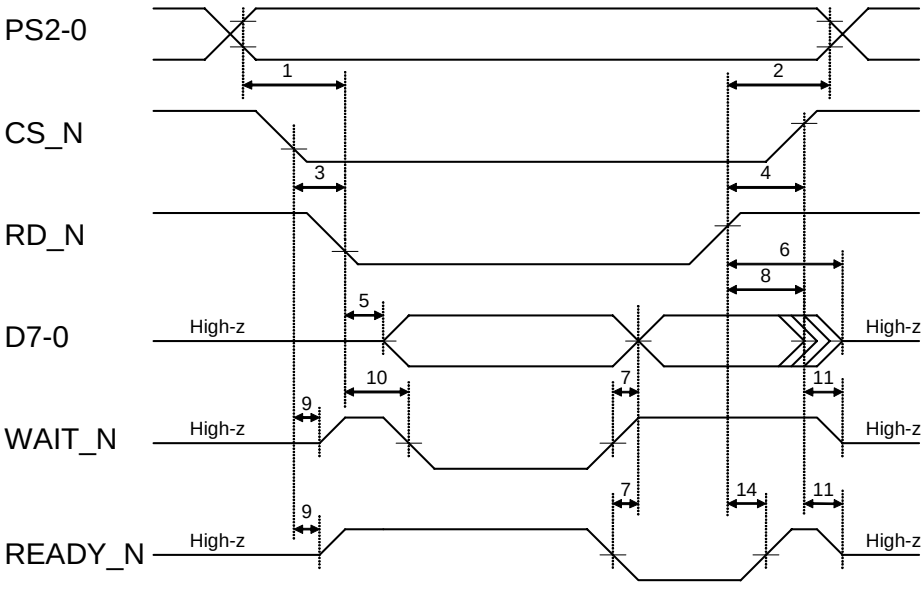
No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	PS2-0: setup time	t_{sA}	4			ns	1
2	PS2-0: hold time	t_{hA}	0				1
3	CS_N: setup time	t_{sCS}	0				2
4	CS_N: hold time	t_{hCS}	0				2
5	D7-0: output data turn on time	t_{onD}	0				
6	D7-0: output data turn off time	t_{offD}			10		
7	D7-0: output data valid delay time	t_{dD}			0		
8	D7-0: output data hold time	t_{hD}	0				
9	WAIT_N,READY_N: turn on time	t_{onWAIT}	0				
10	WAIT_N,READY_N: valid delay time	t_{dWAIT}			13		
11	WAIT_N,READY_N: turn off time	$t_{offWAIT}$			10		
12	D7-0: input data setup time	t_{sD}	t_{SYCLK}+10				
13	D7-0: input data hold time	t_{hD}	0				
14	READY_N: hold time	t_{hREADY}	0				
15	command pulse active time	t_{aCMD}	$2t_{SYCLK}$				3
16	command pulse inhibit time	t_{iCMD}	$4t_{SYCLK}$				3
17	command cycle time	t_{cCMD}	$6t_{SYCLK}$				3

Note1) Regulations for WR_N, RD_N signal. However, in CS_N control, these regulations are for CS_N.

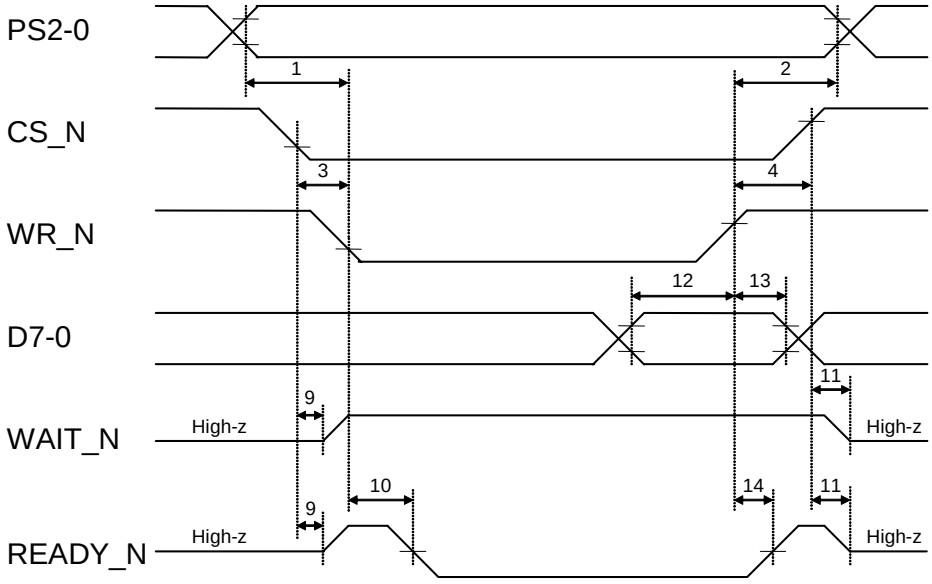
Note2) Conditions to be the control for WR_N, RD_N control. if it does not meet the regulation, the control turns into the CS_N control.

Note3) The command pulse means a low active pulse, which is made by the OR operation performed between each of WR_N and RD_N signal and CS_N signal.

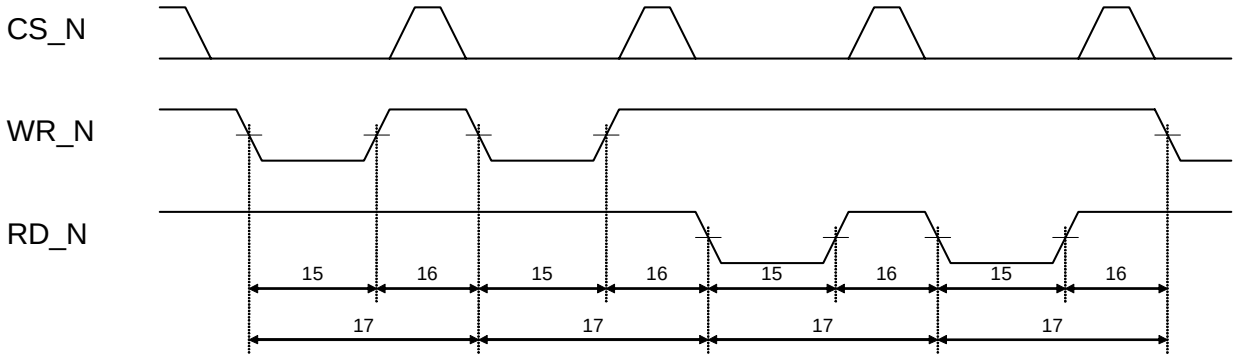
・CPU Read Cycle



・CPU Write Cycle

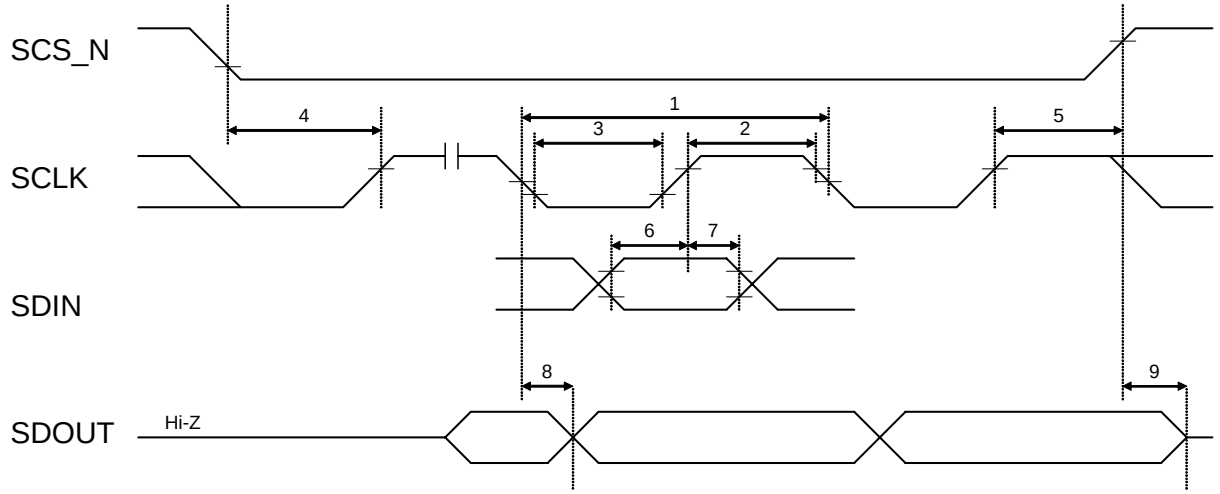


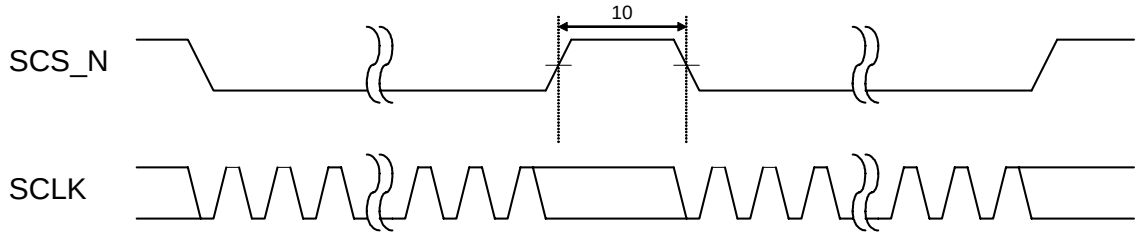
・Access Cycle



・Serial Interface

No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	SCLK Clock Cycle Time	t_{wSCLK}	400			ns	
2	SCLK Clock High Level Pulse Width	t_{whSCLK}	200				
3	SCLK Clock Low Level Pulse Width	t_{wlSCLK}	200				
4	SCS_N: setup time	t_{sSCS}	50				
5	SCS_N: hold time	t_{hSCS}	50				
6	SDIN: setup time	t_{sSDI}	50				
7	SDIN: hold time	t_{hSDI}	50				
8	SDOUT: output data delay time	t_{dSDO}			100		
9	SDOUT: turn off time	t_{offSDO}			20		
10	SCS_N:pulse inhibit time	t_{iSCS}			400		



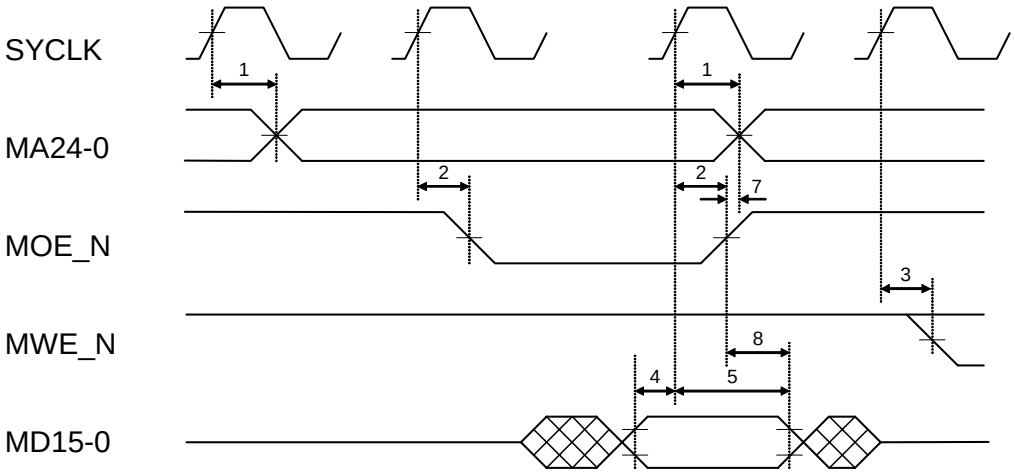


- Pattern Memory Interface

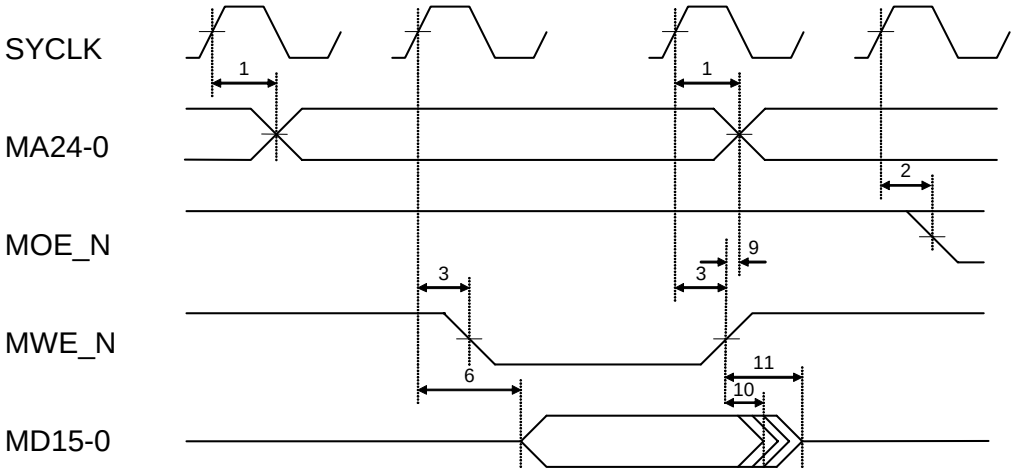
No.	Items	Symbol	Min.	Typ.	Max.	Unit	Note
1	MA24-0 : output delay time from SYCLK	t_{dMA}			16	ns	1
2	MOE_N : output delay time from SYCLK	t_{dOE}	2		11		1
3	MWE_N : output delay time from SYCLK	t_{dWE}	2		11		1
4	MD15-0 : input setup time to SYCLK	t_{sMD}	4				1
5	MD15-0 : input hold time from SYCLK	t_{hMD}	0				1
6	MD15-0 : output delay time from SYCLK	t_{dMD}			24		1
7	MA24-0 : hold time from MOE_N	t_{hMAR}	0				
8	MD15-0 : input hold time from MOE_N, MA	t_{hMDI}	0				
9	MA24-0 : hold time from MWE_N	t_{hMAW}	1				
10	MD15-0 : hold time from MWE_N	t_{hMDO}	1				
11	MD15-0 : turn off time from MWE_N	t_{offMDO}	1		6		
12	Output turn off/on time from /RAHZ	$t_{on/offRA}$			25		

Note1) SYCLK is an internal clock.

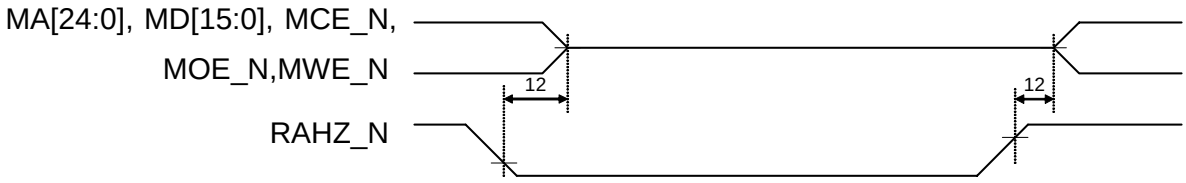
・Memory Access Cycle (Random Read Cycle)



・Memory Access Cycle (Write Cycle)



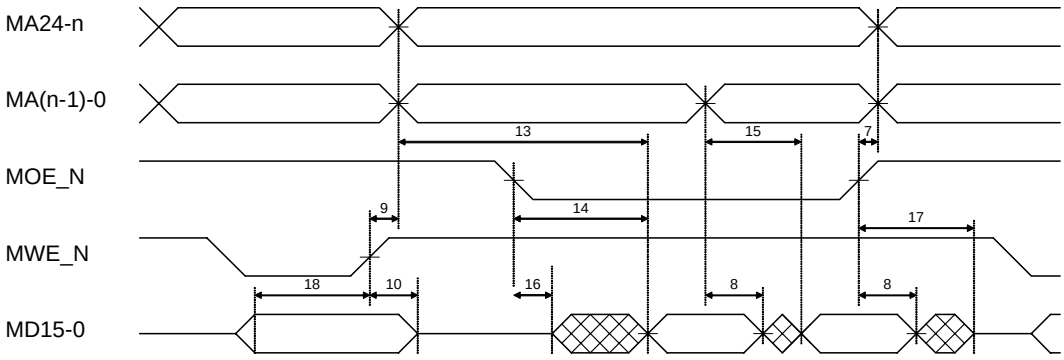
・RAHZ_N



The AC characteristics of the external memory, which connects to the VC1 must meet the following conditions. (The following conditions are the value, which are converted from the AC characteristics, and does not guarantee the following specification directly. And, the following name of the items is for the external memory connected. And, the following item names are mainly for the external memory connected.)

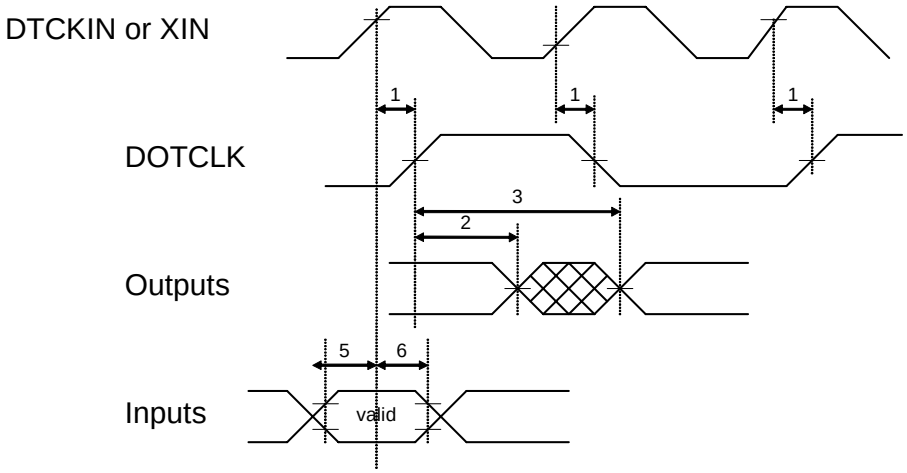
F in the following formula means the number of the Floating Clock that is set by R#23:FLTIM[1:0], and R means the number of the Random Access Clock that is set by R#24:RDM[3:0], and P means the number of the Page Mode Access Clock that is set by R#24:PAG[2:0]. Therefore, if a condition does not meet the following condition, set so that the register meets the following conditions.

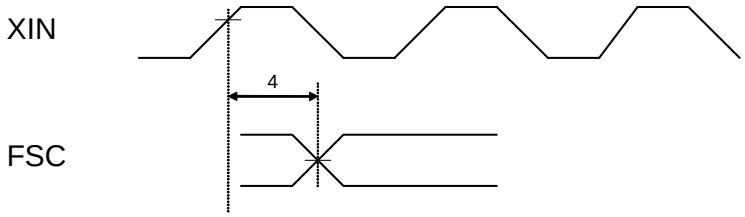
No.	Items	Conditions
13	Address, Access Time	It should be (F + R) * $t_{SYCLK} - t_{dMA}(max) - t_{sMD}(max)$ or lower.
14	Output Enable Time	It should be R * $t_{SYCLK} - t_{dOE}(max) - t_{sMD}(max)$ or lower.
15	Page Mode Access Time	It should be P * $t_{SYCLK} - t_{dMA}(max) - t_{sMD}(max)$ or lower.
16	Data Turn On Time	It should be 0[ns] or over
17	Data Turn Off Time	It should be F * t_{SYCLK} - $t_{dOE}(max) + t_{dWE}(min)$ or lower.
18	Data Setup Time	It should be R * t_{SYCLK} - $t_{dMD}(max) + t_{dWE}(min)$ or lower.



- Display Timing Signals

No.	Items	Symbol	Min.	Typ.	Max.	Unit
1	DOTCLK: delay time	t_{dDOTC}			20	ns
2	VSYNC_N,HCSYNC_N,BLANK_N,DR5-0,DG5-0, DB5-0, YS_N : output hold time	t_{hDISP}	0			ns
3	VSYNC_N,HCSYNC_N,BLANK_N,DR5-0,DG5-0, DB5-0, YS_N : output delay time	t_{dDISP}			10	ns
4	FSC: delay time	t_{dFSC}			20	ns
5	HSIN_N, VSIN_N: input setup time	t_{sSIN}	10			ns
6	HSIN_N, VSIN_N: input hold time	t_{hSIN}	0			ns





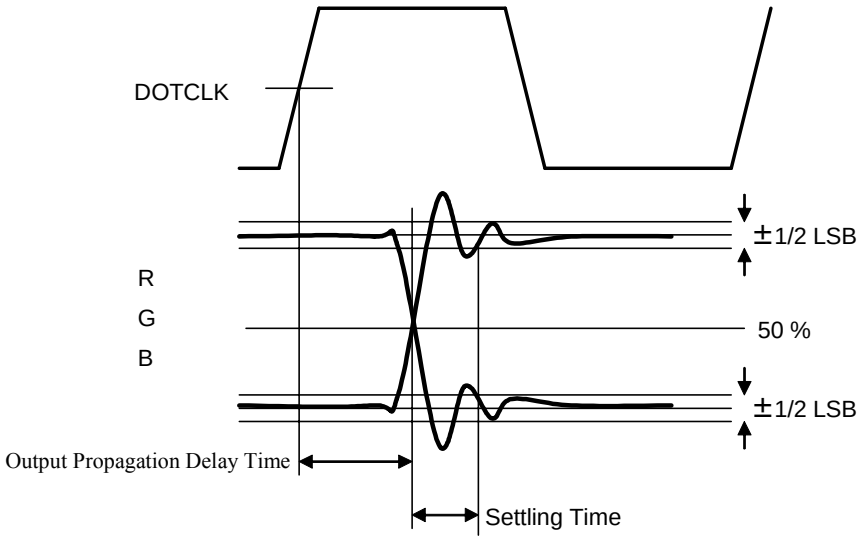
- Analog Characteristics

- RGB pin Output Characteristics

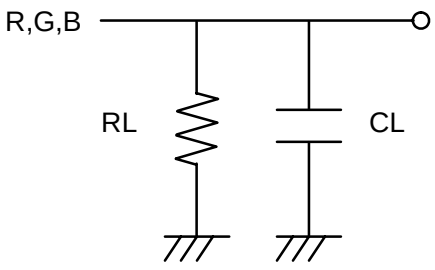
Items	Conditions	Min.	Typ.	Max.	Unit
Resolution	RL = 37.5Ω CL = 30 pF IREF = -9.38mA			6	bit
Settling Time				20	ns
Output Propagation Delay Time			0		ns
Output Voltage Amplitude (Vp-p)			0.7		V
Maximum Output Voltage (VWHITE)			0.7		V
Minimum Output Voltage (VBLACK)			0		V
Vp-p Deflection of R,G,B				3	%

Settling time is defined as the interval between the point at which DAC output level comes up to 50% and the point at which the output level reaches and stays within ±1/2 LSB centered on the resulting output level.

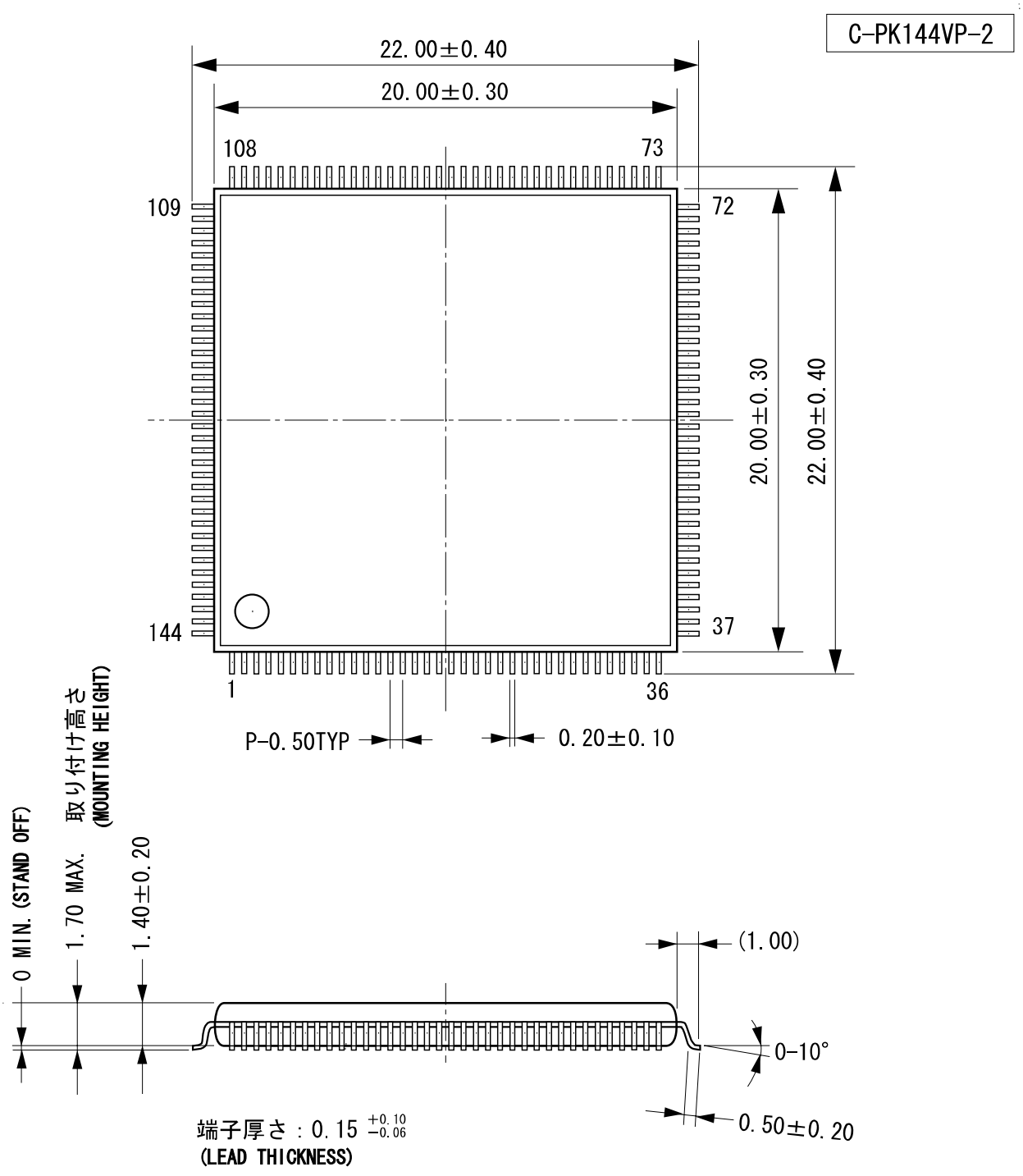
Output Propagation Delay Time is defined as the interval between the rising edge of DOTCLK and the point at which DAC output level comes up to 50%.



Measurement Circuit



■ Package Outline Drawing



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位：mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
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