

## 2N and 2P-Channel Enhancement Mode Power MOSFET

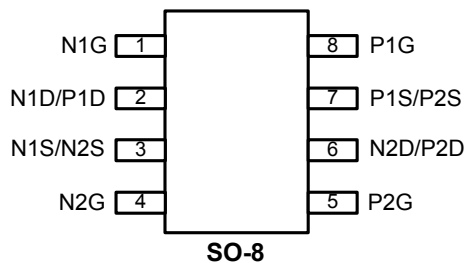
### ■ Features

- Simple Drive Requirement
- Low On-Resistance
- Full Bridge Application on LCD Monitor Inverter
- Pb Free Plating Product

### ■ Product Summary

CH	BV <sub>DSS</sub> (V)	R <sub>DS(ON)</sub> (mΩ)	I <sub>D</sub> (A)
N	30	40	4.3
P	-30	70	-3.3

### ■ Pin Assignments



### ■ General Description

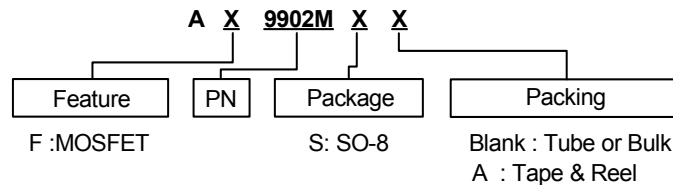
The advanced power MOSFET provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

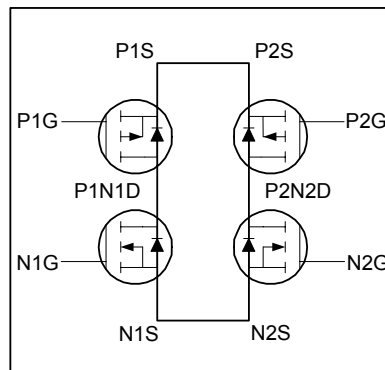
### ■ Pin Descriptions

Pin Name	Description
N1G	Gate (NMOS1)
N1D/P1D	Drain(NMOS1) / Drain(PMOS1)
N1S/N2S	Source(NMOS1) / Source(NMOS2)
N2G	Gate (NMOS2)
P2G	Gate (PMOS2)
N2D/P2D	Drain(NMOS2) / Drain(PMOS2)
P1S/P2S	Source(PMOS1) / Source(PMOS2)
P1G	Gate (PMOS1)

### ■ Ordering information



### ■ Block Diagram





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### ■ Absolute Maximum Ratings

Symbol	Parameter	N-Channel	P-Channel	Units
$V_{DS}$	Drain-Source Voltage	30	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	$\pm 12$	
$I_D$	Continuous Drain Current (Note 1)	$T_A=25^\circ\text{C}$	-3.3	A
		$T_A=70^\circ\text{C}$	-2.6	
$I_{DM}$	Pulsed Drain Current (Note 2)	20	-20	A
$P_D$	Total Power Dissipation	$T_A=25^\circ\text{C}$		W
	Linear Derating Factor			$W/^\circ\text{C}$
$T_{STG}$	Storage Temperature Range			$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range			$^\circ\text{C}$

### ■ Thermal Data

Symbol	Parameter	Value	Units
$R_{\theta JA}$	Thermal Resistance Junction-Ambient (Note 1)	Max. 90	$^\circ\text{C}/\text{W}$

### ■ Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits				Unit
			CH	Min.	Typ.	Max.	
$BV_{DSS}$	Drain-Source breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	N	30	-	-	V
		$V_{GS}=0\text{V}, I_D=-250\mu\text{A}$	P	-30	-	-	
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	N	-	0.03	-	$V/^\circ\text{C}$
		Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$	P	-	-0.02	-	
$R_{DS(ON)}$	Static Drain-Source On-Resistance (Note 3)	$V_{GS}=10\text{V}, I_D=5\text{A}$	N	-	-	40	m $\Omega$
		$V_{GS}=4.5\text{V}, I_D=4\text{A}$		-	-	50	
		$V_{GS}=2.5\text{V}, I_D=2\text{A}$		-	-	60	
		$V_{GS}=-10\text{V}, I_D=-4\text{A}$	P	-	-	70	
		$V_{GS}=-4.5\text{V}, I_D=-3\text{A}$		-	-	90	
		$V_{GS}=-2.5\text{V}, I_D=-2\text{A}$		-	-	120	
$V_{GS(th)}$	Gate-Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	N	0.5	-	-	V
		$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	P	-0.5	-	-	
$g_{fs}$	Forward Transconductance	$V_{DS}=5\text{V}, I_D=4\text{A}$	N	-	13	-	S
		$V_{DS}=-5\text{V}, I_D=-3\text{A}$	P	-	8	-	
$I_{DSS}$	Drain-Source Leakage Current	$T_J=25^\circ\text{C}$	N	-	-	1	uA
		$T_J=70^\circ\text{C}$		-	-	25	
		$T_J=25^\circ\text{C}$	P	-	-	-1	
		$T_J=70^\circ\text{C}$		-	-	-25	
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 12\text{V}$	N	-	-	$\pm 100$	nA
			P	-	-	$\pm 100$	
$Q_g$	Total Gate Charge (Note 3)	N-Channel $V_{DS}=24\text{V}, V_{GS}=4.5\text{V}$	N	-	9	15	nC
$Q_{gs}$	Gate-Source Charge	P-Channel $I_D=4\text{A}$	P	-	10	16	
			N	-	1.6	-	
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{DS}=-24\text{V}, V_{GS}=-4.5\text{V}$ $I_D=-3\text{A}$	N	-	4	-	
			P	-	3	-	



## 2N and 2P-Channel Enhancement Mode Power MOSFET

### ■ Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits				Unit
			CH	Min.	Typ.	Max.	
$t_{d(on)}$	Turn-On Delay Time (Note 3)	N-Channel $V_{DS}=15V, V_{GS}=5V$ $I_D=1A, R_G=3.3\Omega,$ $R_D=15\Omega$ P-Channel $V_{DS}=-15V, V_{GS}=-5V$ $I_D=-1A, R_G=3.3\Omega,$ $R_D=15\Omega$	N	-	8	-	ns
			P	-	8	-	
$t_r$	Rise Time		N	-	9	-	
			P	-	9	-	
$t_{d(off)}$	Turn-Off Delay Time		N	-	17	-	
			P	-	25	-	
$t_f$	Fall-Time		N	-	5	-	
			P	-	14	-	
$C_{iss}$	Input Capacitance	N-Channel $V_{GS}=0V, V_{DS}=25V$ $f=1.0\text{MHz}$ P-Channel $V_{GS}=0V, V_{DS}=-25V$ $f=1.0\text{MHz}$	N	-	630	1000	pF
			P	-	690	1100	
$C_{oss}$	Output Capacitance		N	-	140	-	
			P	-	170	-	
$C_{rss}$	Reverse Transfer Capacitance		N	-	65	-	
			P	-	75	-	

### ■ Source-Drain Diode

Symbol	Parameter	Test Conditions	Limits				Unit
			CH	Min.	Typ.	Max.	
$V_{SD}$	Forward On Voltage (Note 3)	$I_S=1.2A, V_{GS}=0V$	N	-	-	1.2	V
		$I_S=-1.2A, V_{GS}=0V$	P	-	-	-1.2	
$t_{rr}$	Reverse Recovery Time	N-Channel $I_S=4A, V_{GS}=0V$ $di/dt=100A/\mu s$ P-Channel $I_S=-3A, V_{GS}=0V$ $di/dt=-100A/\mu s$	N	-	17	-	ns
			P	-	25	-	
$Q_{rr}$	Reverse Recovery Charge		N	-	9	-	nC
			P	-	20	-	

**Note 1:** Surface Mounted on 1 in<sup>2</sup> copper pad of FR4 board;  $t \leq 10\text{sec}$ ;  $186^\circ\text{C/W}$  when mounted on Min. copper pad.

**Note 2:** Pulse width limited by Max. junction temperature

**Note 3:** Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .

## 2N and 2P-Channel Enhancement Mode Power MOSFET

### Typical Performance Characteristics (N-Channel)

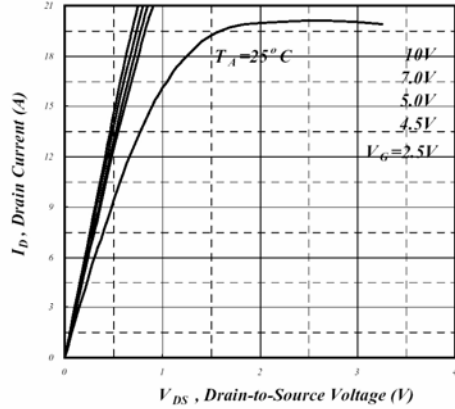


Fig 1. Typical Output Characteristics

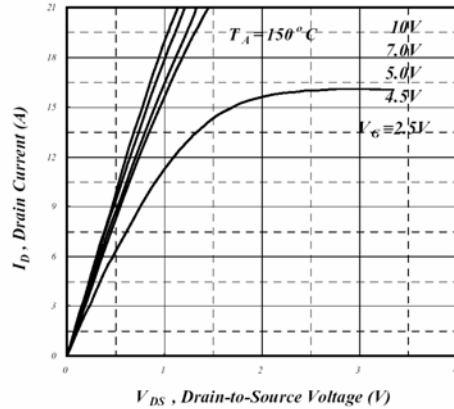


Fig 2. Typical Output Characteristics

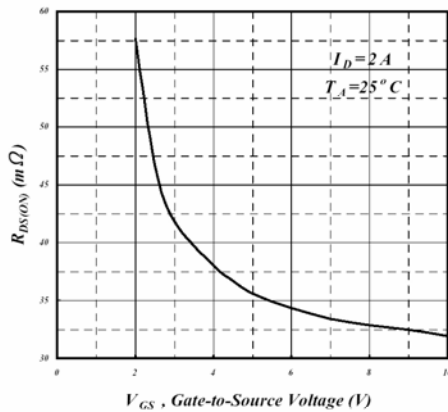


Fig 3. On-Resistance v.s. Gate Voltage

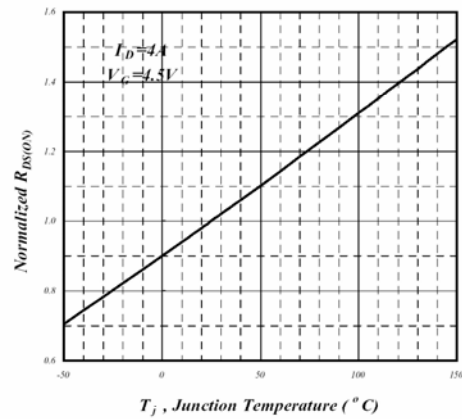


Fig 4. Normalized On-Resistance v.s. Junction Temperature

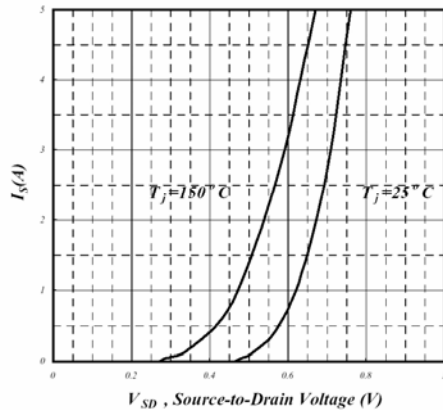


Fig 5. Forward Characteristic of Reverse Diode

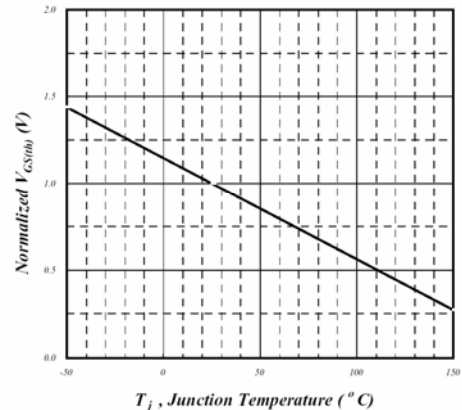


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

## 2N and 2P-Channel Enhancement Mode Power MOSFET

### ■ Typical Performance Characteristics (N-Channel) (Continued)

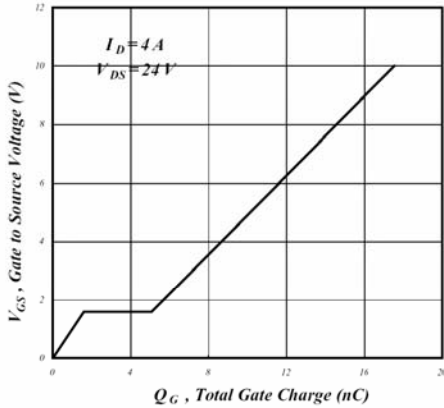


Fig 7. Gate Charge Characteristics

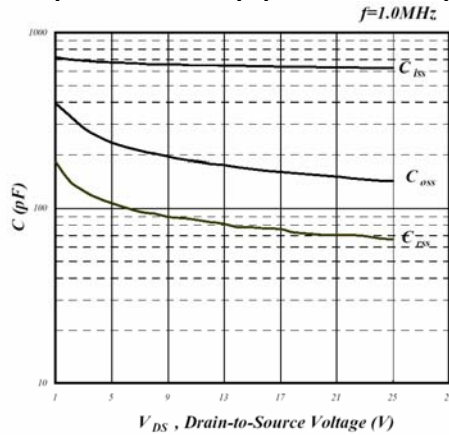


Fig 8. Typical Capacitance Characteristics

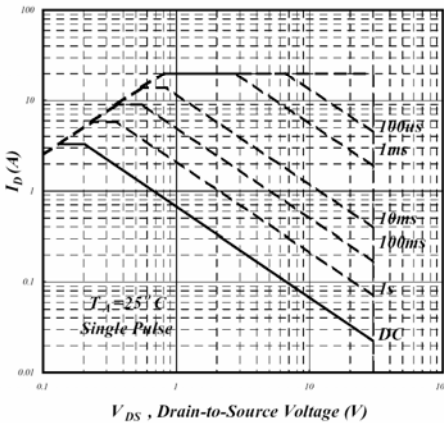


Fig 9. Maximum Safe Operating Area

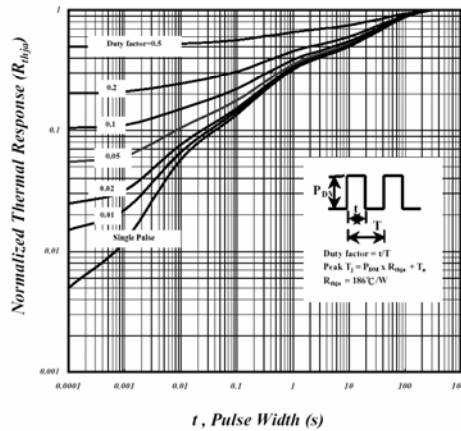


Fig 10. Effective Transient Thermal Impedance

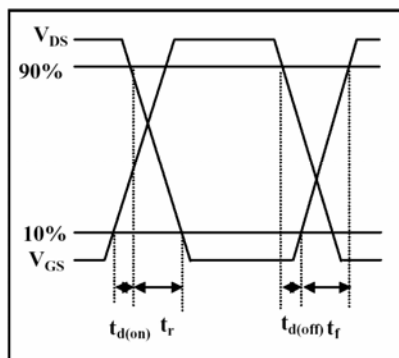


Fig 11. Switching Time Waveform

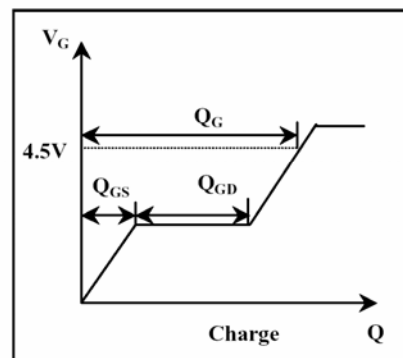


Fig 12. Gate Charge Waveform

## 2N and 2P-Channel Enhancement Mode Power MOSFET

### Typical Performance Characteristics (P-Channel)

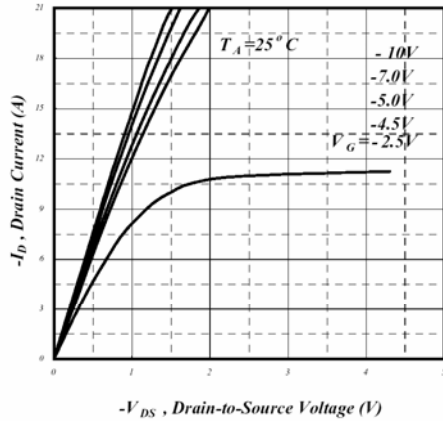


Fig 1. Typical Output Characteristics

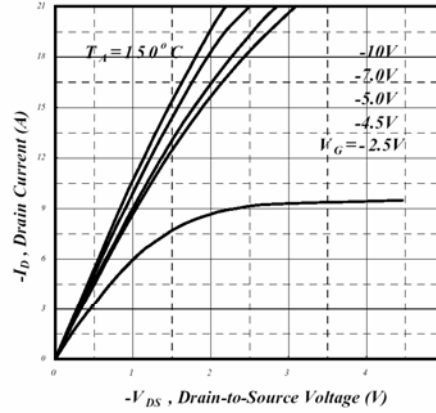


Fig 2. Typical Output Characteristics

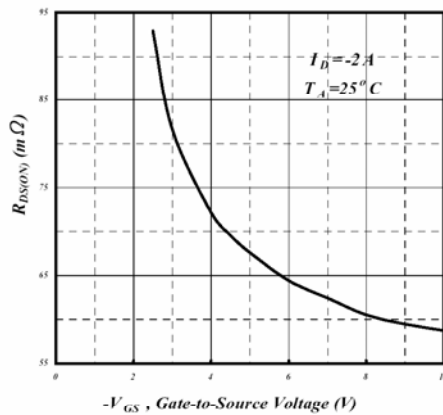


Fig 3. On-Resistance v.s. Gate Voltage

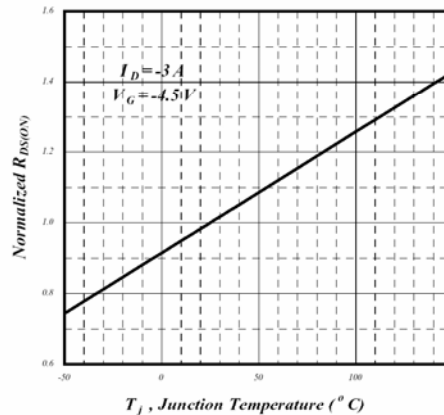


Fig 4. Normalized On-Resistance v.s. Junction Temperature

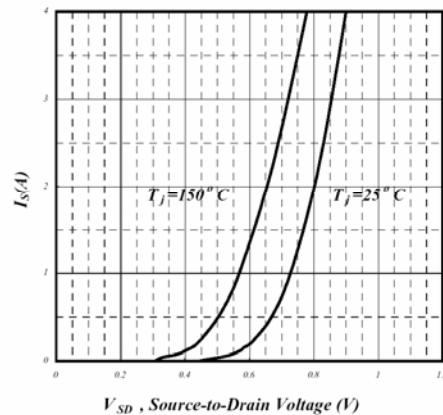


Fig 5. Forward Characteristic of Reverse Diode

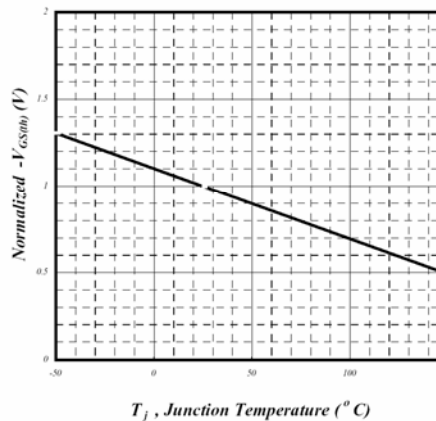


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

## 2N and 2P-Channel Enhancement Mode Power MOSFET

### ■ Typical Performance Characteristics (P-Channel) (Continued)

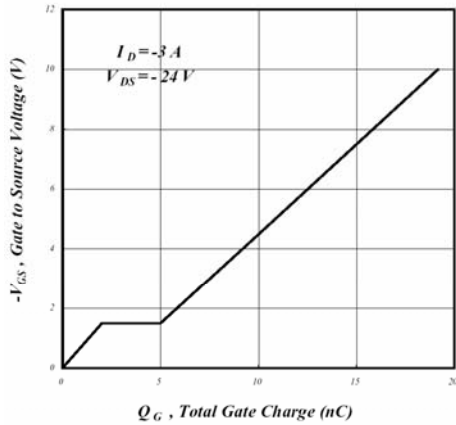


Fig 7. Gate Charge Characteristics

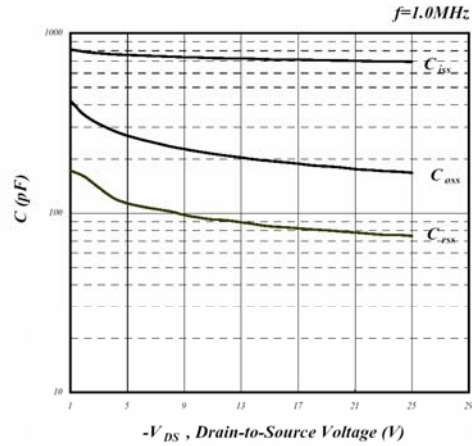


Fig 8. Typical Capacitance Characteristics

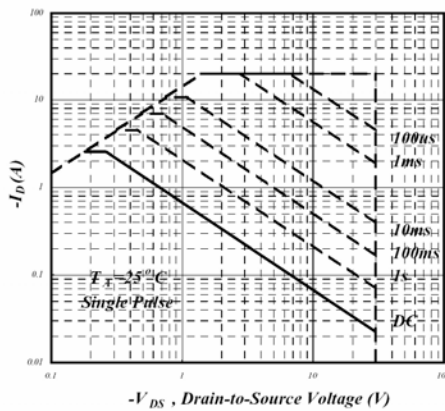


Fig 9. Maximum Safe Operating Area

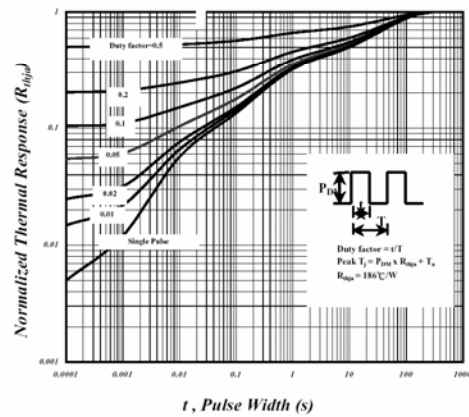


Fig 10. Effective Transient Thermal Impedance

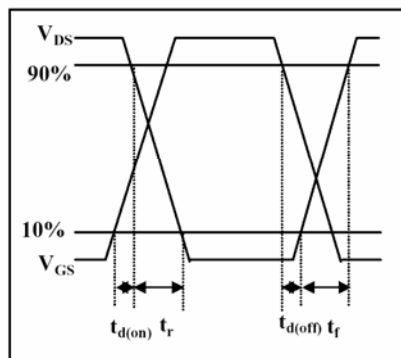


Fig 11. Switching Time Waveform

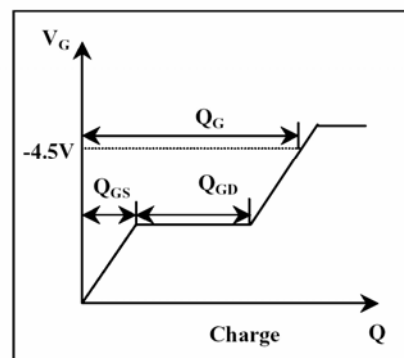
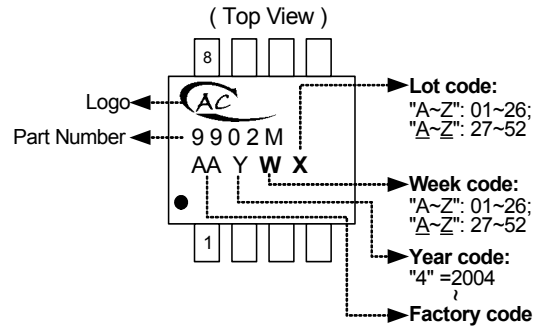


Fig 12. Gate Charge Waveform

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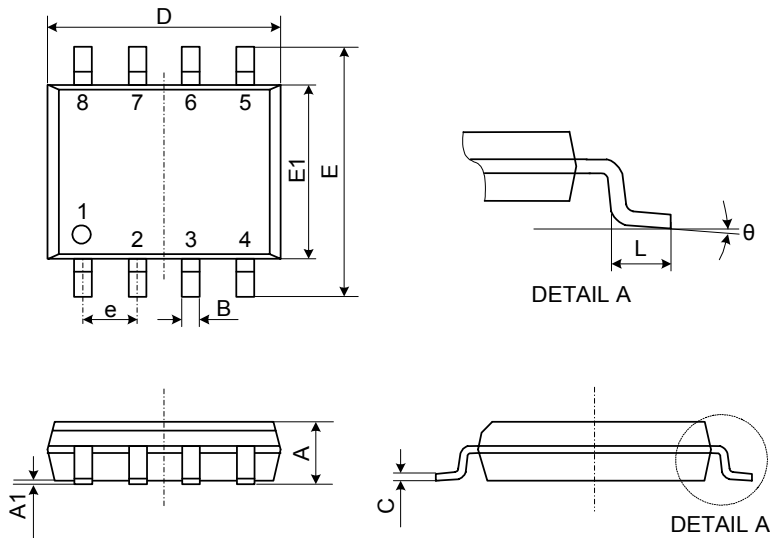
### ■ Marking Information

SO-8L



### ■ Package Information

Package Type: SO-8L



1. All Dimensions Are in Millimeters.
2. Dimension Does Not Include Mold Protrusions.

Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
B	0.33	0.41	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E	5.80	6.15	6.50
E1	3.80	3.90	4.00
L	0.38	0.71	1.27
$\theta$	0°	4°	8°
e	1.27 TYP.		