November 1994, Rev A FN7164

Triple 80MHz Video Amplifier with DC Restore

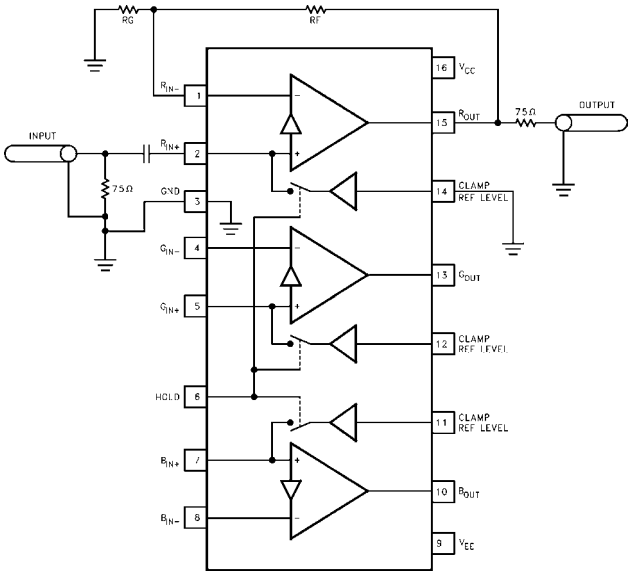
The EL4390 is three wideband current-mode feedback amplifiers optimized for video performance, each with a DC restore amplifier. The DC restore function is activated by a common TTL/CMOS compatible control signal while each channel has a separate restore reference.

Each amplifier can drive a load of 150Ω at video signal levels. The EL4390 operates on supplies as low as ±4V up to ±15V.

Being a current-mode feedback design, the bandwidth stays relatively constant at approximately 80MHz over the ±1 to ±10 gain range. The EL4390 has been optimized for use with 1300Ω feedback resistors.

Pinout

EL4390
(16-PIN PDIP, SO)
TOP VIEW



Features

- 80MHz -3dB bandwidth for gains of 1 to 10
- 800V/µs slew rate
- 15MHz bandwidth flat to 0.1dB
- Excellent differential gain and phase
- TTL/CMOS compatible DC restore function
- Available in 16-pin PDIP, 16-pin SOL

Applications

- RGB drivers requiring DC restoration
- RGB multiplexers requiring DC restoration
- RGB building blocks
- Video gain blocks requiring DC restoration
- Sync and color burst processing

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL4390CN	-40°C to +85°C	16-Pin PDIP	MDP0031
EL4390CM	-40°C to +85°C	16-Pin SOL	MDP0027

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S+ and GND . . . . . +12.6V
Input Voltage (IN+, IN-, ENABLE, CLAMP) . . . GND -0.3V, V_S +0.3V
V_S Supply Voltage . . . . . ±18V or 36V
V_{IN} Input Voltage . . . . . ±15V or V_S
ΔV_{IN} Differential Input Voltage . . . . . ±6V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications

Supplies at ±15V, Load = 1kΩ

PARAMETER	DESCRIPTION	TEMP	MIN	TYP	MAX	UNITS
AMPLIFIER SECTION (NOT RESTORED)						
V_{OS}	Input Offset Voltage	+25°C		2	15	mV
I_B+	I_{IN}+ Input Bias Current	+25°C		0.2	5	µA
I_B-	I_{IN}- Input Bias Current	+25°C		10	65	µA
R_{OL}	Transimpedance (Note 1)	+25°C	100	220		kΩ
R_{IN}-	I_N- Resistance	+25°C		50		Ω
CMRR	Common-Mode Rejection Ratio (Note 2)	+25°C	50	56		dB
PSRR	Power Supply Rejection Ratio (Note 3)	+25°C	50	70		dB
V_O	Output Voltage Swing; R_L = 1kΩ	+25°C	±12	±13		V
I_{SC}	Short-Circuit Current	+25°C	45	70	100	mA
I_{SY}	Supply Current (Quiescent)	+25°C	10	20	32	mA
RESTORING SECTION						
V_{OS}, COMP	Composite Input Offset Voltage (Note 4)	+25°C		8	35	mV
I_B+, R	Restore I_N+ Input Bias Current	+25°C		0.2	5	µA
I_{OUT}	Restoring Current Available	+25°C	2	4		mA
PSRR	Power Supply Rejection Ratio (Note 3)	+25°C	50	70		dB
G_{OUT}	Conductance	+25°C		8		mA/V
I_{SY}, RES	Supply Current, Restoring	+25°C	10	23	37	mA
V_{IL}, RES	RES Logic Low Threshold	+25°C		1.0	1.4	V
V_{IH}, RES	RES Logic High Threshold	+25°C	1.4	1.8		V
I_{IL}, RES	RES Input Current, Logic Low	+25°C		2	10	µA
I_{IH}, RES	RES Input Current, Logic High	+25°C		0.5	3	µA

NOTES:

1. For current feedback amplifiers, $A_{VOL} = R_{OL}/R_{IN}$-
2. V_{CM} = ±10V for V_S = ±15V.
3. V_{OS} is measured at V_S = ±4.5V and V_S = ±16V, both supplies are changed simultaneously.
4. Measured from V_{CL} to amplifier output, while restoring.

Closed-Loop AC Electrical Specifications

Supplies at ±15V, Load = 150Ω and 15pF, T_A = 25°C (Note 1)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
AMPLIFIER SECTION					
SR	Slew Rate (Note 1)		800		V/µs
SR	Slew Rate w/ ±5V Supplies (Note 2)		550		V/µs
BW	Bandwidth, -3dB, A_V = 1 ±5V Supplies, -3dB		95 72		MHz MHz
BW	Bandwidth, -0.1dB ±5V Supplies, -0.1dB		20 14		MHz MHz
dG	Differential Gain at 3.58MHz at ±5V Supplies (Note 3)		0.02 0.02		% %
dθ	Differential Phase at 3.58MHz at ±5V Supplies (Note 3)		0.03 0.06		(°) (°)
RESTORING SECTION					
T_{RE}	Time to Enable Restore		35		ns
T_{RD}	Time to Disable Restore		35		ns

NOTES:

1. Test fixture was designed to minimize capacitance at the I_N- input. A “good” fixture should have less than 2pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.
2. SR is measured at 20% to 80% of 4Vpk-pk square wave, with A_V = 5, R_F = 820Ω, R_G = 200Ω.
3. DC offset from -0.714V to +0.714V, AC amplitude is 286mV_{P-P}, equivalent to 40 ire.

TABLE 1. CHARGE STORAGE CAPACITOR VALUE VS. DROOP AND CHARGING RATES

CAP VALUE (NF)	DROOP IN 60µS (MV)	CHARGE IN 2µS (MV)	CHARGE IN 4µS (MV)
10	30	400	800
22	13.6	182	364
47	6.4	85	170
100	3.0	40	80
220	1.36	18	36

These numbers represent the worst case bias current, and the worst case charging current. Note that to get the full (2mA+) charging current, the clamp input must have >250mV of error voltage.

Note that the magnitude of the bias current will decrease as temperature increases.

The basic droop formula is:

V (droop) = $I_{B+} \times$ (Line time - Charge time) / capacitor value

and the basic charging formula is:

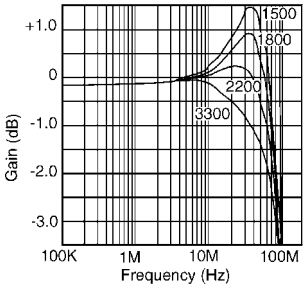
V (charge) = $I_{OUT} \times$ Charge time / capacitor value

Where I_{OUT} is:

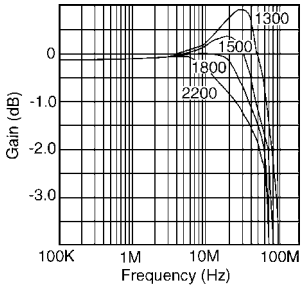
I_{OUT} = (Clamp voltage - IN+ voltage) / 120

Typical Performance Curves

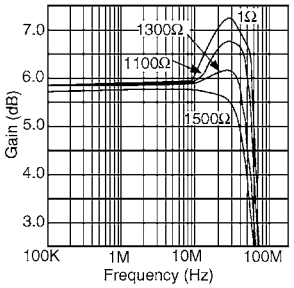
Gain Flatness for Various R_F
V_S = ±15V, A_V = 0dB



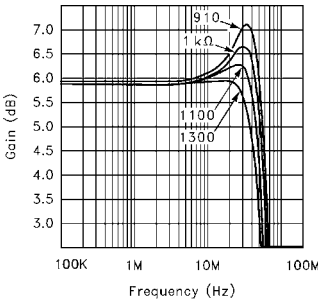
Gain Flatness for Various R_F
V_S = ±5V, A_V = 0dB



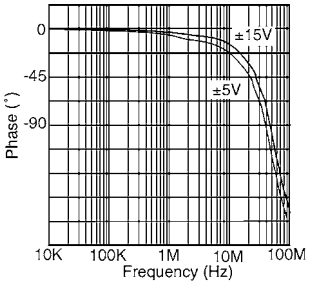
Gain Flatness
for Various R_F and R_G Values
V_S = ±15V, A_V = 6dB



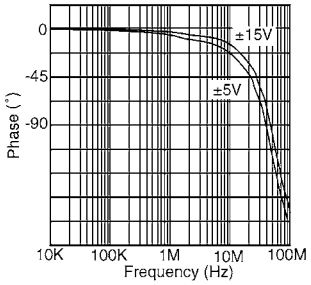
Gain Flatness
for Various R_F and R_G Values
V_S = ±5V, A_V = 6dB



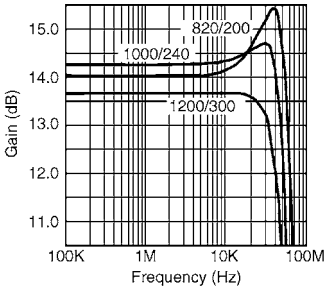
Phase Shift for A_V = 2,
$R_F = R_G$ = 1300Ω



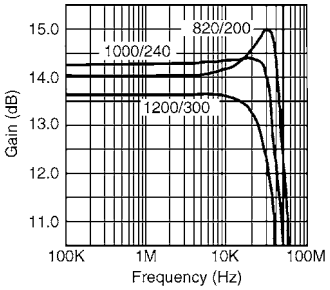
Phase Shift for A_V = 2,
$R_F = R_G$ = 1000Ω
at V_S = ±5V and V_S = ±15V



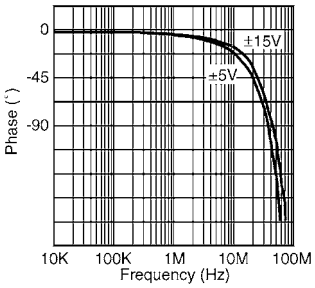
Gain Flatness
V_S = ±15V, A_V = 14dB,
R_F/R_G as Shown



Gain Flatness
V_S = ±5V, A_V = 14dB,
R_F/R_G as Shown

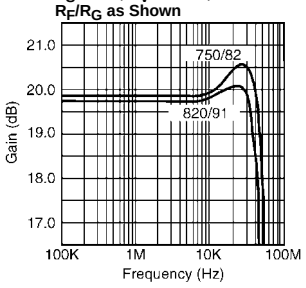


Phase Shift
for A_V = 5dB, R_F = 820Ω,
R_G = 200Ω, V_S = ±5V

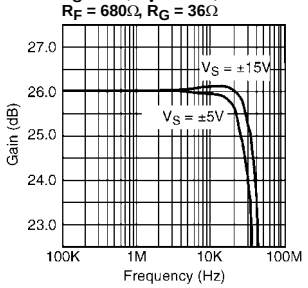


Typical Performance Curves (Continued)

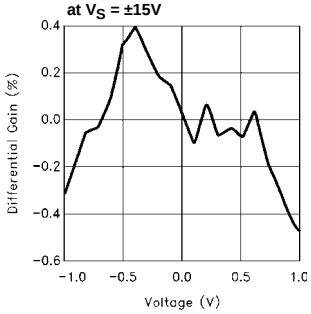
Gain Flatness
V_S = ±5V, A_V = 20dB,
R_F/R_G as Shown



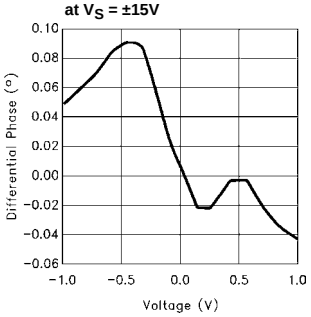
Gain Flatness
V_S = ±5V, A_V = 26dB,
R_F = 680Ω, R_G = 36Ω



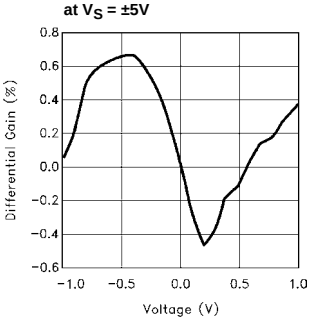
Differential Gain
at V_S = ±15V



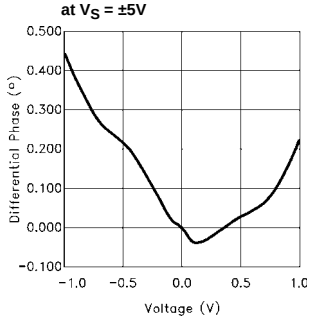
Differential Phase
at V_S = ±15V



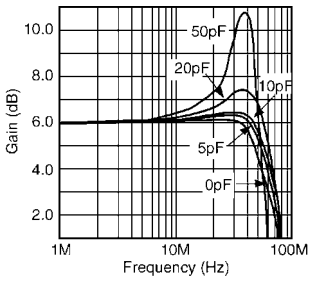
Differential Gain
at V_S = ±5V



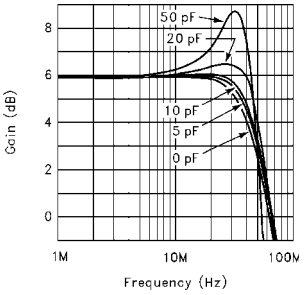
Differential Phase
at V_S = ±5V



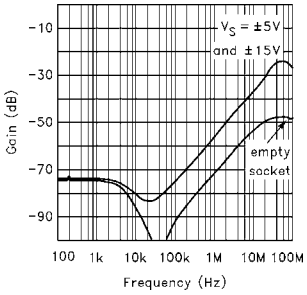
Frequency Response
for Various C_{LOAD}, V_S = ±15V,
$R_F = R_G$ = 1300Ω



Frequency Response
for Various C_{LOAD}, V_S = ±5V,
$R_F = R_G$ = 1300Ω

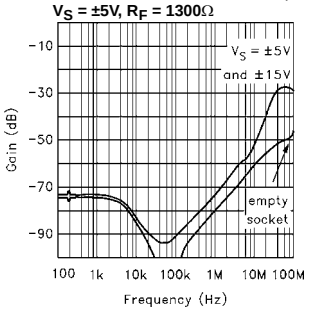


Crosstalk,
Channel R and B to Channel G,
V_S = ±5V, R_F = 1300Ω

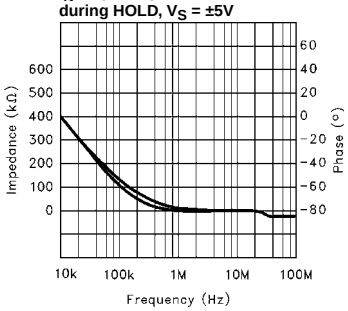


Typical Performance Curves (Continued)

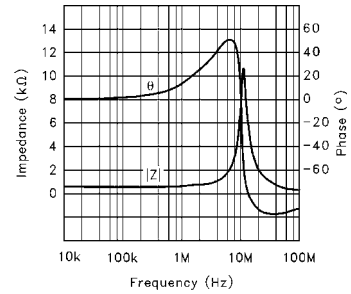
Crosstalk, Channel R and G to Channel B, V_S = ±5V, R_F = 1300Ω



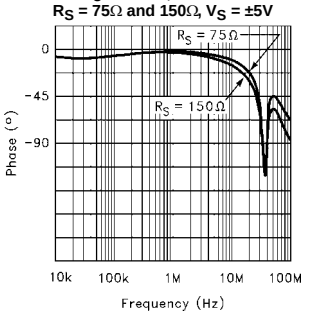
I_N+ Input Impedance during HOLD, V_S = ±5V



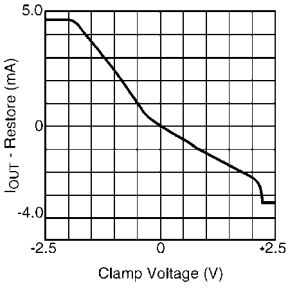
I_N+ Input Impedance during SAMPLE, V_S = ±5V



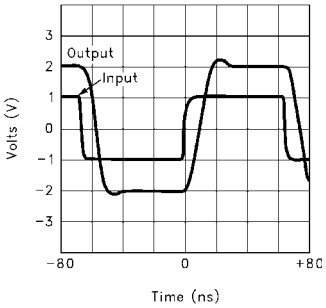
Phase Shift at I_N+ Pin during Restore, R_S = 75Ω and 150Ω, V_S = ±5V



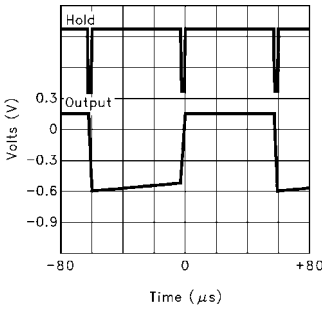
I_{OUT} Restoring vs Clamp, Voltage at V_S = ±5V



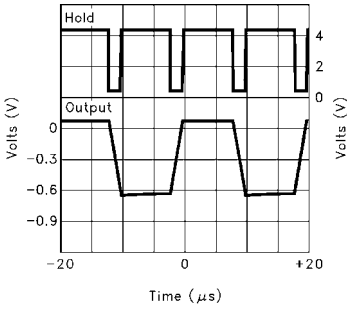
Pulse Response with A_V = 2, R_F = R_G = 1300Ω at V_S = ±5V



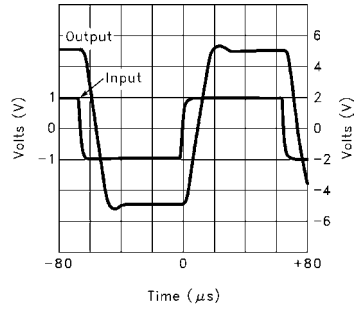
Output during DC-Restoration, Showing DC Droop R_F = R_G = 1300Ω, V_S = ±5V



Output during DC-Restoration, R_F = R_G = 1300Ω, V_S = ±5V

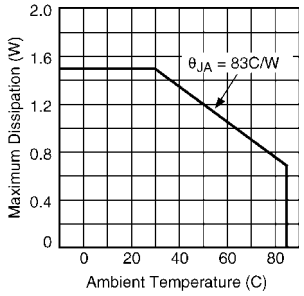


Pulse Response with A_V = 5, R_F = 820Ω and R_G = 200Ω at V_S = ±15V

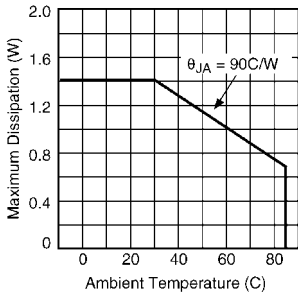


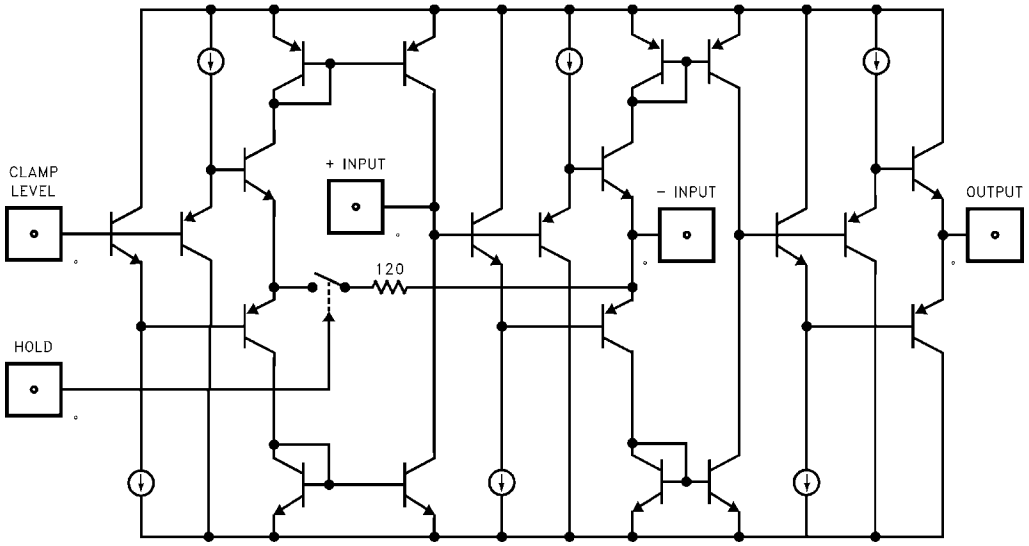
Typical Performance Curves (Continued)

Maximum Power Dissipation vs Ambient Temperature— 16-Pin PDIP



Maximum Power Dissipation vs Ambient Temperature— 16-Pin PDIP





Simplified Schematic of One Channel of EL4390

Applications Information

Circuit Operation

Each channel of the EL4390 contains a current feedback amplifier and a TTL/CMOS compatible clamp circuit. The current that the clamp can source or sink into the non-inverting input is approximately:

$I = (V_{CLAMP} - V_{IN}+) / 120$

So, when the non-inverting input is at the same voltage as the clamp reference, no current will flow, and hence no charge is added to the capacitor. When there is a difference in voltage, current will flow, in an attempt to cancel the error AT THE NON-INVERTING input. The amplifier's offset voltage and ($I_B- \times R_F$) DC errors are not cancelled with this loop. It is purely a method of adding a controlled DC offset to the signal.

As well as the offset voltage error, which goes up with gain, and the $I_B- \times R_F$ error which drops with gain, there is also the I_B+ error term. Since the amplifier is capacitively coupled, this small current is slowly integrated and shows up as a very slow ramp voltage. Table below shows the output

voltage drift in 60µS for various values of coupling capacitor, all assuming the very worst I_B+ current.

TABLE 2. CHARGE STORAGE CAPACITOR VALUE VS. DROOP AND CHARGING RATES

CAP VALUE (NF)	DROOP IN 60µS (MV)	CHARGE IN 2µS (MV)	CHARGE IN 4µS (MV)
10	30	400	800
22	13.6	182	364
47	6.4	85	170
100	3.0	40	80
220	1.36	18	36

In normal circuit operation, the picture content will also cause a slow change in voltage across the capacitor, so at every back porch time period, these error terms can be corrected.

When a signal source is being switched, e.g., from two different surveillance cameras, it is recommended to synchronize the switching with the vertical blanking period, and to drive the HOLD pin (pin 6) low, during these lines. This will ensure that the system has been completely restored, regardless of the average intensity of the two pictures.

Application Hints

Figures 1 & 2 shows a three channel DC-restoring system, suitable for R-G-B or Y-U-V component video, or three synchronous composite signals.

Figure 1 shows the amplifiers configured for non-inverting gain, and Figure 2 shows the amplifiers configured for inverting gains. Note that since the DC-restoring function is accomplished by clamping the amplifier's non-inverting input, during the back porch period, any signal on the non-inverting input will be distorted. For this reason, it is recommended to use the inverting configuration for composite video, since this avoids the color burst being altered during the clamp time period.

Since all three amplifiers are monolithic, they run at the same temperature, and will have very similar input bias currents. This can be used to advantage, in situations where the droop voltage needs to be compensated, since a single trim circuit can be used for all three channels. A 560kΩ or similar value resistor helps to isolate each signal. See Figure 2. The advantage of compensating for the droop voltage, is that a smaller capacitor can be used, which allows a larger level restoration within one line. See Table 1 for values of capacitor and charge/droop rates.

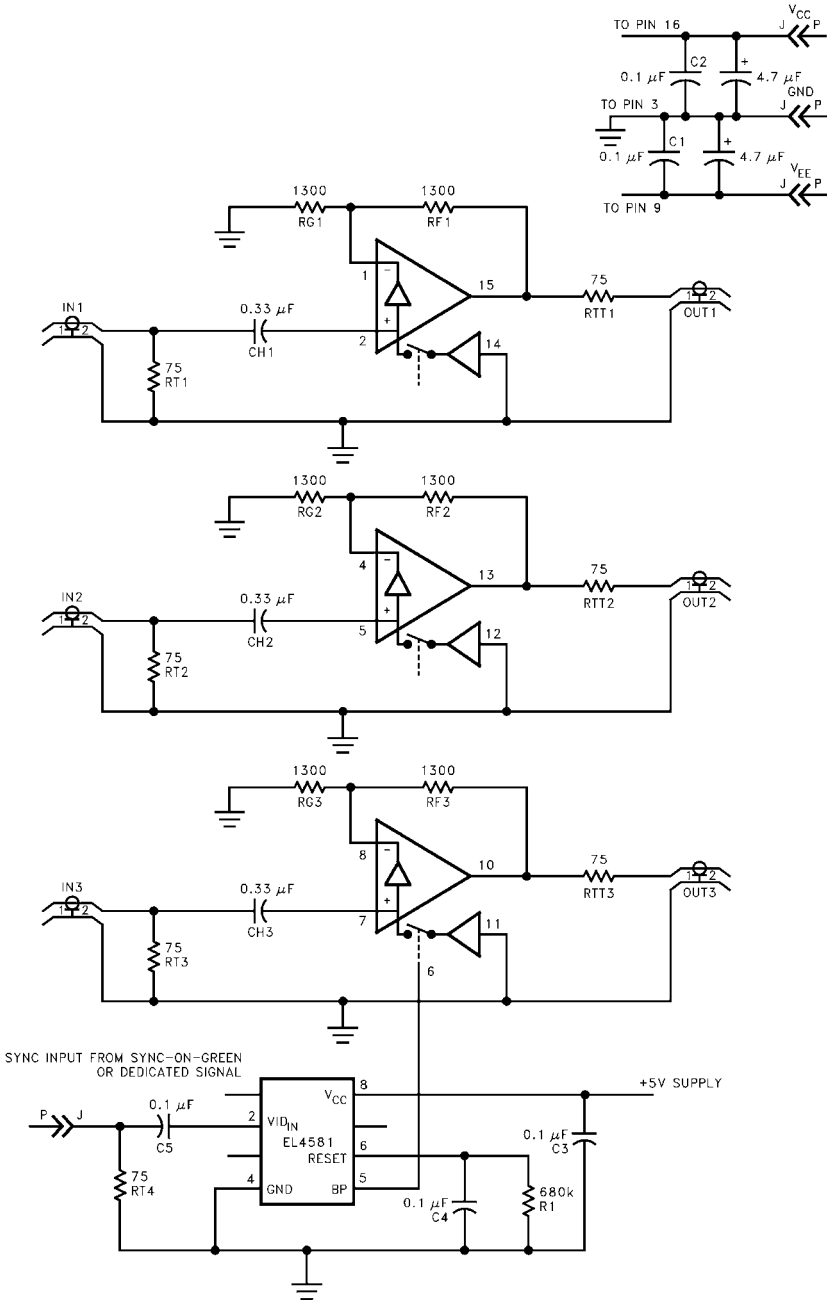

TO PIN 16
V_{CC}
0.1 µF
C2
4.7 µF
GND
TO PIN 3
C1
0.1 µF
4.7 µF
V_{EE}
TO PIN 9
1300
RG1
1300
RF1
IN1
0.33 µF
CH1
75
RT1
75
RTT1
OUT1
1300
RG2
1300
RF2
IN2
0.33 µF
CH2
75
RT2
75
RTT2
OUT2
1300
RG3
1300
RF3
IN3
0.33 µF
CH3
75
RT3
75
RTT3
OUT3
SYNC INPUT FROM SYNC-ON-GREEN
OR DEDICATED SIGNAL
0.1 µF
C5
75
RT4
VID_{IN}
EL4581
RESET
GND
BP
V_{CC}
+5V SUPPLY
0.1 µF
C3
0.1 µF
C4
680k
R1

FIGURE 1.

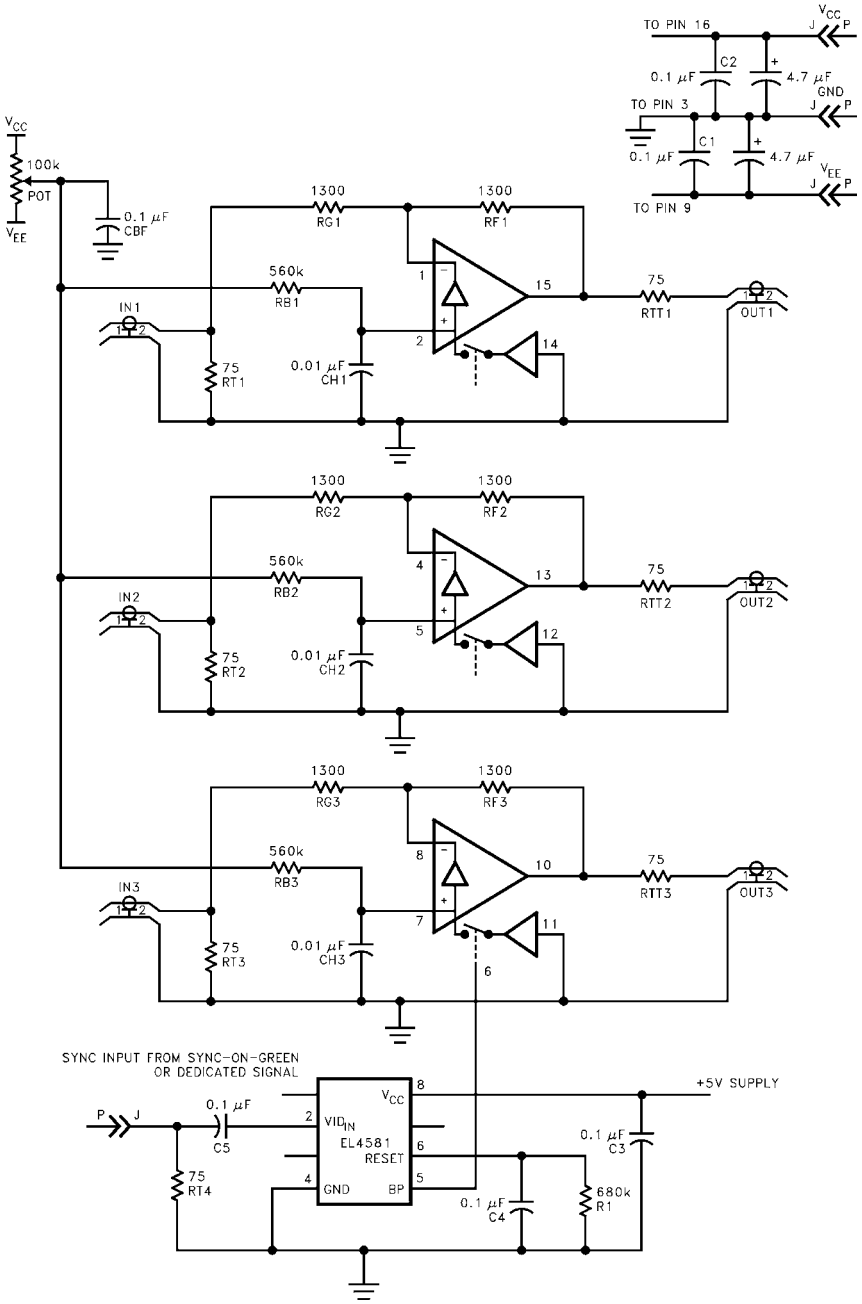

TO PIN 16
V_{CC}
J P
0.1 µF
C2
4.7 µF
GND
TO PIN 3
J P
C1
0.1 µF
4.7 µF
V_{EE}
J P
TO PIN 9
V_{CC}
100k
POT
V_{EE}
0.1 µF
CBF
1300
RG1
1300
RF1
560k
RB1
IN1
75
RT1
0.01 µF
CH1
75
RTT1
OUT1
1300
RG2
1300
RF2
560k
RB2
IN2
75
RT2
0.01 µF
CH2
75
RTT2
OUT2
1300
RG3
1300
RF3
560k
RB3
IN3
75
RT3
0.01 µF
CH3
75
RTT3
OUT3
SYNC INPUT FROM SYNC-ON-GREEN
OR DEDICATED SIGNAL
P J
0.1 µF
C5
75
RT4
V_{CC}
VID_{IN}
EL4581
RESET
GND
BP
+5V SUPPLY
0.1 µF
C3
0.1 µF
C4
680k
R1

FIGURE 2.

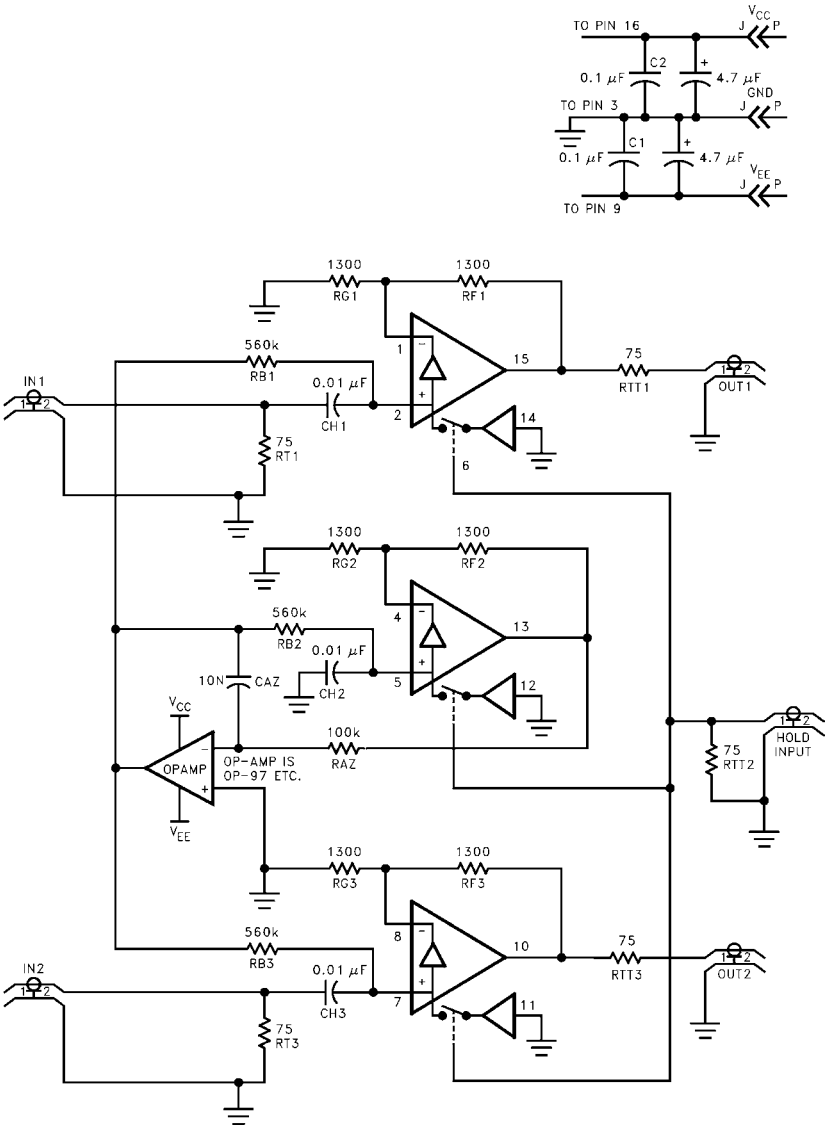


FIGURE 3.

In Figure 3, one of the three channels is used, together with a low-offset op-amp, to automatically trim the bias current of the other two channels. The two remaining channels are shown in the non-inverting configuration, but could equally well be set to provide inverting gains. Two DC-restored channels are typically needed in fader applications. See the EL4094 and EL4095 for suitable, monolithic video faders.

Layout and Dissipation Considerations

As with all high frequency circuits, the supplies should be bypassed with a 0.1µF ceramic capacitor very close to the supply pins, and a 4.7µF tantalum capacitor fairly close, to handle the high current surges. While a ground plane is recommended, the amplifier will work well with a “star” grounding scheme. The pin 3 ground is only used for the internal bias generator and the reference for the TTL compatible “HOLD” input.

As with all current feedback capacitors, all stray capacitance to the inverting inputs should be kept as low as possible, to avoid unwanted peaking at the output. This is especially true if the value of R_F has already been reduced to raise the bandwidth of the part, while tolerating some peaking. In this situation, additional capacitance on the inverting input can lead to an unstable amplifier.

Since there are three amplifiers all in one package, and each amplifier can sink or source typically more than 70mA, some care is needed to avoid excessive die temperatures. Sustained, DC currents, of over 30mA, are not recommended, due to the limited current handling capability of the metal traces inside the IC. Also, the short circuit

protection can be tripped with currents as low as 45mA, which is seen as excessive distortion in the output waveform. As a quick rule of thumb, both the SOL and DIP 16 pin packages can dissipate about 1.4 watts at 25°C, and with ±15V supplies and a worst case quiescent current of 32mA, yields 0.96 watts, before any load is driven.

Dissipation of the EL4390 can be reduced by lowering the supply voltage. Although some performance is degraded at lower supplies, as seen in the characteristic curves, it is often found to be a useful compromise. The bandwidth can be recovered, by reducing the value of R_F, and R_G as appropriate.