LOW SKEW, 1-TO-9 DIFFERENTIAL-TO-LVCMOS ZERO DELAY BUFFER

# ICS87951I-147

GENERAL DESCRIPTION

The ICS87951I-147 is a low voltage, low skew 1-to-9 Differential-to-LVCMOS/LVTTL Zero Delay Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87951I-147 has two selectable clock inputs. The single ended clock input accepts LVCMOS or LVTTL input levels. The CLK1, nCLK1 pair can accept most standard differential input levels. With output frequencies up to 180MHz, the ICS87951I-147 is targeted for high performance clock applications. Along with a fully integrated PLL, the ICS87951I-147 contains frequency configurable outputs and an external feedback input for regenerating clocks with "zero delay".

FEATURES

- Fully integrated PLL

- Nine single ended 3.3V or 2.5V LVCMOS/LVTTL outputs

- Selectable single ended CLK0 or differential CLK1, nCLK1 inputs

- The single ended CLK0 input can accept the following input levels: LVCMOS or LVTTL input levels

- CLK1, nCLK1 supports the following input types: LVDS, LVPECL, LVHSTL, SSTL, HCSL

- Output frequency range: 31.25MHz to 200MHz

- VCO range: 250MHz to 500MHz

- External feedback for "zero delay" clock regeneration

- Cycle-to-cycle jitter, RMS: 7ps (maximum)

- Output skew: 270ps (maximum)

- Full 3.3V operating supply at -40°C to 85°C ambient operating temperature

- Full 2.5V operating supply at 0°C to 85°C ambient operating temperature

- Available in both standard and lead-free RoHS compliant packages

PIN ASSIGNMENT
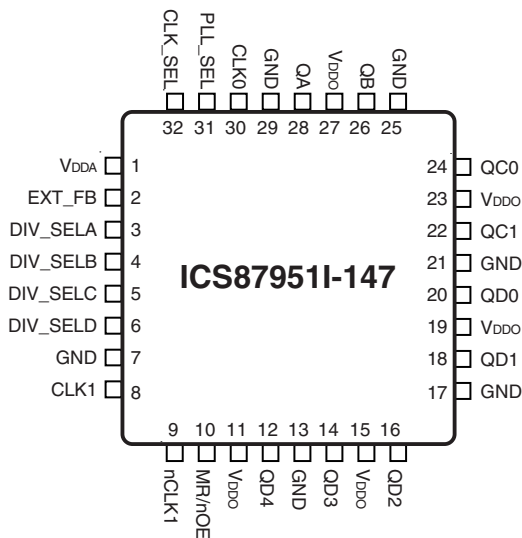
32-Lead LQFP
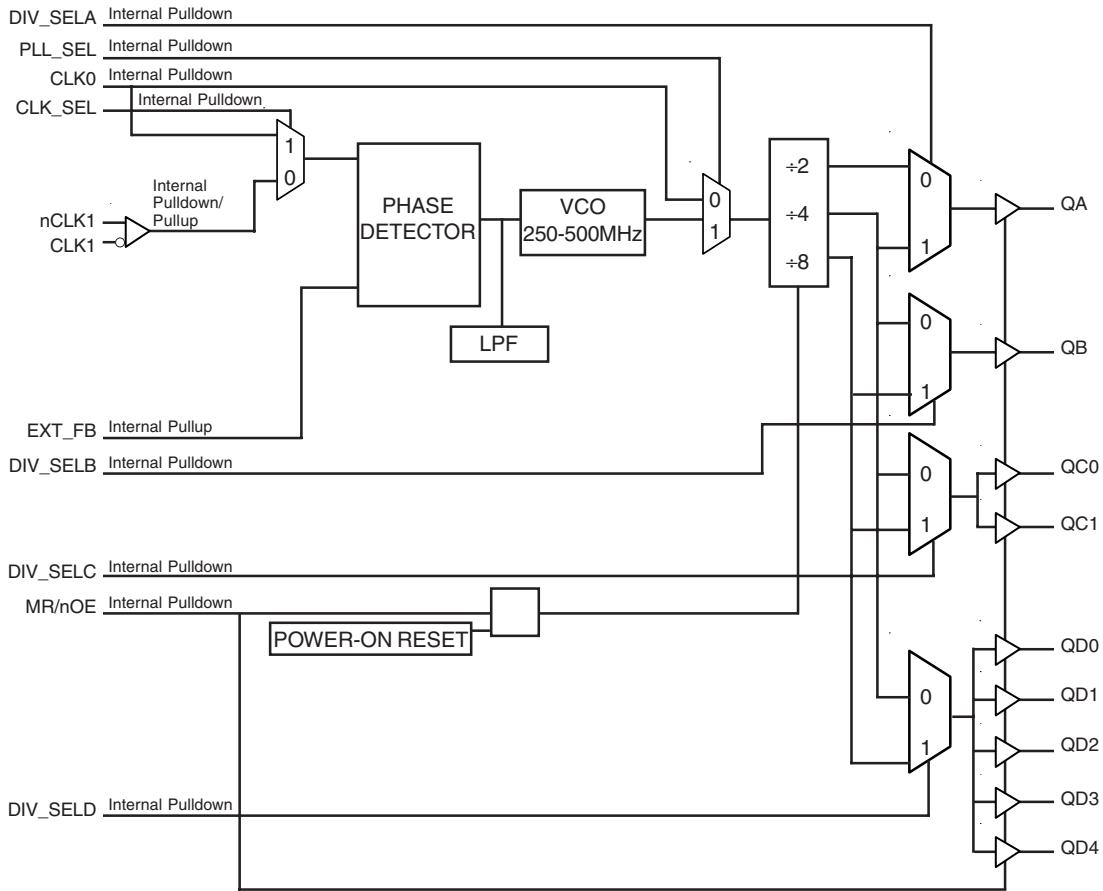7mm x 7mm x 1.4mm package body
Y package
Top View

BLOCK DIAGRAM

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	EXT_FB	Input	Pullup	Feedback input to phase detector for regenerating clocks with "zero delay". LVCMOS / LVTTL interface levels.
3	DIV_SELA	Input	Pulldown	Selects divide value for Bank A output as described in Table 3D. LVCMOS / LVTTL interface levels.
4	DIV_SELB	Input	Pulldown	Selects divide value for Bank B output as described in Table 3D. LVCMOS / LVTTL interface levels.
5	DIV_SELC	Input	Pulldown	Selects divide value for Bank C outputs as described in Table 3D. LVCMOS / LVTTL interface levels.
6	DIV_SELD	Input	Pulldown	Selects divide value for Bank D outputs as described in Table 3D. LVCMOS / LVTTL interface levels.
7, 13, 17, 21, 25, 29	GND	Power		Power supply ground.
8	CLK1	Input	Pullup	Non-inverting differential clock input.
9	nCLK1	Input	Pulldown	Inverting differential clock input.
10	MR/nOE	Input	Pulldown	Active High Master Reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are tri-stated (HiZ). When logic LOW, the internal dividers and outputs are enabled. LVCMOS / LVTTL interface levels.
11, 15, 19, 23, 27	V_{DDO}	Power		Output supply pins.
12, 14, 16, 18, 20	QD4, QD3, QD2, QD1, QD0	Output		Bank D clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
22, 24	QC1, QC0	Output		Bank C clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
26	QB	Output		Bank B clock output. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
28	QA	Output		Bank A clock output. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
30	CLK0	Input	Pulldown	LVCMOS / LVTTL phase detector reference clock input.
31	PLL_SEL	Input	Pulldown	Selects between the PLL and the reference clock as the input to the dividers. When HIGH, selects PLL. When LOW, selects the reference clock. LVCMOS / LVTTL interface levels.
32	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK0. When LOW, selects CLK1, nCLK1. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDA}, V_{DDO} = 3.465V		25		pF
		V_{DDA}, V_{DDO} = 2.625V		15		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

Input	Outputs			
MR/nOE	QA	QB	QC0, QC1	QD0:QD4
1	HiZ	HiZ	HiZ	HiZ
0	Enabled	Enabled	Enabled	Enabled

TABLE 3B. OPERATING MODE FUNCTION TABLE

Input	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

TABLE 3C. PLL INPUT FUNCTION TABLE

Inputs	
CLK_SEL	PLL Input
0	CLK1, nCLK1
1	CLK0

TABLE 3D. PROGRAMMABLE OUTPUT FREQUENCY FUNCTION TABLE

Inputs				Outputs			
DIV_SELA	DIV_SELB	DIV_SELC	DIV_SELD	QA	QB	QCx	QDx
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/4	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/8	VCO/4
0	0	1	1	VCO/2	VCO/4	VCO/8	VCO/8
0	1	0	0	VCO/2	VCO/8	VCO/4	VCO/4
0	1	0	1	VCO/2	VCO/8	VCO/4	VCO/8
0	1	1	0	VCO/2	VCO/8	VCO/8	VCO/4
0	1	1	1	VCO/2	VCO/8	VCO/8	VCO/8
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8
1	0	1	0	VCO/4	VCO/4	VCO/8	VCO/4
1	0	1	1	VCO/4	VCO/4	VCO/8	VCO/8
1	1	0	0	VCO/4	VCO/8	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/8	VCO/4	VCO/8
1	1	1	0	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	1	VCO/4	VCO/8	VCO/8	VCO/8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DDA} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	42.1°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DDA} = V_{DDO} = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DDO}	Power Supply Current	All V_{DD} pins			115	mA
I_{DDA}	Analog Supply Current				20	mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, V_{DDA} = V_{DDO} = 2.5V±5%, T_A = 0°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DDO}	Power Supply Current	All V_{DD} pins			75	mA
I_{DDA}	Analog Supply Current				12	mA

TABLE 4C. DC CHARACTERISTICS, V_{DDA} = V_{DDO} = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA:DIV_SELD, EXT_FB, MR/nOE, PLL_SEL, CLK_SEL		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA:DIV_SELD, EXT_FB, MR/nOE, PLL_SEL, CLK_SEL		-0.3		0.8	V
		CLK0		-0.3		1.3	V
I_{IN}	Input Current					±120	µA
V_{PP}	Peak-to-Peak Input Voltage	CLK1, nCLK1		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2	CLK1, nCLK1		GND + 0.5		V_{DD} - 0.85	V
V_{OH}	Output High Voltage		I_{OH} = -40mA	2.4			V
V_{OL}	Output Low Voltage		I_{OL} = 40mA			0.55	V
			I_{OL} = 12mA			0.3	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK1 and nCLK1 is V_{DDA}+ 0.3V.

TABLE 4D. DC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 2.5V\pm5\%$, $T_A = 0°C$ TO $85°C$

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA:DIV_SELD, EXT_FB, MR/nOE, PLL_SEL, CLK_SEL		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA:DIV_SELD, EXT_FB, MR/nOE, PLL_SEL, CLK_SEL		-0.3		0.8	V
		CLK0		-0.3		0.8	V
I_{IN}	Input Current					±150	µA
V_{PP}	Peak-to-Peak Input Voltage	CLK1, nCLK1		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2	CLK1, nCLK1		GND + 0.5		V_{DD} - 0.85	V
V_{OH}	Output High Voltage	I_{OH} = -15mA		1.8			V
V_{OL}	Output Low Voltage	I_{OL} = 15mA				0.6	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK1 and nCLK1 is V_{DDA}+ 0.3V.

TABLE 5. PLL INPUT REFERENCE CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V\pm5\%$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency				250	MHz

TABLE 6A. AC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V\pm5\%$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	QA ÷2				250	MHz
		Qx ÷4				125	MHz
		QB, QC, QD ÷8				62.5	MHz
f_{VCO}	PLL VCO Lock Range			250		500	MHz
$t(\varnothing)$	Static Phase Offset; NOTE 1,3	CLK0	fREF = 50MHz Feedback = VCO/8	-135		170	ps
		CLK1, nCLK1		-420		-100	ps
$t$sk(o)	Output Skew; NOTE 2, 3					270	ps
$t$jit(cc)	Cycle-to-Cycle Jitter, RMS; NOTE 3	All Outputs @ Same Frequency				7.5	ps
t_{LOCK}	PLL Lock Time; NOTE 3					10	mS
t_R / t_F	Output Rise/Fall Time	20% to 80%		300		800	ps
odc	Output Duty Cycle			46		54	%
t_{PZL}	Output Enable Time					6	ns
t_{PLZ}, t_{PHZ}	Output Disable Time					7	ns

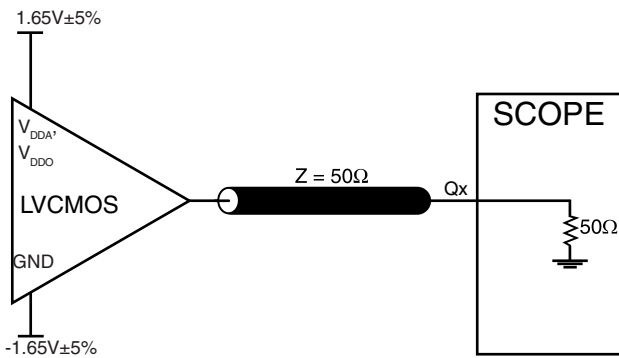All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Defined as the time difference between the input reference clock and the averaged feedback input signal,
when the PLL is locked and the input reference frequency is stable.
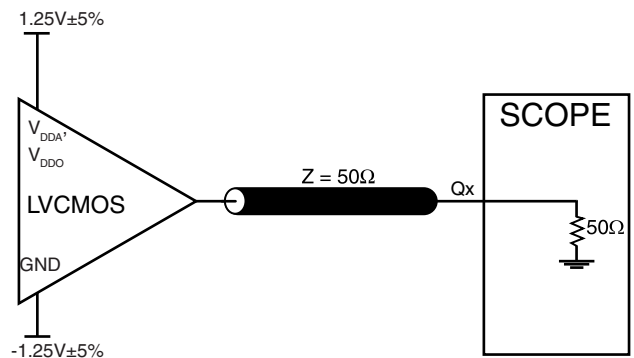NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at V_{DDO}/2.
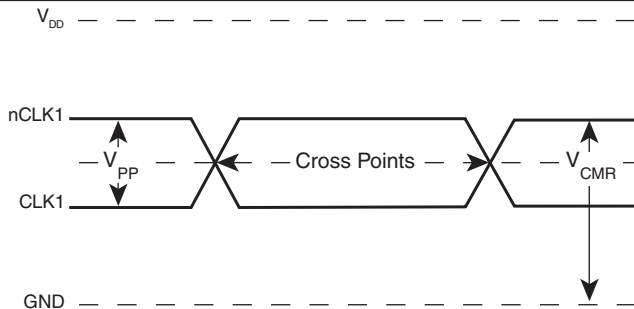NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. AC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 2.5V\pm5\%$, TA = 0°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		QA ÷2			200	MHz
			Qx ÷4			120	MHz
			QB, QC, QD ÷8			60	MHz
f_{VCO}	PLL VCO Lock Range			250		500	MHz
$t(Ø)$	Static Phase Offset; NOTE 1,3	CLK0		-180		220	ps
		CLK1, nCLK1		-500		-165	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3					310	ps
$t_{jit(cc)}$	Cycle-to-Cycle Jitter, RMS; NOTE 3		FVCO ≤ 400MHz, All Outputs @ same frequency			9	ps
t_{LOCK}	PLL Lock Time; NOTE 3					10	mS
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		700	ps
odc	Output Duty Cycle			46		54	%
t_{PZL}	Output Enable Time					6	ns
t_{PLZ}, t_{PHZ}	Output Disable Time					7	ns

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Defined as the time difference between the input reference clock and the averaged feedback input signal,
when the PLL is locked and the input reference frequency is stable.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
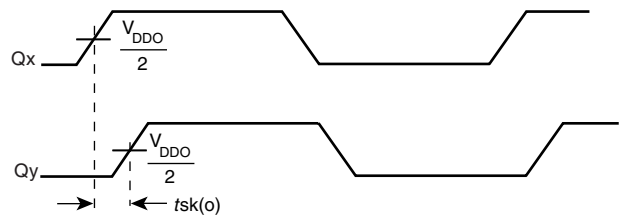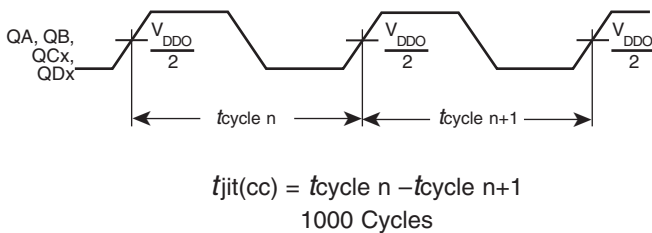
PARAMETER MEASUREMENT INFORMATION

1.65V±5%

V_{DDA}, V_{DDO}

LVCMOS

GND

-1.65V±5%

Z = 50Ω   Qx

SCOPE

50Ω

3.3V OUTPUT LOAD AC TEST CIRCUIT

1.25V±5%

V_{DDA}, V_{DDO}

LVCMOS

GND

-1.25V±5%

Z = 50Ω   Qx

SCOPE

50Ω

2.5V OUTPUT LOAD AC TEST CIRCUIT

V_{DD}

nCLK1

V_{PP} — Cross Points — V_{CMR}

CLK1

GND

DIFFERENTIAL INPUT LEVEL

Qx $\dfrac{V_{DDO}}{2}$

Qy $\dfrac{V_{DDO}}{2}$

$t$sk(o)

OUTPUT SKEW

QA, QB, QCx, QDx $\dfrac{V_{DDO}}{2}$ $\dfrac{V_{DDO}}{2}$ $\dfrac{V_{DDO}}{2}$

$t$cycle n $t$cycle n+1

$$t\text{jit(cc)} = t\text{cycle n} - t\text{cycle n+1}$$
1000 Cycles

CYCLE-TO-CYCLE JITTER

80%   80%

20%   20%

Clock Outputs t_R t_F

OUTPUT RISE/FALL TIME

QAx, QBx, QCx, QDx $\dfrac{V_{DDO}}{2}$

t_{PW}

t_{PERIOD}

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$
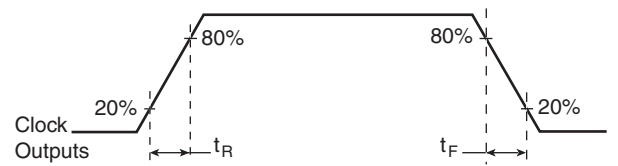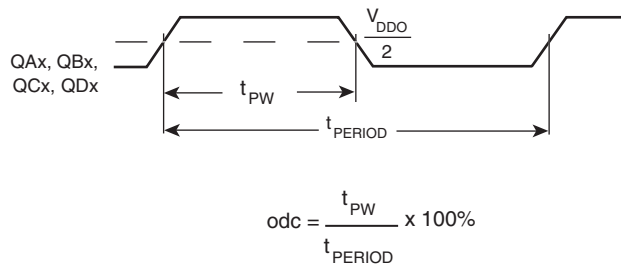
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

nCLK1

CLK0, CLK1

EXT_FB $\dfrac{V_{DD}}{2}$

$t(\varnothing)$

$$t\text{jit}(\varnothing) = \left| t(\varnothing) - t(\varnothing)_{mean} \right| = \text{Phase Jitter}$$

$t(\varnothing)_{mean}$ = Static Phase Offset

(where $t(\varnothing)$ is any random sample, and $t(\varnothing)_{mean}$ is the average of the sampled cycles measured on controlled edges)
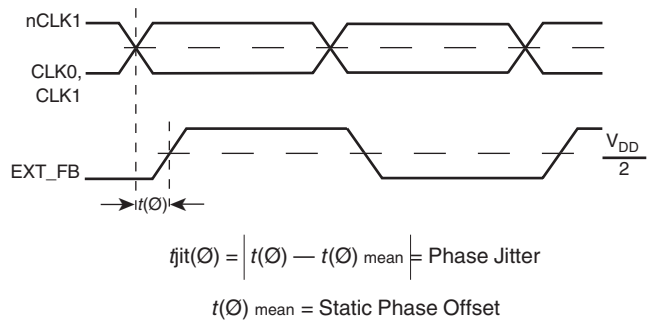
PHASE JITTER AND STATIC PHASE OFFSET

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.
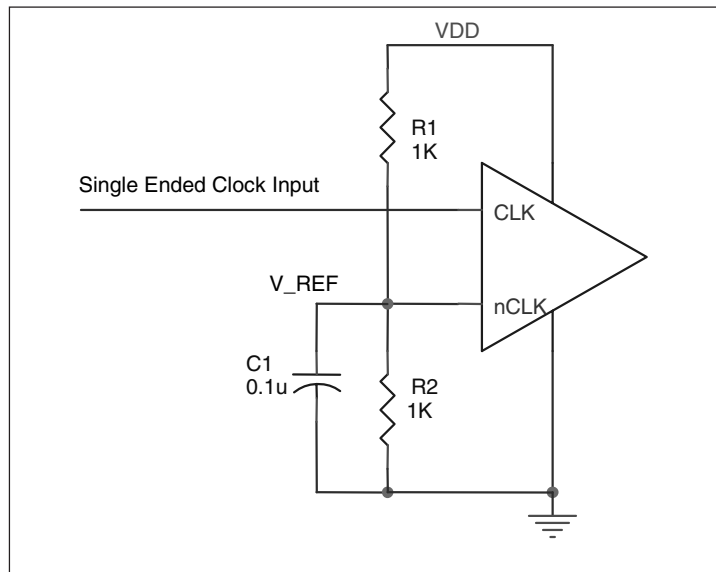
FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87951I-147 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.
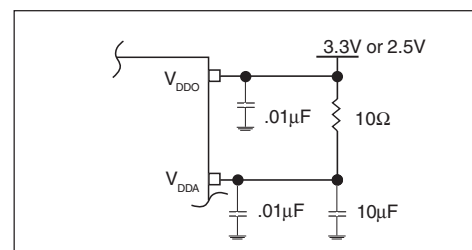
FIGURE 2. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK INPUT:
For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

CLK/nCLK INPUT:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. There should be no trace attached.

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.
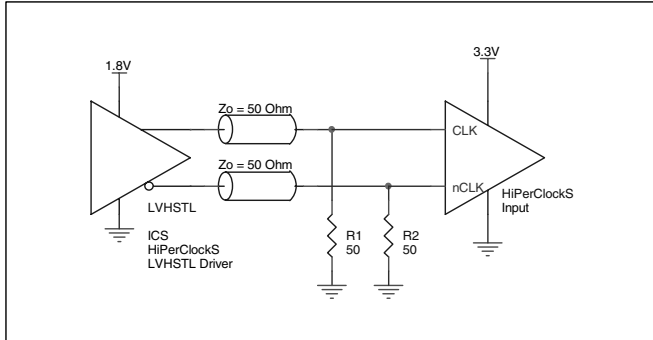

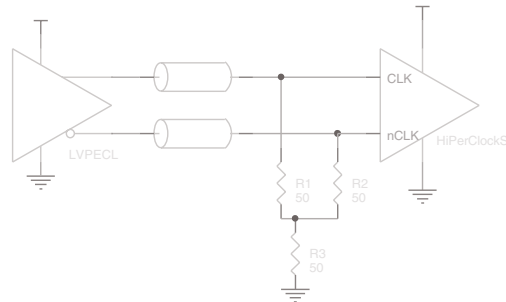**FIGURE 3A. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER**

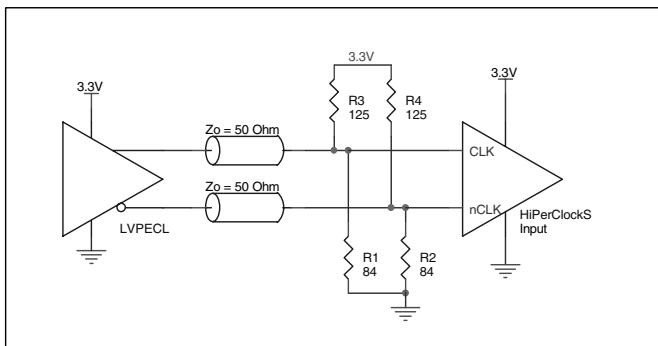**FIGURE 3B. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**

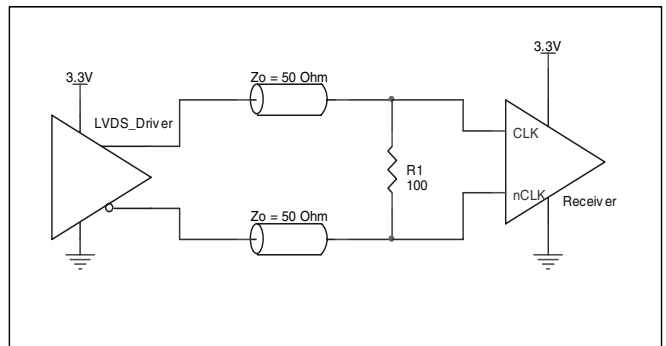**FIGURE 3C. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**

FIGURE 3D. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)

	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87951I-147 is: 2674

Pin compatible with the MPC951

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP
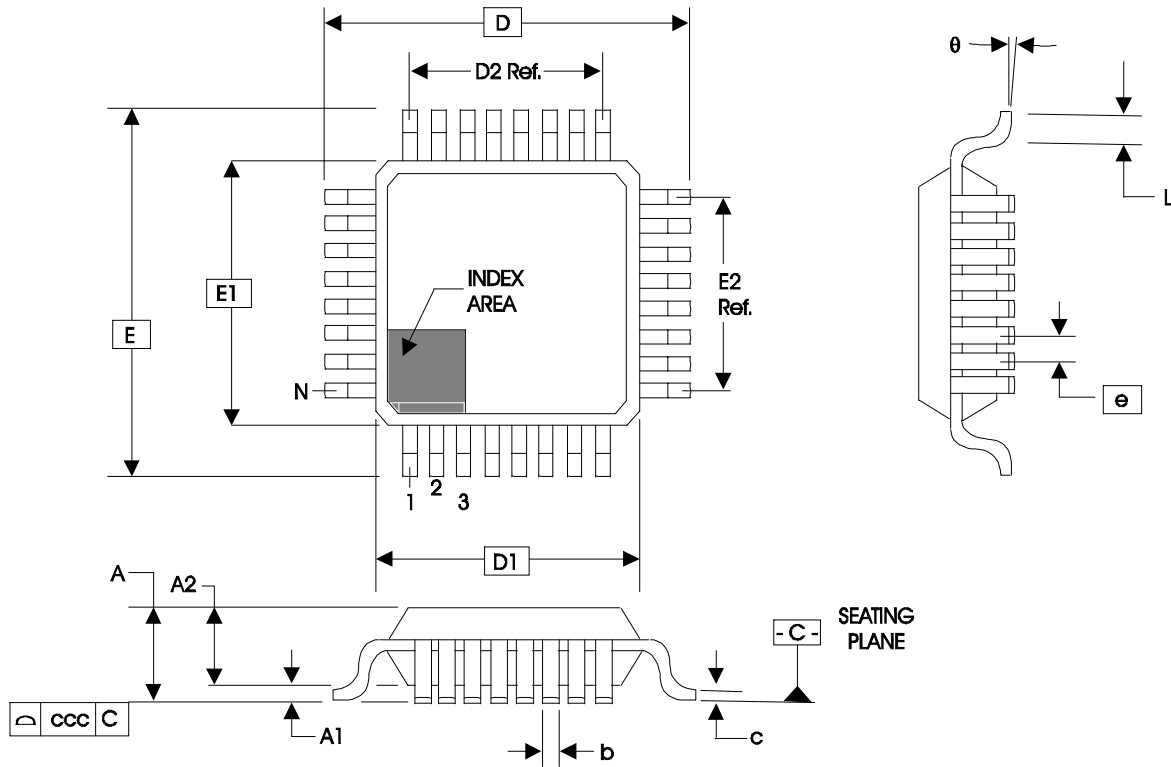
TABLE 8. PACKAGE DIMENSIONS

	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
	BBA		
SYMBOL	**MINIMUM**	**NOMINAL**	**MAXIMUM**
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS87951AYI-147	ICS87951AYI-147	32 Lead LQFP	tray	-40°C to 85°C
ICS87951AYI-147T	ICS87951AYI-147	32 Lead LQFP	1000 tape & reel	-40°C to 85°C
ICS87951AYI-147LF	ICS951AI147L	32 Lead "Lead-Free" LQFP	tray	-40°C to 85°C
ICS87951AYI-147LFT	ICS951AI147L	32 Lead "Lead-Free" LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T9	1 13	Features Section - added Lead-Free bullet. Ordering Information Table - added Lead-Free part number and note.	6/14/05
A	T9	10 13	Added *Recommendations for Unused Input and Output Pins.* Ordering Information Table - corrected standard marking and added lead-free marking.	6/21/06

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