



General Description

The MAX9517/MAX9524 are low-power video amplifiers with integrated reconstruction filters. Specially suited for standard-definition video signals, such as composite and luma, these devices are ideal for a wide range of applications such as cell phones and security/CCTV cameras. Video signals should be DC-coupled into the MAX9517 input and AC-coupled into the MAX9524 input.

The MAX9517/MAX9524 have two single-pole, single-throw (SPST) analog switches that can be used to route stereo audio, video, or digital signals. The reconstruction filter typically has $\pm 1 dB$ passband flatness at 9MHz and 52dB attenuation at 27MHz. The amplifiers have a gain of 2V/V, and the outputs can be DC-coupled to a load of 75 Ω , which is equivalent to two video loads. The outputs can be AC-coupled to a load of 150 Ω , which is equivalent to one video load.

The MAX9517/MAX9524 operate from a 2.7V to 3.6V single supply and are specified over the -40°C to +125°C automotive temperature range. The MAX9517/ MAX9524 are available in a small 12-pin TQFN (3mm x 3mm) package.

Features

- Integrated Reconstruction Filter for Standard-Definition Video
- ♦ 9MHz, ±1dB Passband
- ♦ 52dB Attenuation at 27MHz
- **♦ Dual SPST Switches**
- ♦ Fixed Gain of 2V/V
- ♦ DC- or AC-Coupled Output
- ♦ 2.7V to 3.6V Single-Supply Operation

Applications

Security/CCTV Cameras

Mobile Phones/Cell Phones

Digital Still Cameras (DSC)

Camcorders (DVC)

Portable Media Players (PMP)

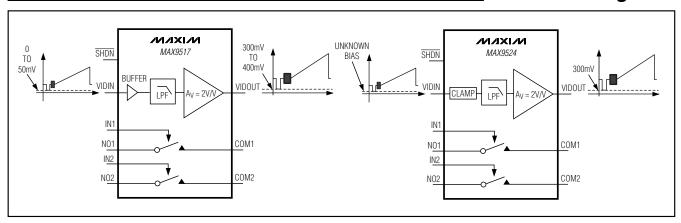
Ordering Information

PART	INPUT TYPE	PIN-PACKAGE	PKG CODE	TOP MARK
MAX9517ATC+	DC BIAS	12 TQFN-EP*	T1233+4	ABF
MAX9524ATC+	AC CLAMP	12 TQFN-EP*	T1233+4	ABE

Note: All devices are specified over the -40°C to +125°C operating temperature range.

Pin Configuration appears at end of data sheet.

Functional Diagrams



MIXIM

Maxim Integrated Products

⁺Denotes a lead-free package.

^{*}EP = Exposed pad.

ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND0.3V to +4V VIDIN to GND0.3V to +4V	Peak Current COM_, NO_ (pulsed at 1ms, 10% duty cycle)±200mA
COM_, NO_ to GND0.3V to (V _{DD} + 0.3V)	Continuous Power Dissipation ($T_A = +70^{\circ}C$)
SHDN, IN_ to GND0.3V to +4V	12-Pin TQFN (derate 14.7mW/°C above +70°C)1177mW
VIDOUT Short-Circuit Duration to VDD, GNDContinuous	Operating Temperature Range40°C to +125°C
Continuous Input Current	Junction Temperature+150°C
VIDIN, IN_, SHDN±20mA	Storage Temperature Range65°C to +150°C
COM_, NO±100mA	Lead Temperature (soldering 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{DD} = \overline{SHDN} = 3.3V, GND = 0V, no load, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)$

PARAMETER	SYMBOL	COND	MIN	TYP	MAX	UNITS	
Supply Voltage Range	V _{DD}	Guaranteed by PSRR		2.7		3.6	V
Cupply Current	la e	MAX9517			3.5	7	m /
Supply Current	IDD	MAX9524	MAX9524			8	mA
Shutdown Supply Current	ISHDN	V _{SHDN} = GND				1	μΑ
VIDEO							
DC BUFFER INPUTS (MAX951	17)						
Input Voltage Range	V _{IN}	Guaranteed by output	$V_{DD} = 2.7V$	0		1.05	V
input voltage riange	VIIN	voltage swing	$V_{DD} = 3V$	0		1.2	v
Input Current	I _{IN}	$V_{IN} = 0V$			3.5	10	μΑ
Input Resistance	R _{IN}				300		kΩ
DC Voltage Gain	A.,	$R_L = 150\Omega$ to GND	$V_{DD} = 2.7V,$ $0 \le V_{IN} \le 1.05V$	1.95	2.00		V/V
	Av	HL = 15022 to GIND	$V_{DD} = 3V,$ $0 \le V_{IN} \le 1.2V$	1.95	2.00		
Output Level		Measured at V_{OUT} , VIDIN = 0.1μF to GND, $R_L = 150\Omega$ to GND		200	300	410	mV
		Measured at output, $V_{DD} = 2.7V$, $0 \le V_{IN} \le 1.05V$, $R_L = 150\Omega$ to $-0.2V$			2.1		
		Measured at output, V 0 ≤ V _{IN} ≤ 1.05V, R _L =		2.1			
Output-Voltage Swing		Measured at output, V $0 \le V_{IN} \le 1.2V$, $R_L = 1.2V$		2.4	V _{P-I}		
		Measured at output, V 0 ≤ V _{IN} ≤ 1.2V, R _L = 15		2.4			
		Measured at output, V 0 ≤ V _{IN} ≤ 1.05V, R _L =		2.1		1	
SYNC-TIP CLAMP INPUT (MA	X9524)						•
Sync-Tip Clamp Level	V _{CLP}	Sync-tip clamp		0.23		0.39	V
Input Voltage Range		V _{DD} = 2.7V to 3.6V				1.05	\/
		$V_{DD} = 3V \text{ to } 3.6V$				1.2	V _{P-P}
Sync Crush		Sync-tip clamp, perce sync pulse (0.3V _{P-P}), clamping current mea			2	%	

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD} = \overline{SHDN} = 3.3V, GND = 0V, no load, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)$

PARAMETER	SYMBOL	CONE	DITIONS		MIN	TYP	MAX	UNITS	
Input Clamping Current		Sync-tip clamp				1	2	μΑ	
Maximum Input Source Resistance			_			300		Ω	
DC Voltage Gain (Note 2)	Ay	$R_{L} = 150\Omega$ to GND	$V_{DD} = 2$ $0 \le V_{IN}$	2.7V, ≤ 1.05V	1.95	2.00	2.04	- V/V	
20 Tollage dall (11010 2)	Αγ	TIL = 10052 to GIND	$V_{DD} = 3$ $0 \le V_{IN}$		1.95	2.00	2.04	V / V	
Output Level		Measured at V_{OUT} , $V_{RL} = 150\Omega$ to GND	'IDIN = 0.	1μF to GND,	0.21	0.30	0.39	V	
		Measured at output, V _{CLP} to (V _{CLP} +1.05)				2.1			
		Measured at output, VCLP to (VCLP +1.05)				2.1			
Output-Voltage Swing		Measured at output, to (V _{CLP} +1.2V), R _L =				2.4		V _{P-P}	
		Measured at output, V_{DD} = 3V, V_{IN} = V_{CLP} to (V_{CLP} +1.2V), R_L = 150 Ω to V_{DD} /2			2.4				
		Measured at output, V_{DD} = 3.135V, V_{IN} = V_{CLP} to $(V_{CLP}$ +1.05V), R_L = 75 Ω to -0.2V				2.1			
Short to GND (sourcing)				140		mΛ			
Output Short-Circuit Current		Short to V _{CC} (sinking)				70		mA	
Output Resistance	Rout	$V_{OUT} = 1.5V$, $-10mA \le I_{LOAD} \le +10mA$				0.2		Ω	
Output Leakage Current		SHDN = GND				1	μΑ		
Power-Supply Rejection Ratio		$2.7V \le V_{DD} \le 3.6V$			48			dB	
		±1dB passband flatn	ess			9		MHz	
Standard-Definition		\/ O\/ #of		f = 5.5MHz		+0.15			
Reconstruction Filter		V _{VIDOUT} = 2V _{P-P} , referred frequency is 100kHz		f = 10MHz		-3		dB	
		Troqueriey to rectain		f = 27MHz		-52			
Differential Gain	DG	5-step modulated staircase of 129mV step size and 286mV _{P-P} subcarrier amplitude; f = 4.43MHz			1		%		
Differential Phase	DP	5-step modulated staircase of 129mV step size and 286mV _{P-P} subcarrier amplitude; f = 4.43MHz				0.4		Degrees	
2T Pulse-to-Bar K Rating		Bar time is 18µs, the beginning 2.5% and the ending 2.5% of the bar time are ignored, 2T = 200ns				0.6		K%	
2T Pulse Response		2T = 200ns				0.2		K%	
2T Bar Response		Bar time is 18µs, the the ending 2.5% of the ignored, 2T = 200ns				0.2		K%	

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD} = \overline{SHDN} = 3.3V, GND = 0V, no load, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25 °C.) (Note 1)$

PARAMETER	SYMBOL	CONDITIONS			TYP	MAX	UNITS
Nonlinearity		5-step staircase, f =		0.5		%	
Group Delay Distortion		100kHz ≤ f ≤ 5.5MHz		12		ns	
Peak Signal to RMS Noise		100kHz ≤ f ≤ 5.5MHz			71		dB
Power-Supply Rejection Ratio		f = 1MHz, 100mV _{P-P}			29		dB
Output Impedance		f = 5.5MHz			4.8		Ω
All-Hostile Crosstalk		f = 4.43MHz			-64		dB
ANALOG SWITCHES	•						
Analog Signal Range	V _{COM_} , V _{NO_}			0		V _{DD}	V
On-Resistance (Note 3)	Ron	V _{DD} = 2.7V, I _{COM} =	10mA, V _{NO} _ = 1.5V		1.7	5.0	Ω
On-Resistance Match Between Channels (Notes 3, 4)	ΔR _{ON}	V _{DD} = 2.7V, I _{COM} _ =	10mA, V _{NO} _ = 1.5V			0.4	Ω
On-Resistance Flatness (Note 5)	R _{FLAT} (ON)	V _{DD} = 2.7V, I _{COM} = 1.5V, 2.0V	$10\text{mA}, V_{\text{NO}} = 1.0V,$		0.5	1.5	Ω
NO_ Off-Leakage Current (Note 3)	I _{NO_(OFF)}	V _{DD} = 3.6V, V _{COM} = V _{NO} = 3.3V, 0.3V	= 0.3V, 3.3V;	-2		+2	nA
COM_ On-Leakage Current (Note 3)	I _{COM_(ON)}	V _{DD} = 3.6V, V _{COM} = V _{NO} = 0.3V, 3.3V, o		-2.5		+2.5	nA
Turn-On Time	ton	V _{NO} _ = 1.5V; R _L = 30 V _{IH} = 1.5V, V _{IL} = 0V			100	ns	
Turn-Off Time	toff	V _{NO} _ = 1.5V; R _L = 30 V _{IH} = 1.5V, V _{IL} = 0V	00Ω, C _L = 35pF,			100	ns
Skew (Note 3)	tskew	$R_S = 39\Omega$, $C_L = 50pF$	=			2	ns
Charge Injection	Q	V _{GEN} = 1.5V, R _{GEN} =	= 0Ω, C _L = 1nF		10		рС
Off-Isolation	V _{ISO}	f = 10MHz; V _{NO} _ = 1 C _L = 5pF			-55		dB
On Channal 2dD Dandwidth	DW	f = 1MHz; V _{NO} _ = 1V _F		-80		N 41 1	
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, R _L =	·		300		MHz
Total Harmonic Distortion	THD	V _{COM} = 2V _{P-P} , R _L =	: 60022		0.03		%
NO_ Off-Capacitance	C _{NO_} (OFF)	f = 1MHz			20		pF
Switch On-Capacitance	C _(ON)	f = 1MHz			50		pF
Switch-to-Switch	V _{CT}	$ \begin{split} f &= 10 MHz; V_{NO_} = 1 V_{P\text{-}P}, R_L = 50 \Omega, \\ C_L &= 5 p F \end{split} $			-80		dB
omon to omiton	VC1	$f = 1MHz; V_{NO} = 1V$ $C_L = 5pF$	P_{P-P} , $R_L = 50\Omega$,		-110		QD
NO to VIDOLIT		Video circuit is on,	f = 10MHz; V _{NO} _ = 1V _{P-P}		-55		dD.
NOto-VIDOUT		switches are open	f = 1MHz; V _{NO} _ = 1V _{P-P}		-80		dB

__ /N/XI/N

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD} = \overline{SHDN} = 3.3V, GND = 0V, no load, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CROSSTALK	•					
VIDOUT-to-NO_		Video circuit is on, f = $20kHz$, VIDOUT = $2V_{P-P}$, $R_L = 50\Omega$, $C_L = 5pF$		90		dB
VIDIN-to-COM		Video circuit is shutdown, f = 20kHz, $0.25V_{P-P}$ at VIDIN, $R_L = 600\Omega$		100		dB
VIDOUT-to-COM		Video circuit is on, f = $20kHz$, VIDOUT = $2V_{P-P}$, $R_L = 50\Omega$, $C_L = 5pF$		90		dB
LOGIC SIGNAL (IN1 AND IN	2)					
Logic-Low Threshold	VIL				0.5	V
Logic-High Threshold	VIH		1.4			V
Logic-Input Current	I _{IN}				10	μΑ
LOGIC SIGNAL (SHDN)						
Logic-Low Threshold	VIL				0.3 x V _{DD}	V
Logic-High Threshold	VIH		0.7 x V _{DD}			V
Logic-Input Current	I _{IN}				10	μΑ

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

Note 2: Voltage gain (Ay) is a two-point measurement in which the output-voltage swing is divided by the input-voltage swing.

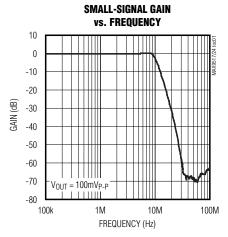
Note 3: Guaranteed by design.

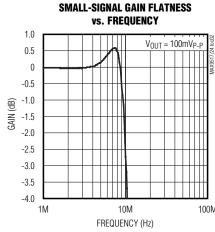
Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

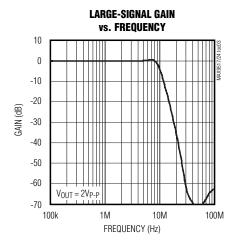
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Typical Operating Characteristics

 $(V_{DD} = \overline{SHDN} = 3.3V)$. Video outputs have $R_L = 150\Omega$ connected to GND. $T_A = +25^{\circ}C$, unless otherwise noted.)

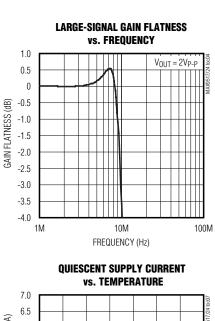


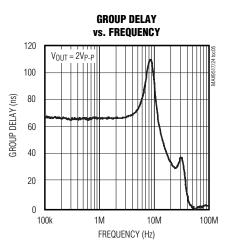


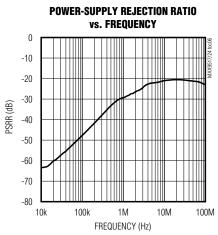


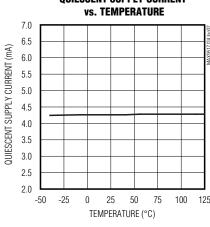
Typical Operating Characteristics (continued)

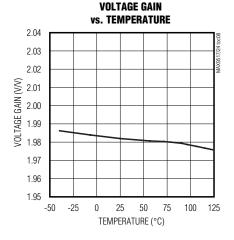
 $(V_{DD} = \overline{SHDN} = 3.3V)$. Video outputs have $R_L = 150\Omega$ connected to GND. $T_A = +25^{\circ}C$, unless otherwise noted.)

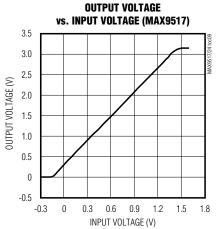


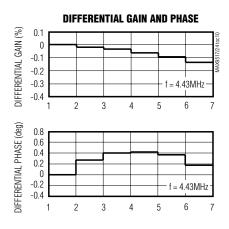


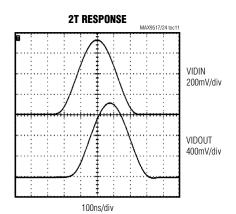






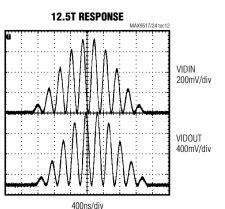


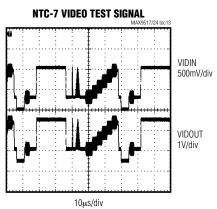


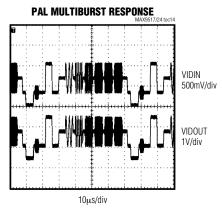


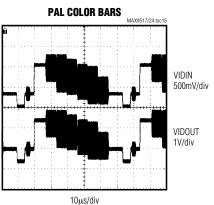
_Typical Operating Characteristics (continued)

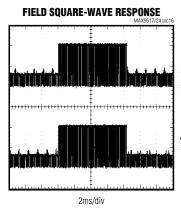
 $(V_{DD} = \overline{SHDN} = 3.3V)$. Video outputs have $R_L = 150\Omega$ connected to GND. $T_A = +25$ °C, unless otherwise noted.)

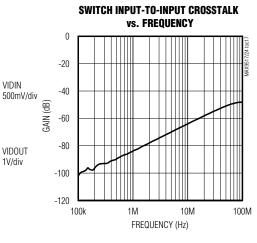


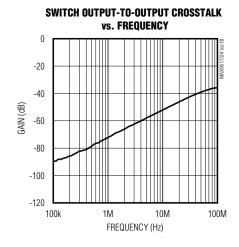


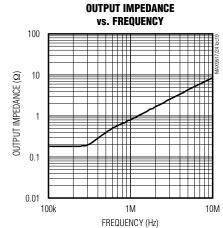






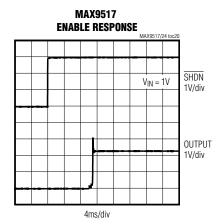




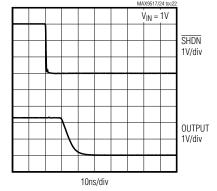


Typical Operating Characteristics (continued)

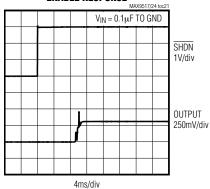
 $(V_{DD} = \overline{SHDN} = 3.3V. \text{ Video outputs have } R_L = 150\Omega \text{ connected to GND. } T_A = +25^{\circ}C, \text{ unless otherwise noted.})$



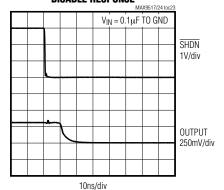




MAX9524 ENABLE RESPONSE



MAX9524 DISABLE RESPONSE



Pin Description

PIN	NAME	FUNCTION
1	N.C.	No Connection. Not internally connected.
2	COM1	Analog Switch 1 Common Terminal
3	COM2	Analog Switch 2 Common Terminal
4	VIDOUT	Video Output
5	GND	Ground
6	VIDIN	Video Input
7	NO2	Analog Switch 2 Normally Open Terminal
8	NO1	Analog Switch 1 Normally Open Terminal
9	SHDN	Active-Low Shutdown Input. Connect to GND to place device in shutdown.
10	IN1	Analog Switch 1 Digital Control Input
11	IN2	Analog Switch 2 Digital Control Input
12	V_{DD}	Positive Power Supply. Bypass to GND with a 0.1µF capacitor.
_	EP	Exposed Paddle. Connect EP to GND. EP is also internally connected to GND.

Detailed Description

The MAX9517/MAX9524 consist of a lowpass filter and an output amplifier capable of driving a standard 150 Ω video load to ground. The MAX9517 has an input buffer and the MAX9524 has an input sync-tip clamp. The MAX9517/MAX9524 both have two SPST analog switches that can be used to route audio, video, or digital signals. The output amplifiers provide a fixed gain of 2V/V.

The MAX9517/MAX9524 filter and amplify the video DAC output. External video signals, in which the DC bias is usually not known, can be AC-coupled to the MAX9524.

Input with DC Buffer (MAX9517)

The input of the MAX9517 can be directly connected to the video source if the signal is approximately between ground and 1V. This specification is commonly found at the output of most video DACs.

DC-coupling requires that the input signals are ground referenced so that the sync tip of composite or luma signals is within 50mV of ground.

Input with Sync-Tip Clamp (MAX9524)

When the bias of the incoming video signal is either unknown or not between ground and 1V (such as an external video source), use the MAX9524 to connect the video source through a $0.1\mu F$ capacitor.

The VIDIN input of the MAX9524 can only handle signals with a sync pulse, such as composite video and luma. An internal sync-tip clamp sets the internal DC level of the video signal.

Video Filter

The filter passband (±1dB) is typically 9MHz to make the device suitable for standard-definition video signals from all sources (including broadcast video and DVD). Broadcast video signals are channel limited: NTSC signals have 4.2MHz bandwidth, and PAL signals have 5MHz bandwidth. Video signals from a DVD player, however, are not channel limited; therefore, the bandwidth of DVD video signals can approach the Nyquist limit of 6.75MHz (recommendation ITU-R BT.601-5 specifies 13.5MHz as the sampling rate for standard-definition video). Therefore, the maximum bandwidth of the signal is 6.75MHz. To ease the filtering requirements, most modern video systems oversample by two times, clocking the video current DAC at 27MHz.

Outputs

The video output amplifiers can both source and sink load current, allowing output loads to be DC- or AC-coupled. The amplifier output stage needs around 300mV of headroom from either supply rail. The parts have an internal level shift circuit that positions the sync tip at approximately 300mV at the output.

If the supply voltage is greater than 3.135V (5% below a 3.3V supply), each amplifier can drive two DC-coupled video loads to ground. If the supply is less than 3.135V, each amplifier can drive only one DC-coupled or AC-coupled video load.

Shutdown

The MAX9517/MAX9524 draw less than $1\mu A$ supply current when \overline{SHDN} is low. In shutdown, the amplifier output becomes high impedance.

SPST Analog Switches

Table 1. Logic for Analog Switches

IN_	SWITCH STATE
0	OFF
1	ON

_Applications Information

Reducing Power Consumption in the Video DACs

The MAX9517/MAX9524 have high-impedance input buffers that can work with source resistances as high as 300Ω . To reduce power dissipation in the video DACs, the DAC output resistor can be scaled up in value. The reference resistor that sets the reference current inside the video DACs must also be similarly scaled up. For instance, if the output resistor is 37.5Ω , the DAC must source 26.7mA when the output is 1V. If the output resistor is increased to 300Ω , the DAC only needs to source 3.33mA when the output is 1V.

There is parasitic capacitance from the DAC output to ground. That capacitance in parallel with the DAC output resistor forms a pole that can potentially roll off the frequency response of the video signal. For example, 300Ω in parallel with 50pF creates a pole at 10.6 MHz. To minimize this capacitance, reduce the area of the signal trace attached to the DAC output as much as possible, and place the MAX9517/MAX9524 as close as possible to the video DAC outputs.

AC-Coupling the Outputs

The outputs can be AC-coupled because the output stage can source and sink current as shown in Figure 1. Coupling capacitors should be $220\mu F$ or greater to keep the highpass filter formed by the 150Ω equivalent resistance of the video transmission line to a corner frequency of 4.8Hz or below. The frame rate of PAL systems is 25Hz, and the frame rate of NTSC systems is 30Hz. The corner frequency should be well below the frame rate.

Changing Between Video Output and Microphone Input on a Single Connector

A single pole on a mobile phone jack can be used for transmitting a video signal to a television or receiving the signal from the microphone of a headset. Figure 2 shows how the MAX9517 can transmit a video signal. Figure 3 shows how the MAX9517 can receive and pass on the signal from a microphone.

Switching Between Video and Digital Signals

The dual SPST analog switches and the high-impedance output of the video amplifier enable video transmission, digital transmission, and digital reception all on a single pole of a connector. Figures 4, 5, and 6 show the different configurations of the MAX9517.

Selecting Between Two Video Sources

The analog switches can multiplex between two video sources. For example, a mobile phone might have an application processor with an integrated video encoder and a mobile graphics processor with an integrated video encoder, each creating a composite video signal that is between 0 and 1V. Figure 7 shows this application

in which the MAX9517 chooses between two internal video sources. The two analog switches can be used as a 2:1 multiplexer to select which video DAC output is actually filtered, amplified, and then driven out to the connector. Close switch 1 to select the video from the application processor. Close switch 2 to select the video from the mobile graphics processor.

Figure 8 shows the application in which the MAX9524 chooses between two external video sources with unknown DC bias.

Y/C Mixer with Chroma Mute

If the video application processor has two current output digital-to-analog converters (DACs) for luma (Y) and chroma (C), respectively, then the signals can be mixed together to create a composite video signal by summing the currents into a single resistor, as shown in Figure 9. The composite video signal should be AC-coupled into the MAX9524 because the composite video signal has a positive DC level shift. The sync-tip clamp of the MAX9524 will re-establish the DC bias level of the signal inside the chip.

The chroma current is connected to essentially a single-pole, double-throw (SPDT) switch. In one position, the switch routes the chroma current into the resistor. In the other position, the switch routes the chroma current into ground. For the Y/C mixer to work properly, the chroma current must be routed through analog switch 1 into the resistor.

If the chroma signal needs to be muted, then the chroma current is shunted to ground through analog switch 2. Analog switch 1 stays open. See Figure 10.

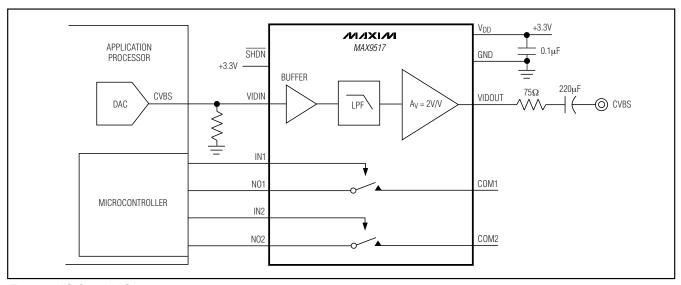


Figure 1. AC-Coupled Outputs

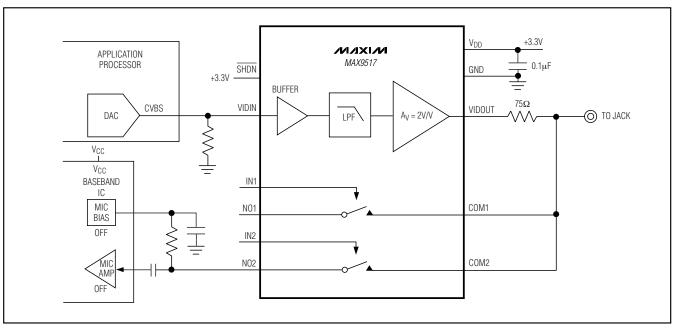


Figure 2. Video Output Configuration

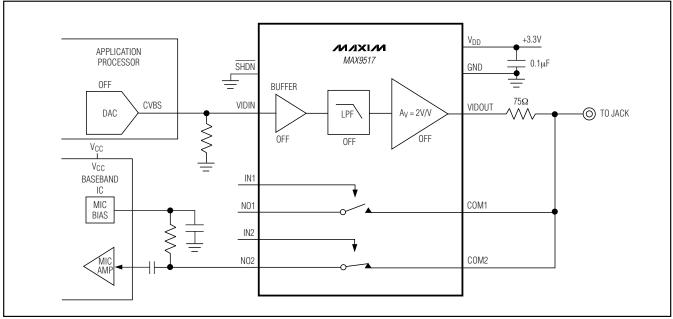


Figure 3. Microphone Input Configuration

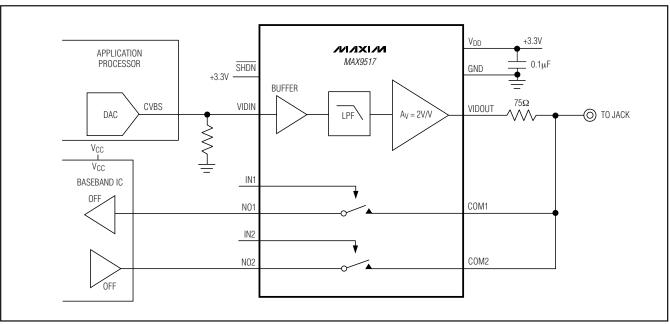


Figure 4. Video Output Configuration

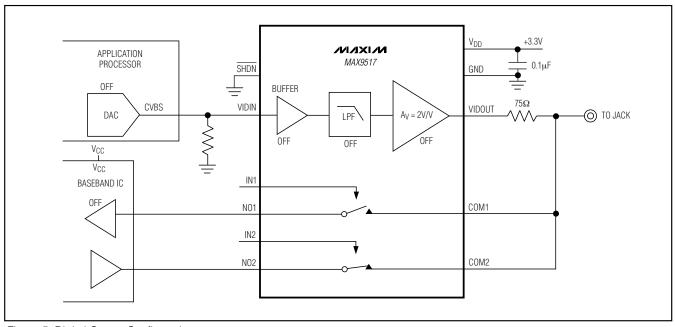


Figure 5. Digital Output Configuration

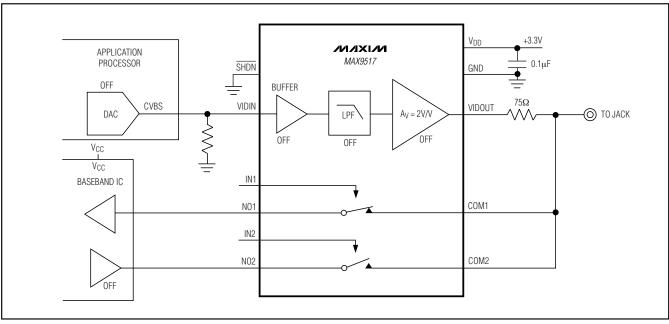


Figure 6. Digital Input Configuration

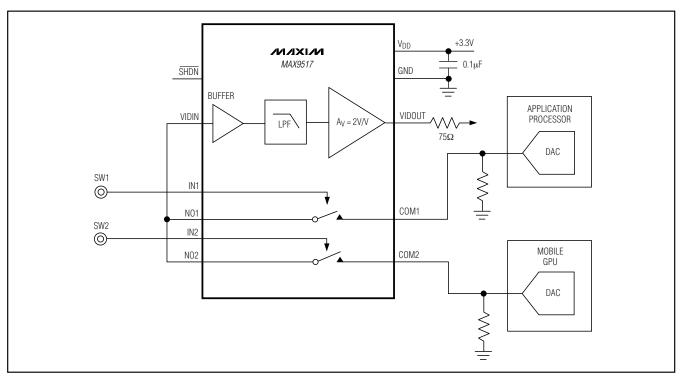


Figure 7. Selecting Between Two Internal Video Sources

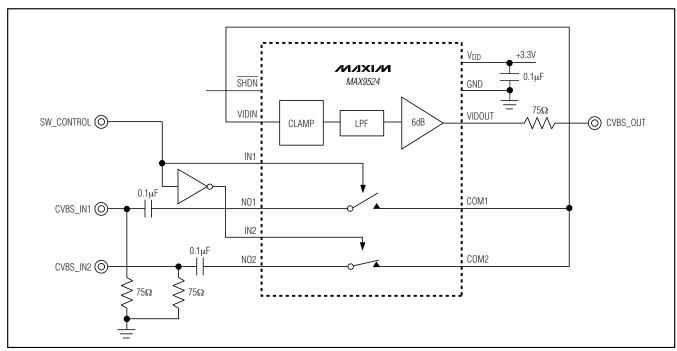


Figure 8. Selecting Between Two External Video Sources

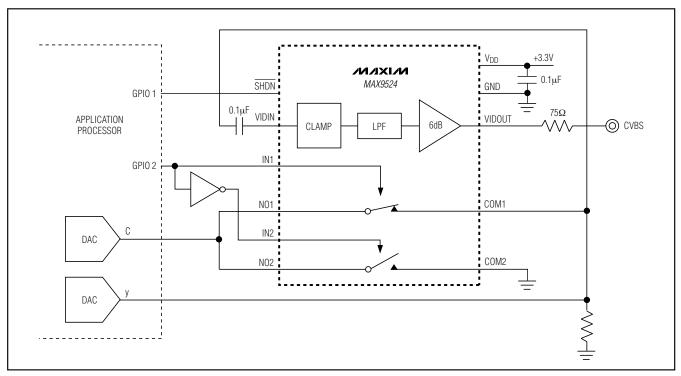


Figure 9. Luma and Chroma Mixer Circuit (Chroma Current Routed into Resistor)

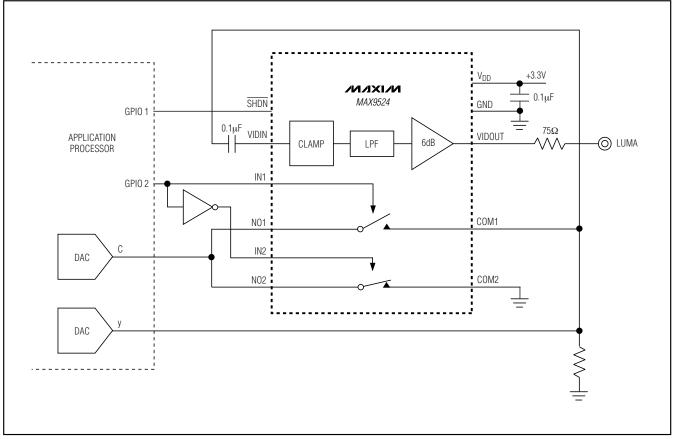


Figure 10. Luma and Chroma Mixer Circuit with Chroma Muted. Chroma Current is Shunted into Ground Through Analog Switch 2.

Anti-Alias Filter

The MAX9524 can also provide anti-alias filtering with buffer before an analog-to-digital converter (ADC), which would be present in an NTSC/PAL video decoder, for example. Figure 11 shows an example application circuit for MAX9524. An external composite video signal is applied to IN, which is terminated with 75 Ω to ground. The signal is AC-coupled to VIDIN because the DC level of an external video signal is usually not well specified.

Power-Supply Bypassing and Ground

The MAX9517/MAX9524 operate from a single-supply voltage down to 2.7V, allowing for low-power operation. Bypass V_{DD} to GND with a 0.1µF capacitor. Place all external components as close as possible to the device.

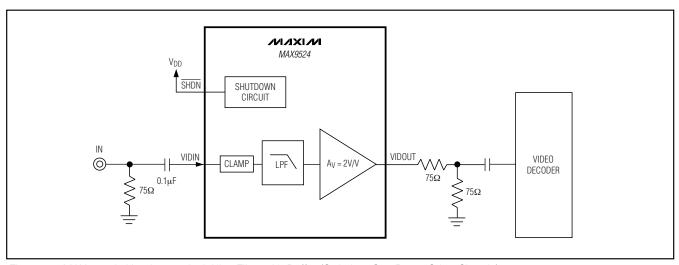


Figure 11. MAX9524 is Used as an Anti-Alias Filter with Buffer (Switches Can Route Other Signals)

Switch Test Circuits/Timing Diagrams

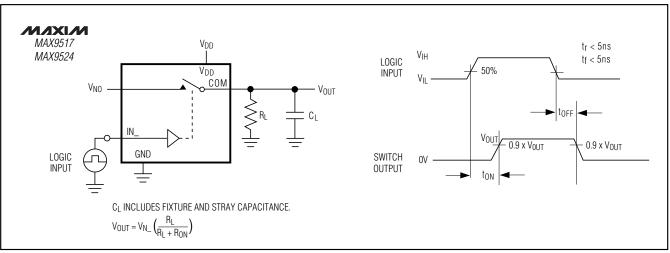


Figure 12. Switching Time

16 _______ **/V**/X\/V

Switch Test Circuits/Timing Diagrams (continued)

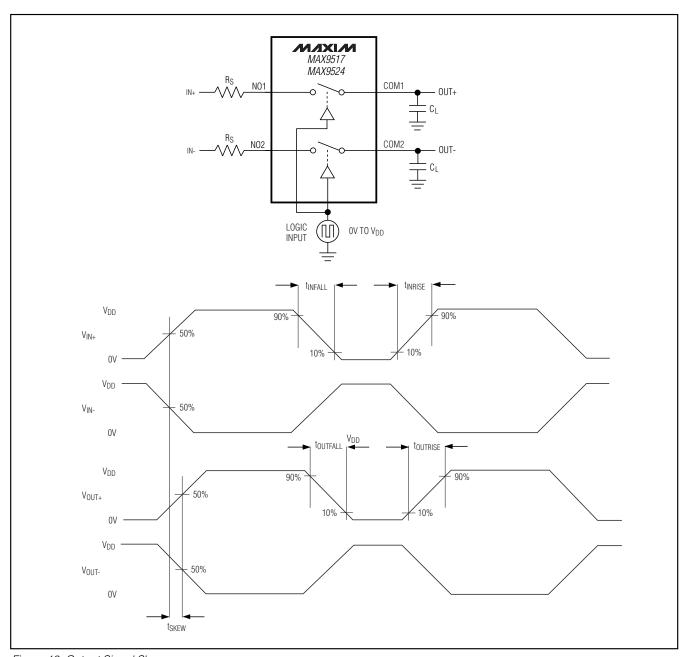


Figure 13. Output Signal Skew

Switch Test Circuits/Timing Diagrams (continued)

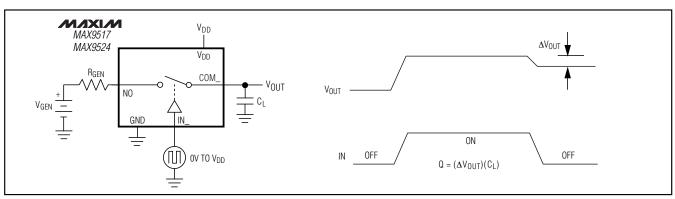


Figure 14. Charge Injection

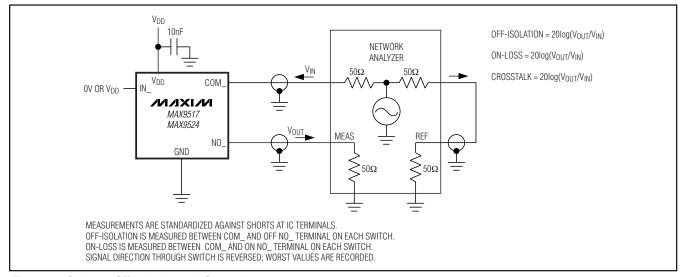


Figure 15. On-Loss, Off-Isolation, and Crosstalk

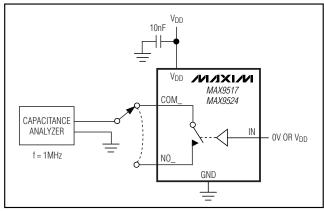
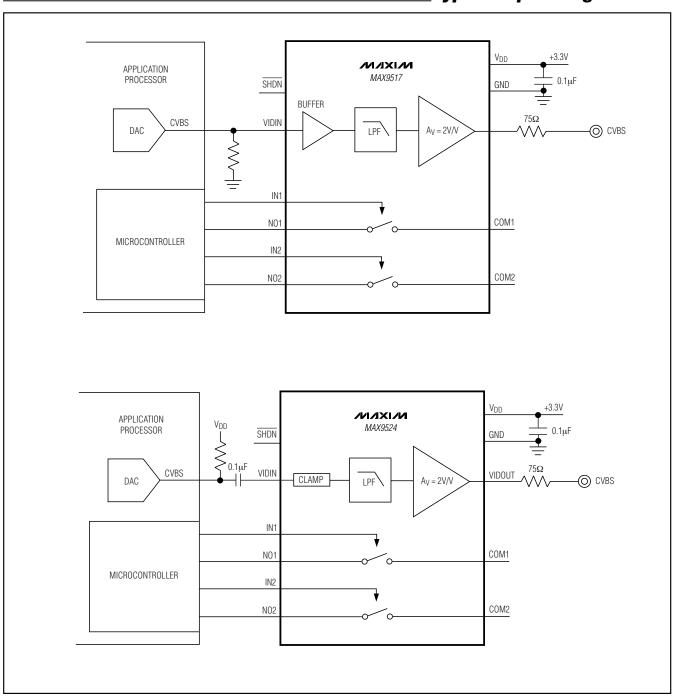


Figure 16. Channel Off-/On-Capacitance

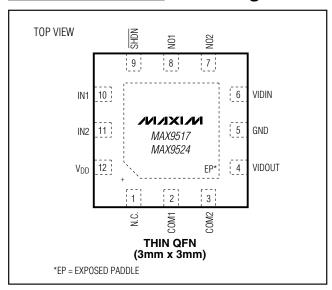
Typical Operating Circuits



Pin Configuration

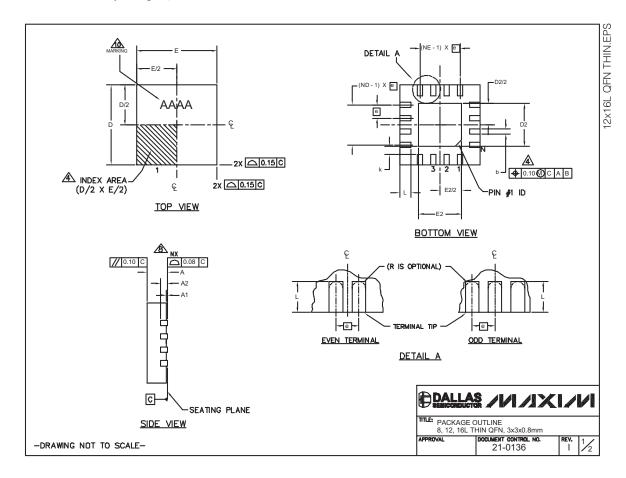
_Chip Information

PROCESS: BiCMOS



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
А	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
Е	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
е	0.	.65 BS0	Э.	0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N		8		12			16		
ND		2		3			4		
NE	2		3			4			
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS										
PKG.		D2			E2		PIN ID	JEDEC		
CODES	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	PINID	JEDEC		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC		
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1		
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1		
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1		
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2		
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2		
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2		
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2		
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2		

- 1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994
- 2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- 4 THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
- ⚠ DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
- 6 ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- ▲ COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
- DRAWING CONFORMS TO JEDEC MOZZU REVISION C.
 MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- 11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY 12. WARPAGE NOT TO EXCEED 0.10mm.

PACKAGE OUTLINE

8. 12. 16L THIN QFN. 3x3x0.8mm

DOCUMENT CONTROL NO 21-0136

Τ

-DRAWING NOT TO SCALE-

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.