FEDL7732-01-10
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OKI Semiconductor

MSM7732-01

Audio CODEC

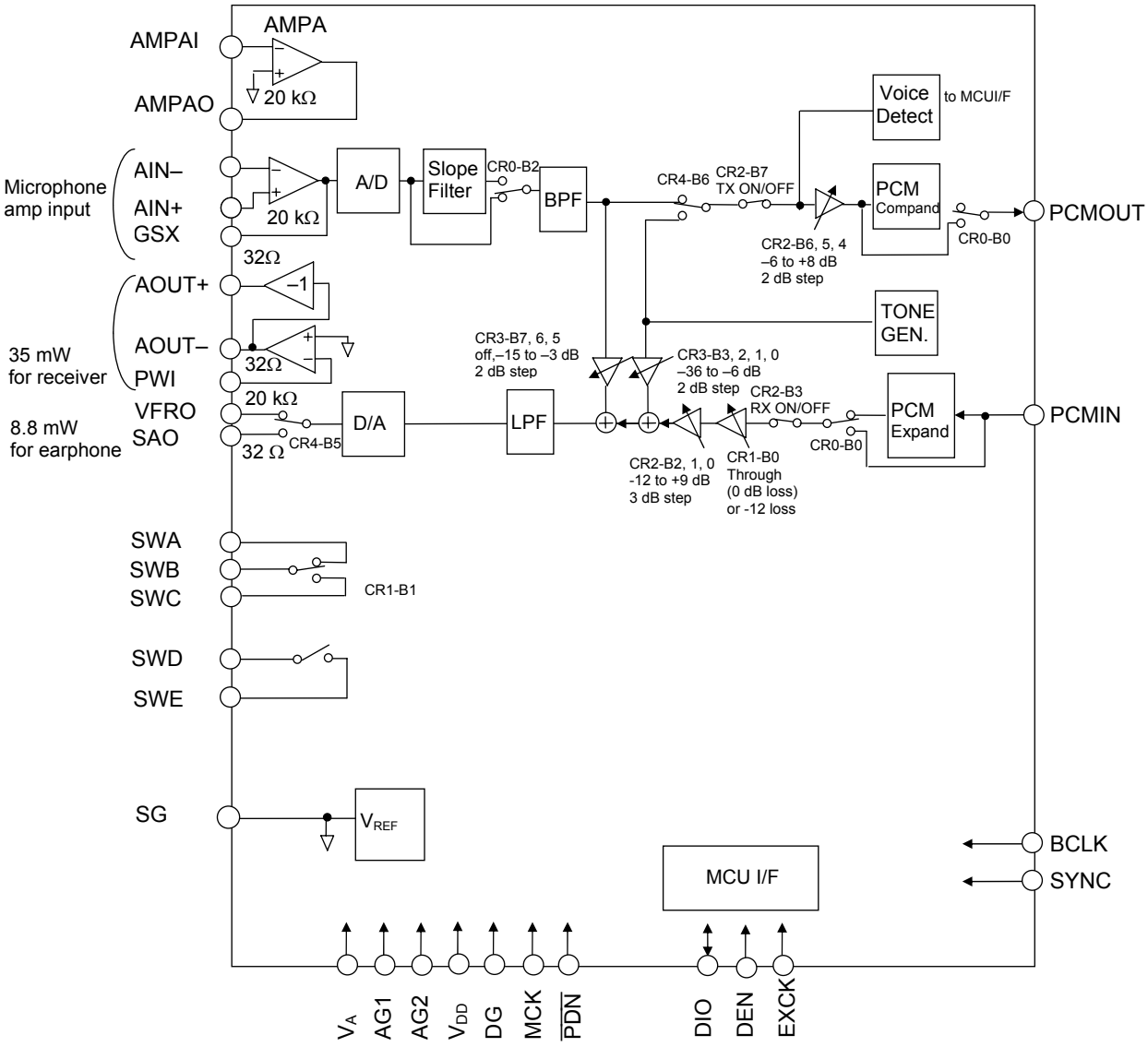
GENERAL DESCRIPTION

The MSM7732 is a single-channel full duplex CODEC CMOS IC which performs mutual transcoding between the analog voice band signals and 64 kbps PCM serial data.
This device performs such functions as DTMF tone and several types of tone generation, transmit/receive data mute and gain control, and side tone path.

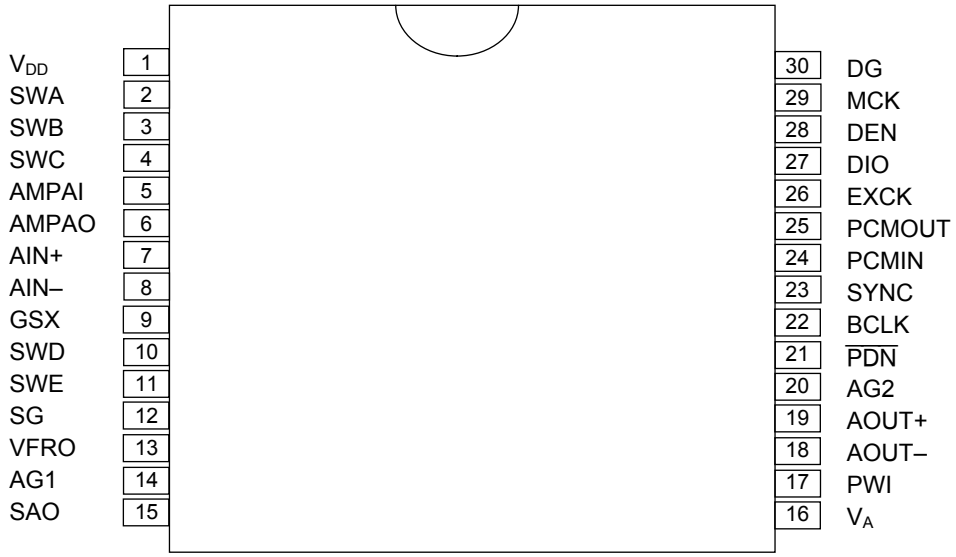
FEATURES

· Single 3 V power supply operation V_{DD}: 2.4 V to 3.3 V
· PCM interface data format : μ-law/A-law/linear (2's complement) selectable
· PCM interface timing : long frame synchronous timing/short frame synchronous timing
· Full-duplex single channel operation
· Serial PCM transmission data rate: 64 kbps to 2048 kbps
· Low power consumption
  Operating mode: 15 mW typ. (V_{DD} = 3.0 V)
  Power-down mode: 3 μW typ. (V_{DD} = 3.0 V)
· Master clock frequency: 2.048 MHz
· Analog output stage
  35 mW drive for receiver speaker (differential drive of 32 Ω)--Gain adjustable
  66 mW drive for receiver speaker (differential drive of 30 Ω)--Gain adjustable
  6.6 mW drive for earphone speaker (single drive of 32 Ω) --Gain adjustable
· Transmit/receive mute, transmit/receive programmable gain control
· Side tone path with programmable attenuation (8-step adjustment level)
· Built-in DTMF tone generator
· Built-in various ringing/function tone generator
· Built-in various ring back tone generator
· Serial MCU interface control: 3 bit
· Built-in transmit voice signal detector
· Built-in op amps and analog switches for various analog interface
· Package options :
  30-pin plastic SSOP (SSOP30-P-56-0.65-K) (MSM7732-01 MB)
  48-pin plastic TQFP (TQFP48-P-0707-0.50-K) (MSM7732-01 TB)
  48-pin plastic LGA (P-TFLGA48-0707-0.8) (MSM7732-01 LB)
  48-pin plastic BGA (P-LFBGA48-0707-0.8) (MSM7732-01 LA)

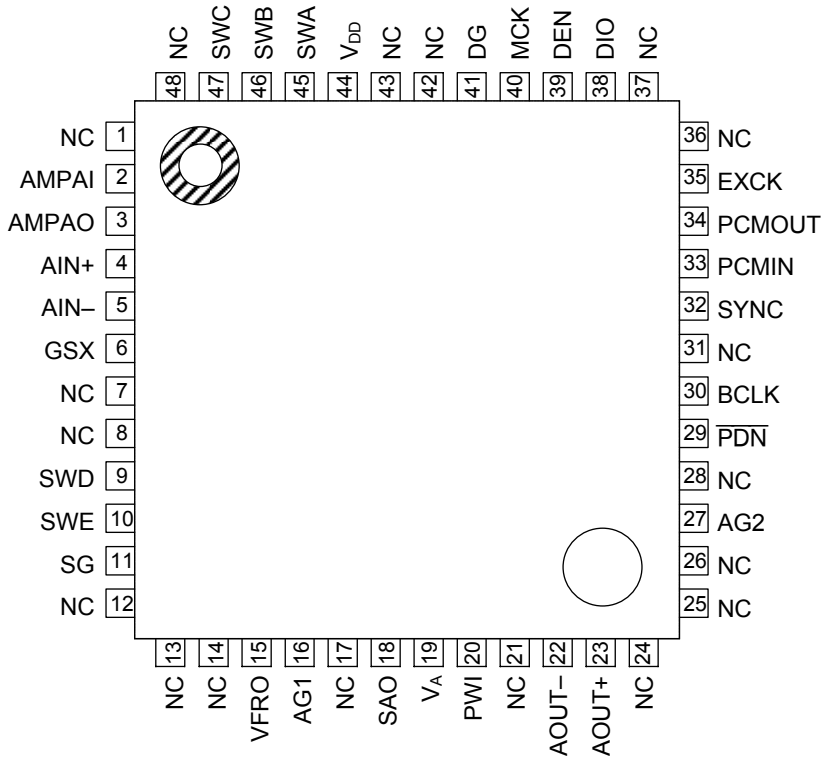
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



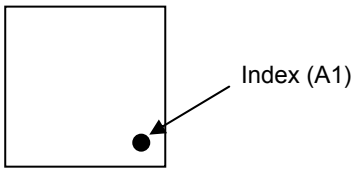
30-Pin Plastic SSOP



NC: No Connection

48-Pin Plastic TQFP

	8	7	6	5	4	3	2	1
H	AG2	AOUT+	AOUT-	PWI	V_A	SAO	AG1	VFRO
G	$\overline{PDN}$	NC	NC	NC	NC	NC	SG	SWE
F	BCLK	NC					NC	SWD
E	SYNC	NC					NC	GSX
D	PCMIN	NC					NC	AIN-
C	PCMOUT	NC					NC	AIN+
B	EXCK	DIO	NC	NC	NC	NC	NC	AMPAO
A	DEN	MCK	DG	V_{DD}	SWA	SWB	SWC	AMPAI



NC: No Connection

48-Pin Plastic LGA
48-Pin Plastic BGA

PIN DESCRIPTION

Pin	Symbol	Type	Description
1	V_{DD}	—	Power supply (3.0 V)
2	SWA	IO	Analog switch A
3	SWB	IO	Analog switch B
4	SWC	IO	Analog switch C
5	AMPAI	I	Amplifier A inverting input
6	AMPAO	O	Amplifier A output
7	AIN+	I	Transmit side amplifier non-inverting input
8	AIN–	I	Transmit side amplifier inverting input
9	GSX	O	Transmit side amplifier output
10	SWD	IO	Analog switch D
11	SWE	IO	Analog switch E
12	SG	O	Analog signal ground (1.4 V)
13	VFRO	O	Receive side voice output
14	AG1	—	Analog ground 1 (0 V)
15	SAO	O	Receive side sounder amplifier output
16	V_A	—	Analog power supply (3.0 V)
17	PWI	I	Receive side voice amplifier input
18	AOUT–	O	Receive side voice amplifier output –
19	AOUT+	O	Receive side voice amplifier output +
20	AG2	—	Analog ground 2 (0 V)
21	$\overline{PDN}$	I	Power down control input
22	BCLK	I	PCM data shift clock input
23	SYNC	I	PCM data shift sync signal input
24	PCMIN	I	Receive side PCM signal input
25	PCMOUT	O	Transmit side PCM signal output
26	EXCK	I	Clock signal input for control register
27	DIO	IO	Address and data input or output for control register
28	DEN	I	Enable signal input for control register
29	MCK	I	Master clock input (2.048 MHz)
30	DG	—	Digital ground (0 V)

PIN FUNCTIONAL DESCRIPTION

AIN+, AIN–, GSX

Transmit analog inputs and the output for transmit gain adjustment.
AIN– connects to inverting input of the internal transmit amplifier. AIN+ connects to non-inverting input of the internal transmit amplifier. GSX connects to the internal transmit amplifier output. Refer to Figure 1 for gain adjustment.

VFRO, SAO, AOUT+, AOUT–, PWI

Receive analog outputs and the outputs for receive gain adjustment.
VFRO is the receive filter output for the voice signal. SAO is the receive filter output for an acoustic component of the sound tone. SAO can directly drive 32 Ω load. AOUT+ and AOUT– are differential analog signal outputs which can directly drive a 32 Ω load. Refer to Figure 1.

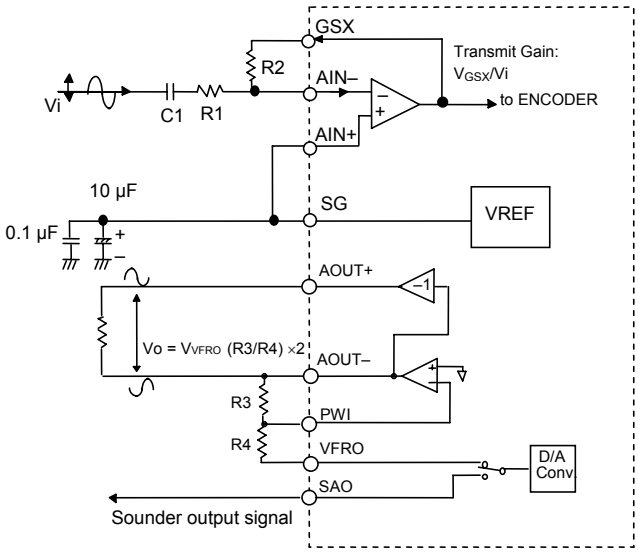


Figure 1 Analog Input/Output Interface

SG

Analog signal ground.
The output voltage of this pin is approximately 1.4 V. Put the bypass capacitors (10 µF in parallel with 0.1 µF ceramic type) between this pin and AG to get the specified noise characteristics. During power-down, this output voltage is 0 V.

AMPAI, AMPAO

Used for amplifier A. The pin AMPAI is connected to the amplifier A inverting input, and the pin AMPAO is connected to the amplifier A output.

SWA, SWB, SWC

Used for the internal analog switch. The pin SWB connects to the pin SWA or the pin SWC. This is controlled by CR1-B1.

SWD, SWE

Used for the internal analog switch. The pin SWD connects to the pin SWE or not. This is controlled by CR1-B2.

V_{DD}, V_A

+3 V power supply for analog. V_{DD} is the digital power supply. V_A is the analog power supply.
Since these pins are separated in the device, connect them as close as possible on the PCB.

DG, AG1, AG2

Ground. DG is the digital system ground. AG1 and AG2 are connected to the analog system ground.
The DG pin must be kept as close as possible to AG1 and AG2 on the PCB.

PDN

Power down and reset control input.
When set to digital "0", the system changes to the power down state and control registers are reset. Since the power down mode is controlled by a logical OR with CR0-B5 of the control register, set CR0-B5 to logic "0" when using this pin.
Be sure to reset the control registers by executing this power down to keep this pin to digital "0" level for 200 ns or longer after the power is turned on and V_{DD} exceeds 2.4 V.

MCK

Master clock input.
The frequency must be 2.048 MHz. MCK can be asynchronous with SYNC and BCLK.

BCLK

Shift clock input for the PCM data.
The frequency is set in the range of 64 kHz to 2048 kHz.

SYNC

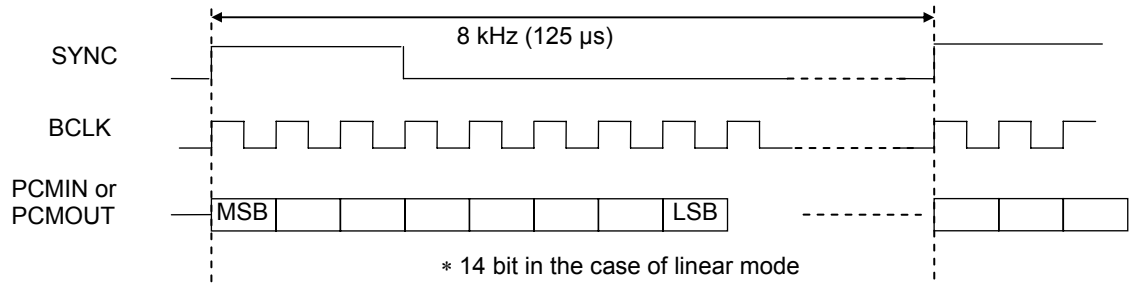
8 kHz synchronous signal input for transmit and receive PCM data.
Synchronize this signal with BCLK signal. Refer to Figure 2.

PCMOUT

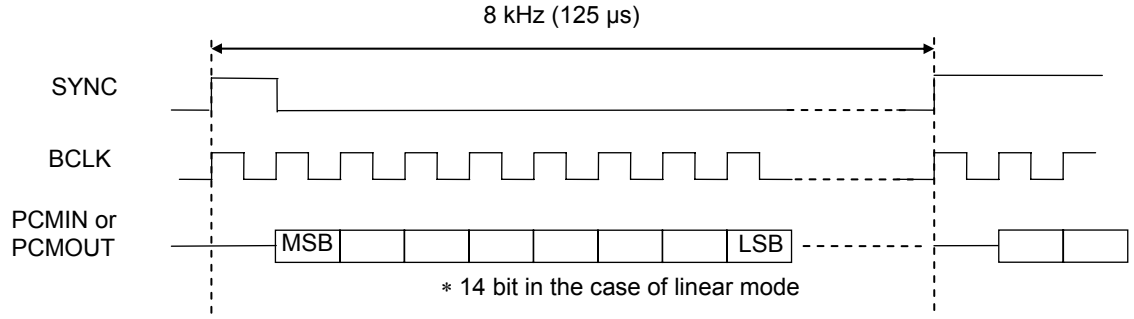
Transmit PCM data output.
This PCM output signal is output from MSB synchronously with the rising edge of BCLK and SYNC. Refer to Figure 2. This is a logic output pin so that external pull-up is not required. This pin outputs logic "L" except during effective PCM data bits, and outputs logic "H" during power-down.

PCMIN

Receive PCM data input.
This PCM input signal is shifted in on the falling edge of BCLK and is input from MSB.
Refer to Figure 2.



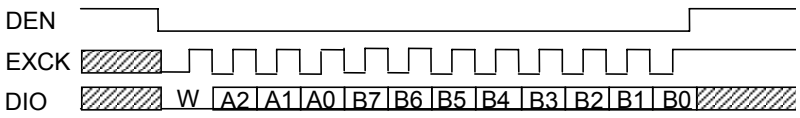
(a) Long frame synchronous interface



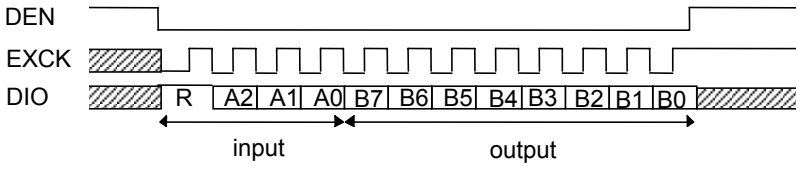
(b) Short frame synchronous interface

Figure 2 PCM Interface Basic Timing Diagram

DEN, EXCK, DIO
Serial control ports for MCU interface.
Reading and writing data is performed by an external MCU through these pins. Eight registers with eight bits are provided on the devices.
DEN is the "Enable" control signal input, EXCK is the data shift clock input, and DIO is the address and data input or output. Figure 3 shows the input or output timing diagram.



(a) Write Data Timing Diagram



(b) Read Data Timing Diagram

Figure 3 MCU Interface Input/Output Timing

Table 1 shows the register map.

Table 1

Name	Address			Control and Detect Data								R/W
	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	A/μ SEL	PON AOUT	PDN ALL	PDN TX	PDN RX	SLP	SLP SEL	LNR	R/W
CR1	0	0	1	—	—	—	—	SHORT FRAME	SW D/E	SW C/A	RX PAD	R/W
CR2	0	1	0	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR3	0	1	1	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0	R/W
CR4	1	0	0	DTMF/ OTHERS SEL	TONE SEND	SAO/ VFRO	TONE4	TONE3	TONE2	TONE1	TONE0	R/W
CR5	1	0	1	—	—	—	—	—	—	—	—	R/W
CR6	1	1	0	VOX ON/OFF	ON LVL1	ON LVL0	—	—	—	—	—	R/W
CR7	1	1	1	VOX OUT	TX NOISE LVL1	TX NOISE LVL0	—	—	—	—	—	R

R/W : Read/Write enable R : Read only register

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +5.0	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD}+0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	+2.4	+3.0	+3.3	V
Operating Temperature	Ta	—	–40	—	+85	°C
Input High Voltage	V_{IH}	To all digital input pins	0.7 x V_{DD}	—	V_{DD}	V
Input Low Voltage	V_{IL}	To all digital input pins	0	—	0.16 x V_{DD}	V
Digital Input Rise Time	t_{ir}	To all digital input pins	—	—	50	ns
Digital Input Fall Time	t_{if}	To all digital input pins	—	—	50	ns
Digital Output Load	C_{DL}	To all digital output pins	—	—	100	pF
Bypass Capacitor for SG	C_{SG}	Between SG and AG	10+0.1	—	—	µF
Master Clock Frequency	F_{MCK}	MCK	–0.01%	2.048	0.01%	MHz
Bit Clock Frequency	F_{BCK1}	BCLK (A/µ-law)	64	—	2048	kHz
	F_{BCK2}	BCLK (Linear)	128	—	2048	kHz
Synchronous Signal Frequency	F_{SYNC}	SYNC	—	8.0	—	kHz
Clock Duty Ratio	D_{CLK}	MCK, BCLK, EXCK	40	50	60	%
Sync Pulse Setting Time	T_{SB}	SYNC → BCLK	-100	—	100	ns
	T_{BS}	BCLK → SYNC	100	—	—	ns
Synchronous Signal Width	t_{WS}	SYNC	1BCLK	—	100	µs

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.4 V to 3.3 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operation Mode No Signal (V_{DD} = 3.0 V)	0	5.0	11.0	mA
	I_{DD2}	Operation Mode No Signal (V_{DD} = 3.0 V) AOUT+, AOUT– or SAO is active	0	9.0	20.0	mA
	I_{DD3}	Power Down Mode (V_{DD} = 3.0 V, Ta = 25°C)	0	1.0	10	µA
Input Leakage Voltage	I_{IH}	$V_I = V_{DD}$	—	—	2.0	µA
	I_{IL}	V_I = 0 V	—	—	0.5	µA
Output High Voltage	V_{OH}	I_{OH} = 0.4 mA	0.5 x V_{DD}	—	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = –1.2 mA	0	0.2	0.4	V
Input Capacitance	C_{IN}	—	—	5	—	pF

Analog Interface Characteristics

(V_{DD} = 2.4 V to 3.3 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	AMPAI, AIN+, AIN–, PWI	10	—	—	MΩ
Output Load Resistance	R_{LGX1}	AMPAO, GSX, VFRO	20	—	—	kΩ
	R_{LGX2}	SAO, AOUT+, AOUT–	32	—	—	Ω
Output Load Capacitance	C_{LGX}	Analog output pins	—	—	100	pF
Output Amplitude	V_{O1}	AMPAO, GSX, VFRO RL = 20 kΩ SAO RL = 32Ω	—	—	*1 1.3	VPP
	V_{O2}	AOUT+, AOUT– Differential output V_{DD} = 2.7 to 3.3 V RL = 32Ω	—	—	3.0	VPP
	*2 V_{O3}	AOUT+, AOUT– Differential output V_{DD} = 3.0 V RL = 30Ω	—	—	3.98	VPP
Total Harmonic Distortion	THD_1	SAO, AOUT+, AOUT–(V_{O1}, V_{O2})	—	—	1.0	%
	*2 THD_2	AOUT+, AOUT– (V_{O3})	—	1.0	—	%
Input Offset Voltage	V_{OFGX1}	AMPAO, GSX	–20	—	20	mV
	V_{OFGX2}	VFRO, SAO, AOUT+, AOUT–	–100	—	100	mV
SG Output Voltage	V_{SG}	SG	—	1.4	—	V
SG Output Impedance	R_{SG}	SG	—	40	80	kΩ
Internal Switch ON Impedance	R_{sw}	All internal switches	—	—	300	Ω

*1 –7.7 dBm (600Ω) = 0 dBm0 , +3.17 dBm0 = 1.3 VPP

*2 Expected value

AC Characteristics

(V_{DD} = 2.4 V to 3.3 V, Ta = –40°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)	Others				
Transmit Frequency Response	L_{OSS} T1	0 to 60	0	—	25	—	—	dB
	L_{OSS} T2	300 to 3000			–0.15	—	0.20	dB
	L_{OSS} T3	1020			Reference			dB
	L_{OSS} T4	3300			–0.15	—	0.80	dB
	L_{OSS} T5	3400			0	—	0.80	dB
	L_{OSS} R6	3968.75			13	—	—	dB
Receive Frequency Response	L_{OSS} R1	0 to 3000	0	—	–0.15	—	0.20	dB
	L_{OSS} R2	1020			Reference			dB
	L_{OSS} R3	3300			–0.15	—	0.80	dB
	L_{OSS} R4	3400			0	—	0.80	dB
	L_{OSS} R5	3968.75			13	—	—	dB
Transmit Signal to Distortion Ratio	SD T1	1020	3	(*1)	35	—	—	dB
	SD T2		0		35	—	—	dB
	SD T3		–30		35	—	—	dB
	SD T4		–40		28	—	—	dB
	SD T5		–45		23	—	—	dB
Receive Signal to Distortion Ratio	SD R1	1020	3	(*1)	35	—	—	dB
	SD R2		0		35	—	—	dB
	SD R3		–30		35	—	—	dB
	SD R4		–40		28	—	—	dB
	SD R5		–45		23	—	—	dB
Transmit Gain Tracking	GT T1	1020	3	—	–0.2	—	0.2	dB
	GT T2		–10		Reference			dB
	GT T3		–40		–0.2	—	0.2	dB
	GT T4		–50		–0.6	—	0.6	dB
	GT T5		–55		–1.2	—	1.2	dB
Receive Gain Tracking	GT R1	1020	3	—	–0.2	—	0.2	dB
	GT R2		–10		Reference			dB
	GT R3		–40		–0.2	—	0.2	dB
	GT R4		–50		–0.6	—	0.6	dB
	GT R5		–55		–1.2	—	1.2	dB

AC Characteristics (Continued)

(V_{DD} = 2.4 V to 3.3 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)	Others				
Idle Channel Noise	N_{IDLT}	—	AIN = SG	(*1)	—	—	–68	dBm0p
	N_{IDLR}	—	—	(*1,*2)	—	—	–72	
Absolute Signal Amplitude	A_{VT}	1020	0	GSX	0.285	0.320 (*3)	0.359	Vrms
	A_{VR}			VFRO	0.285	0.320 (*3)	0.359	Vrms
Power Supply Noise Rejection Ratio	P_{SRRT}	Noise Freq: 0 to 50 kHz	Noise Level: 50 mVpp	—	30	—	—	dB
	P_{SRRR}				30	—	—	dB
Digital Input/Output Timing PCM Interface	t_{SDX} t_{SDR}	—	1 LSTTL + 100 pF	See Fig. 5	0	—	200	ns
	t_{XD1} t_{RD1}				0	—	200	ns
	t_{XD2} t_{RD2}				0	—	200	ns
	t_{XD3} t_{RD3}				0	—	200	ns
Serial Port Digital Input/Output Setting Time	t_{M1}	—	CL = 50 pF	See Fig. 6	50	—	—	ns
	t_{M2}				50	—	—	ns
	t_{M3}				50	—	—	ns
	t_{M4}				50	—	—	ns
	t_{M5}				100	—	—	ns
	t_{M6}				50	—	—	ns
	t_{M7}				50	—	—	ns
	t_{M8}				0	—	100	ns
	t_{M9}				50	—	—	ns
	t_{M10}				50	—	—	ns
	t_{M11}				0	—	50	ns
Shift Clock Frequency	f_{EXCK}	—	—	EXCK	—	—	10	MHz

*1 Use the P-message weighted filter.
*2 PCMIN input code "11010101"(A-law)
"11111111"(μ-law)
*3 0.320 Vrms = 0 dBm0 = –7.7 dBm

AC Characteristics (DTMF and Other Tones)

(V_{DD} = 2.4 V to 3.3 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Frequency Difference	D_{FT}	DTMF Tones, Other Tones		–1.5	—	+1.5	%
Original (Reference) Tones Signal Level *4	V_{TL}	Transmit Tones (Gain setting 0 dB)	DTMF (Low)	–18	–16	–14	dBm0
	V_{TH}		DTMF (High) and Other Tones	–16	–14	–12	dBm0
	V_{RL}	Receive Tones (Gain setting –6 dB)	DTMF (Low)	–10	–8	–6	dBm0
	V_{RH}		DTMF (High) and Other Tones	–8	–6	–4	dBm0
Relative Level of DTMF Tones	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		+1	+2	+3	dB

*4 Does not include the setting value for the programmable gain.

AC Characteristics (Programmable Gain Stages)

(V_{DD} = 2.4 V to 3.3 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Gain Accuracy	D_G	All gain stages, to programmed value	–1	0	+1	dB

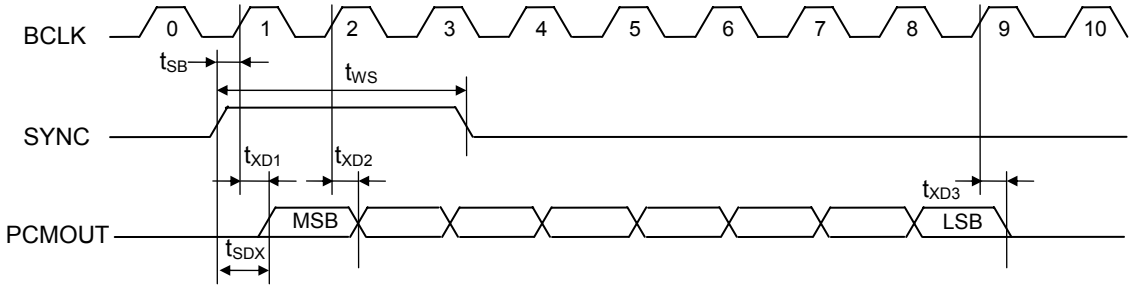
AC Characteristics (Voice Detect Function)

(V_{DD} = 2.4 V to 3.3 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Voice Detection Time	TVON	Silence>Voice	—	5	—	ms
	TVOF	(Voice/Silence differential: 10 dB)	140	160	180	ms
Voice Detection Accuracy	DVX	For detection level set values by CR6-B6, B5	–2.5	0	2.5	dB

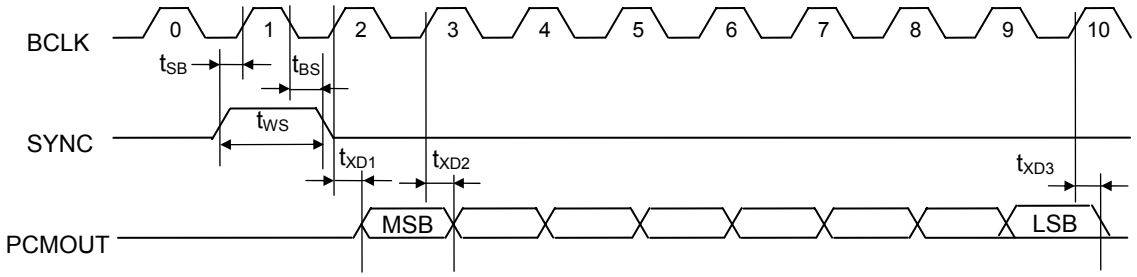
TIMING DIAGRAM

Transmit Side PCM Timing (Normal Synchronous Interface)

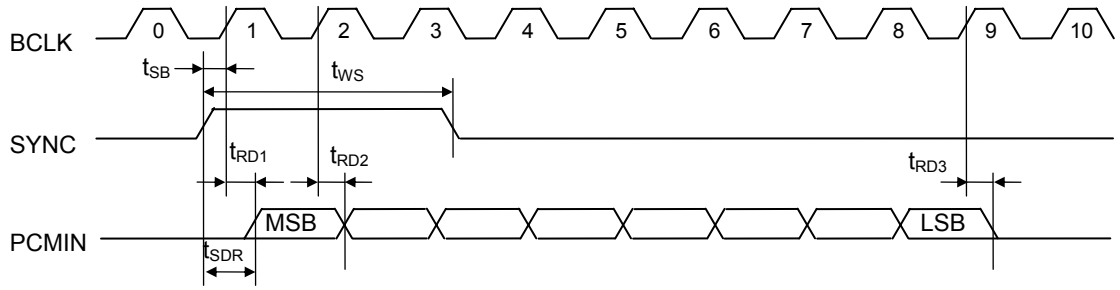


When t_{SB} >= 0, the Delay of the MSB is defined as t_{XD1}.
When t_{SB} < 0, the Delay of the MSB is defined as t_{SDX}.

Transmit Side PCM Timing (Short Frame Synchronous Interface)



Receive Side PCM Timing (Normal Synchronous Interface)



Receive Side PCM Timing (Short Frame Synchronous Interface)

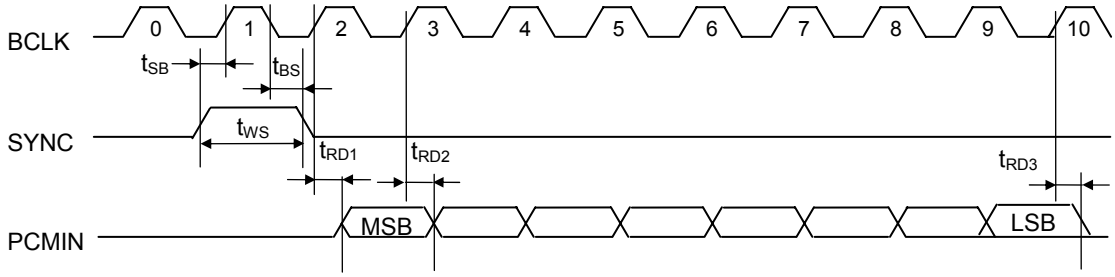


Figure 4 PCM Interface Timing

Serial Port Timing for Microcontroller Interface

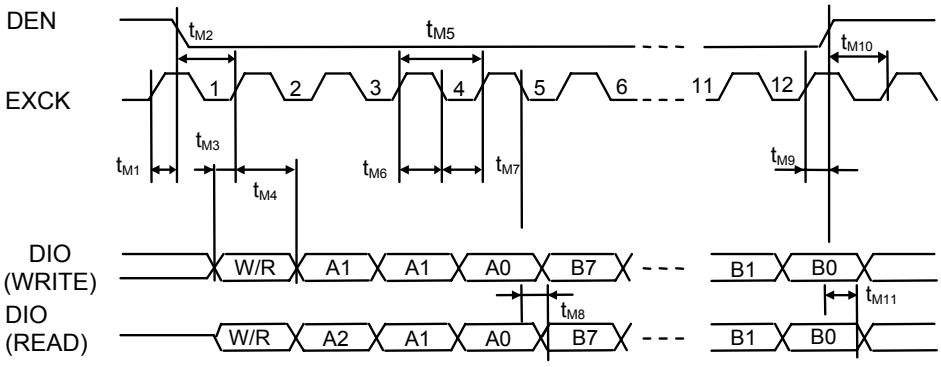


Figure 5 Serial Control Port Interface

FUNCTIONAL DESCRIPTION

Control Registers

CR0 (Basic operating mode 1)

Note: Initial Value: Reset state by $\overline{PDN}$

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	A/μ SEL	PON AOUT	PDN ALL	PDN TX	PDN RX	SLP	SLP SEL	LNR
Initial Value	0	0	0	0	0	0	0	0

B7····· PCM companding law select; 0/μ-law, 1/A-law

B6····· Power on control for output amps (AOUT+, AOUT–); 0/Power down, 1/Power on

B5····· Power down (entire system); 0/Power on, 1/Power down
When using this data for power down control, set pin PDN at "1" level.
The control registers are not reset by this signal.

B4····· Power down (transmit and amplifier A); 0/Power on, 1/Power down

B3····· Power down (receive only); 0/Power on, 1/Power down

B2····· Slope filter enable; 0/Slope filter disable, 1/ Slope filter enable

B1····· The type of slope filter select; 0/CASE1, 1/CASE2, refer to Figure 6.

B0····· PCM interface linear code select;
0/Companding law selected by CR0-B7
1/14-bit linear code (2's complement) in spite of CR0-B7

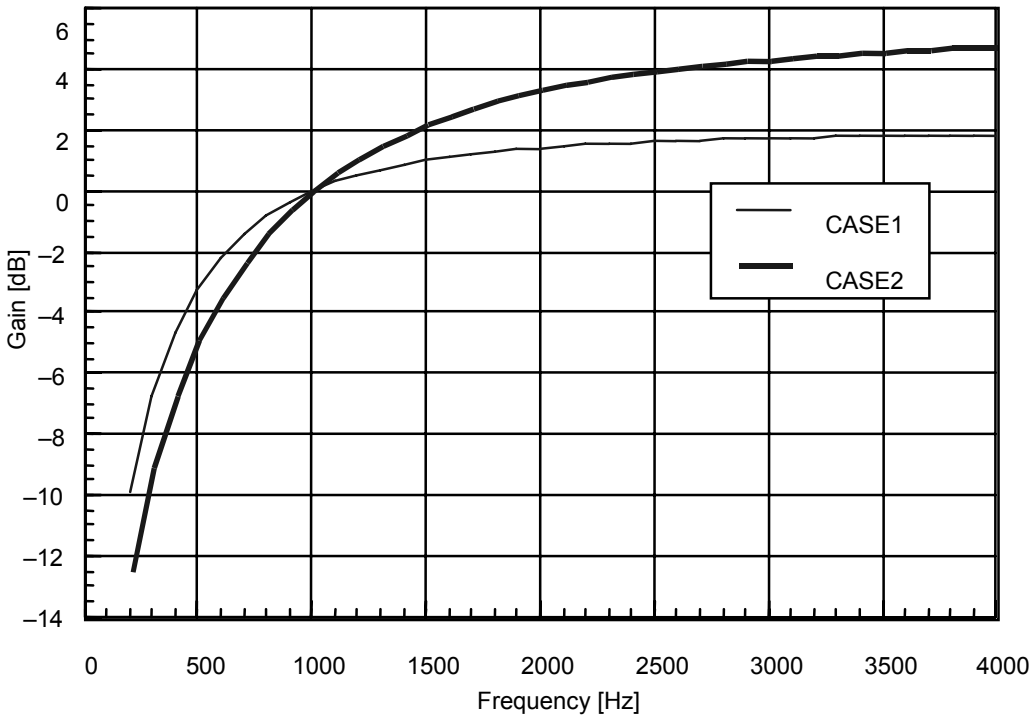


Figure 6 Frequency Response of Slope Filter

CR1 (Basic operating mode 2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	—	—	—	—	SHORT FRAME	SW D/E	SW C/A	RX PAD
Initial Value	0	0	0	0	0	0	0	0

B7, B6, B5, B4……Not used

B3……Short frame synchronous interface select;
0/Long frame synchronous interface, 1/Short frame synchronous interface

B2……Analog switch control : 0/SWD to SWE open, 1/ SWD to SWE closed

B1……Analog switch control : 0/SWB to SWA closed. The SWC pin is high impedance.
1/SWB to SWC closed. The SWA pin is high impedance.

B0……Receive side PAD : 1/inserted, 12 dB loss
0/no PAD

CR2 (PCM CODEC operating mode setting and transmit/receive gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0
Initial Value	0	0	1	1	0	0	1	1

B7····· PCM coder disable; 0/Enable, 1/Disable (transmit PCM idle pattern)

B6, B5, B4····· Transmit gain adjustment, refer to Table 2.

B3····· PCM decoder disable; 0/Enable, 1/Disable (receive PCM idle pattern)

B2, B1, B0····· Receive gain adjustment, refer to Table 2.

Table 2

B6	B5	B4	Transmit Gain	B2	B1	B0	Receive Gain
0	0	0	–6 dB	0	0	0	–12 dB
0	0	1	–4 dB	0	0	1	–9 dB
0	1	0	–2 dB	0	1	0	–6 dB
0	1	1	0 dB	0	1	1	–3 dB
1	0	0	+2 dB	1	0	0	0 dB
1	0	1	+4 dB	1	0	1	+3 dB
1	1	0	+6 dB	1	1	0	+6 dB
1	1	1	+8 dB	1	1	1	+9 dB

The above gain settings table shows the transmit/receive voice signal gain settings and the transmit side gain settings for DTMF tones and other tones. Tone signal transmission is enabled by CR4-B6, and the gain setting is set to the levels shown below.

DTMF tones (low group): –16 dBm0
DTMF tones (high group) and other tones: –14 dBm0

For example, if the transmit gain set value is set to +8 dB (B6, B5, B4) = (1, 1, 1), then the following tones appear at the PCMOUT pin.

DTMF tones (low group): –8 dBm0
DTMF tones (high group) and other tones: –6 dBm0

Gain setting for the side tone (path to the receive side from the transmit side) and the receive side tone is provided by register CR3.

CR3 (Side tone and other tone generator gain setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0
Initial Value	0	0	0	0	0	0	0	0

B7, B6, B5·····Side tone path gain setting, refer to Table 3.

B4····· Tone generator enable; 0/Disable, 1/Enable

B3, B2, B1, B0····· Tone generator gain adjustment for receive side, refer to Table 4.

Table 3

B7	B6	B5	Side Tone Path Gain
0	0	0	OFF
0	0	1	–15 dB
0	1	0	–13 dB
0	1	1	–11 dB
1	0	0	–9 dB
1	0	1	–7 dB
1	1	0	–5 dB
1	1	1	–3 dB

Table 4

B3	B2	B1	B0	Tone Generator Gain	B3	B2	B1	B0	Tone Generator Gain
0	0	0	0	OFF	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

The tone generator gain setting table for the receive side, as shown in Table 4, depends upon the following reference levels.

DTMF tones (low group): –2 dBm0
DTMF tones (high group) and other tones: 0 dBm0

For example, when selecting –6 dB (B3, B2, B1, B0) = (1, 1, 1, 1) as a tone generator gain, the signal amplitude of each DTMF tone on SAO or VFRO is as follows:

DTMF tones (low group): –8 dBm0
DTMF tones (high group) and other tones: –6 dBm0

CR4 (Tone generator operating mode and frequency select)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	DTMF/ Others SEL	TONE SEND	SAO/ VFRO	TONE4	TONE3	TONE2	TONE1	TONE0
Initial Value	0	0	0	0	0	0	0	0

B7 ····· DTMF or other tones select; 0/Others, 1/DTMF
B6 ····· Tone transmit enable (transmit side); 0/Voice signal (transmit), 1/Tone transmit
B5 ····· Tone output pin select (receive side); 0/VFRO, 1/SAO
B4, B3, B2, B1, B0 ··· Tone frequency setting, refer to Tables 5-1 and 5-2.

(a) B7 = 1 (DTMF tones)

Table 5-1

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
*	0	0	0	0	697 Hz + 1209 Hz	*	1	0	0	0	852 Hz + 1209 Hz
*	0	0	0	1	697 Hz + 1336 Hz	*	1	0	0	1	852 Hz + 1336 Hz
*	0	0	1	0	697 Hz + 1477 Hz	*	1	0	1	0	852 Hz + 1477 Hz
*	0	0	1	1	697 Hz + 1633 Hz	*	1	0	1	1	852 Hz + 1633 Hz
*	0	1	0	0	770 Hz + 1209 Hz	*	1	1	0	0	941 Hz + 1209 Hz
*	0	1	0	1	770 Hz + 1336 Hz	*	1	1	0	1	941 Hz + 1336 Hz
*	0	1	1	0	770 Hz + 1477 Hz	*	1	1	1	0	941 Hz + 1477 Hz
*	0	1	1	1	770 Hz + 1633 Hz	*	1	1	1	1	941 Hz + 1633 Hz

*Undefined

(b) B7 = 0 (Other tones)

Table 5-2

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
0	0	0	0	0	2730 Hz/2500 Hz 8 Hz wamble	1	0	0	0	0	1200 Hz
0	0	0	0	1	2000 Hz/2667 Hz 8 Hz wamble	1	0	0	0	1	1300 Hz
0	0	0	1	0	1000 Hz/1333 Hz 8 Hz wamble	1	0	0	1	0	—
0	0	0	1	1	—	1	0	0	1	1	1477 Hz
0	0	1	0	0	—	1	0	1	0	0	1633 Hz
0	0	1	0	1	—	1	0	1	0	1	2000 Hz
0	0	1	1	0	—	1	0	1	1	0	2100 Hz
0	0	1	1	1	—	1	0	1	1	1	—
0	1	0	0	0	—	1	1	0	0	0	2400 Hz
0	1	0	0	1	400 Hz	1	1	0	0	1	—
0	1	0	1	0	440 Hz	1	1	0	1	0	2500 Hz
0	1	0	1	1	480 Hz	1	1	0	1	1	—
0	1	1	0	0	—	1	1	1	0	0	—
0	1	1	0	1	667 Hz	1	1	1	0	1	2700 Hz
0	1	1	1	0	800 Hz	1	1	1	1	0	—
0	1	1	1	1	1000 Hz	1	1	1	1	1	3000 Hz

CR5 (Not used)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0

B7-B0…… Not used

CR6 (VOX function control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	VOX ON/OFF	ON LVL1	ON LVL0	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0

B7 …… VOX function enable; 0/Disable, 1/Enable
If B7 is set to a logic “1”, B3 should be set to a logic “1”.
B6, B5…… Voice detector level setting;
(0,0): –20 dBm0 (0,1): –26 dBm0 (1,0): –32 dBm0 (1,1): –38 dBm0
B4, B2, B1, B0 …… Not used

CR7 (Detect register, read only)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	VOX OUT	TX NOISE LVL1	TX NOISE LVL0	—	—	—	—	—
Initial Value	0	0	0	*	*	*	*	*

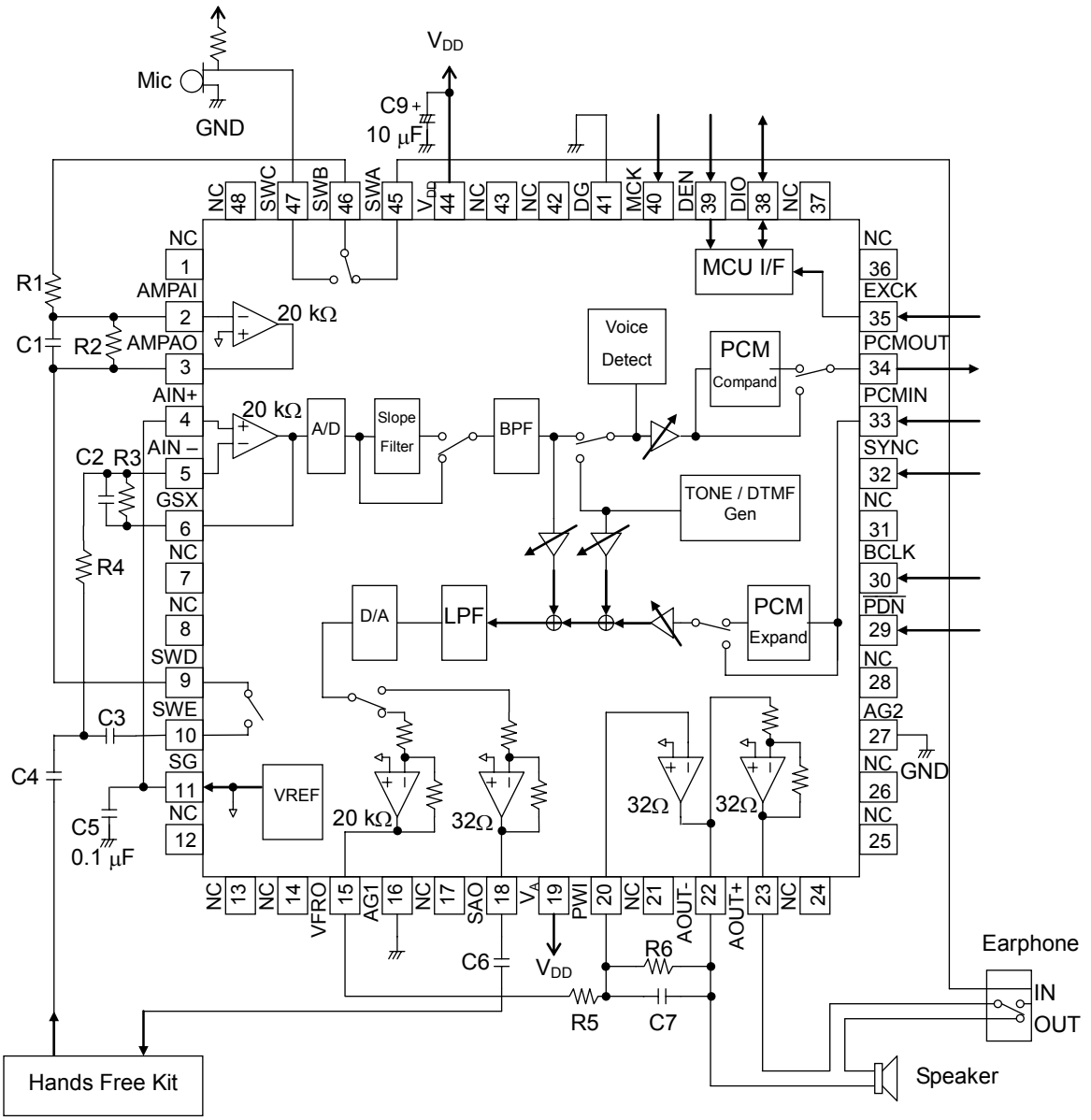
*For IC testing

B7…… Voice detection; 0/Silence, 1/Voice detect
B6, B5…… Voice detect level (indicator);
(0,0): Below –50 dBm0 (0,1): –40 to –50 dBm0
(1,0): –30 to –40 dBm0 (1,1): Above –30 dBm0

Note: These outputs are enabled when the VOX function is turned on by CR6-B7.

B4, B3, B2, B1, B0…… Not used

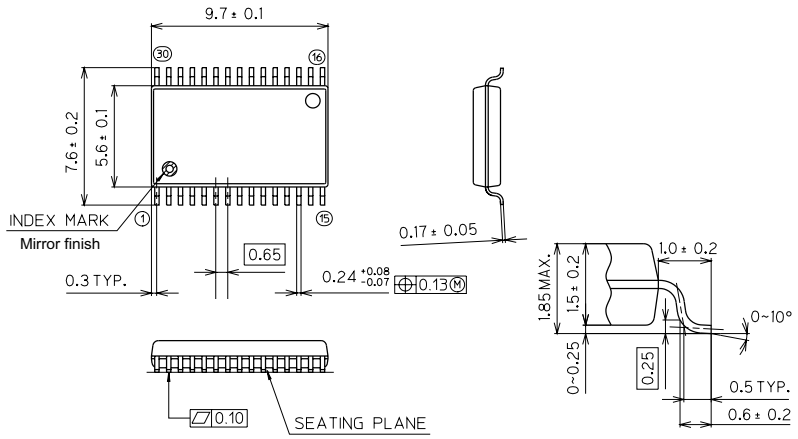
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit: mm)

SSOP30-P-56-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.19 TYP.
Rev. No./Last Revised	5/Dec. 5, 1996

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Notes for Mounting the Surface Mount Type Package

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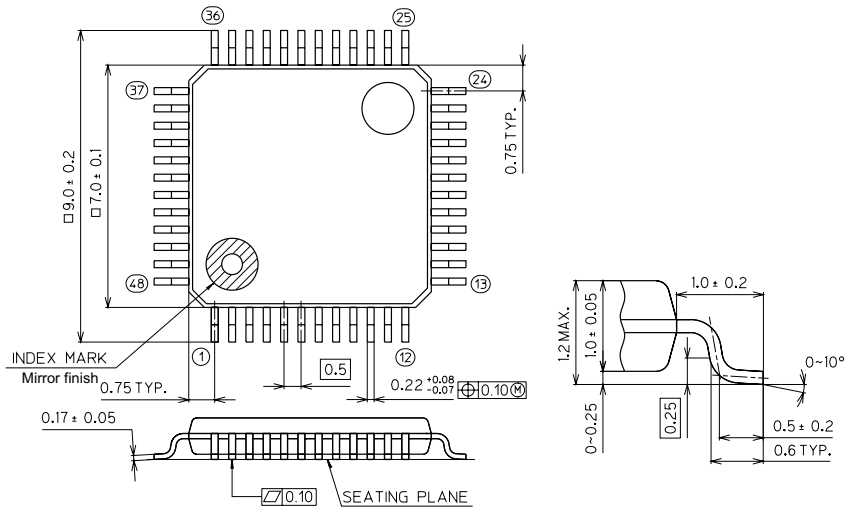
(Unit: mm)

TQFP48-P-0707-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.13 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

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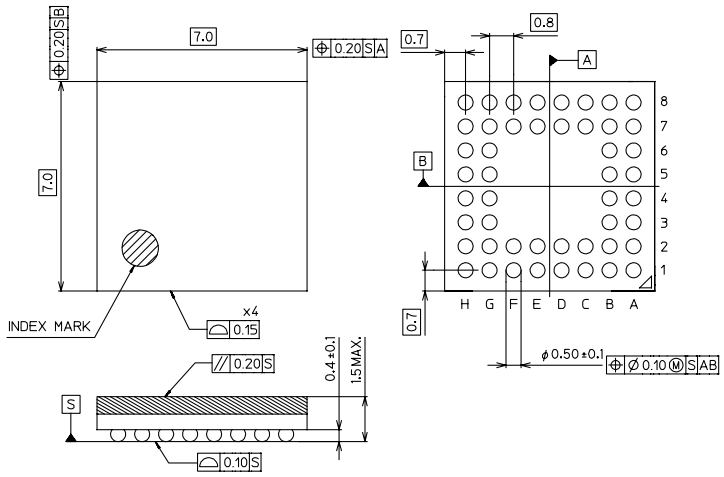
(Unit: mm)

P-LFBGA48-0707-0.80



Package material	Epoxy resin
Package weight (g)	0.12 TYP.
Rev. No./Last Revised	1/Jun. 20, 2001

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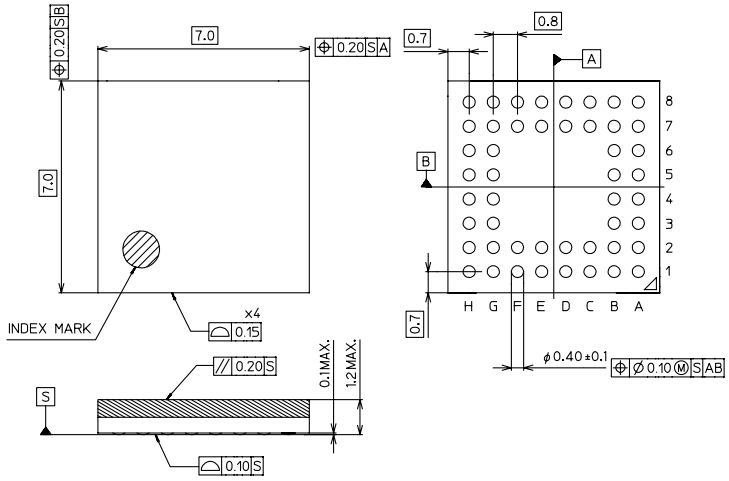
(Unit: mm)

P-TFLGA48-0707-0.80



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Package material	Epoxy resin
Package weight (g)	0.10 TYP.
Rev. No./Last Revised	2/Jun. 20, 2001

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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7732-01-04	Nov. 2001	—	—	Edition 4
FEDL7732-01-05	Jan. 15, 2002	26	26	Changed the package outline diagram.
		27	27	Changed the package outline diagram.
FEDL7732-01-06	Jun. 3, 2004	2	2	Addition of RX PAD in the Block Diagram.
FEDL7732-01-07	Jun. 15, 2004	8	8	More clarification of PCMOUT output state
FEDL7732-01-08	Jul. 29, 2004	23	23	Correction of false connection of C2 and R3 in APPLICATION CIRCUIT
FEDL7732-01-09	May 18, 2005	2	2	Addition of TXON/OFF and RXON/OFF in the Block Diagram
FEDL7732-01-10	Nov 2, 2005	10	10	Addition of t_{SB}
		15	15	Addition of t_{SB} Addition of description about $t_{XD1}$and t_{SDX}

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