

STRUCTURE Silicon Monolithic Integrated Circuit

TYPE Voltage Detector with Watchdog Timer

PRODUCT SERIES **B D 8 7 A 4 1 F V M**

FEATURES
 1. High detection voltage precision: $\pm 1.5\%$ ($T_a=25^\circ\text{C}$)/ Low quiescent current: $5\ \mu\text{A}$.
 2. Reset delay time and Watchdog time can be set with external capacitance.

○ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

| Parameter | Symbol | Limit | Unit |
|------------------------------|--------|--------------|------|
| Supply Voltage | VDD | -0.3~10 | V |
| CT Pin Voltage | VCT | -0.3~VDD+0.3 | V |
| CTW Pin Voltage | VCTW | -0.3~VDD+0.3 | V |
| RESET Pin Voltage | VRESET | -0.3~VDD+0.3 | V |
| INH Pin Voltage | VINH | -0.3~VDD+0.3 | V |
| CLK Pin Voltage | VCLK | -0.3~VDD+0.3 | V |
| Power Dissipation | Pd | 470 ※1 | mW |
| Operating Temperature Range | Topr | -40~+105 | °C |
| Storage Temperature Range | Tstg | -55~+125 | °C |
| Maximum Junction Temperature | Tjmax | 125 | °C |

※1 Reduced by $4.7\text{mW}/^\circ\text{C}$ over $T_a=25^\circ\text{C}$, when mount on a glass epoxy board: $70\text{mm}\times 70\text{mm}\times 1.6\text{mm}$.

○OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|--------------------------|-----------|-----|-----|------|
| Supply Voltage for RESET | VDD RESET | 1.0 | 10 | V |
| Supply Voltage for WDT | VDD WDT | 2.5 | 10 | V |

NOTE) The product described in this specification is a strategic product (and/or service) subject to COCOM regulations. It should not be exported without authorization from the appropriate government.

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

○ELECTRICAL CHARACTERISTICS(Unless otherwise specified, VDD=5V, Ta=-40°C~105°C)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|----------------------------|--------|------------|------------|------------|------|--------------------------------------|
| | | MIN | Typ | MAX | | |
| [Overall] | | | | | | |
| Bias Current 1(WDT ON) | IDD1 | — | 5 | 14 | μA | INH=GND, CTW=0.1 μF |
| Bias Current 2(WDT OFF) | IDD2 | — | 5 | 14 | μA | VDD=INH=5V |
| Output Leak Current | Ileak | — | — | 1 | μA | VDD=VDS=10V |
| Output Current | IOL | 0.7 | — | — | mA | VDD=1.2V, VDS=0.5V |
| [RESET] | | | | | | |
| Detection Voltage 1 | VDET1 | 4.039 | 4.100 | 4.162 | V | Ta=25°C |
| Detection Voltage 2 | VDET2 | 4.007 | 4.100 | 4.202 | V | Ta=-40~105°C |
| Hysteresis Width | Vrhys | VDET*0.018 | VDET*0.035 | VDET*0.050 | V | Ta=-40~105°C |
| Output Delay Time L→H | TPLH | 3.9 | 6.9 | 10.1 | ms | CT=0.001 μF ※1 When VDD=VDET±0.5V |
| Output Delay Resistance | Rrst | 5.8 | 10.0 | 14.5 | MΩ | VCT=GND |
| CT Pin Threshold Voltage | VCTH | VDD×0.3 | VDD×0.45 | VDD×0.6 | V | RL=470kΩ |
| CT Pin Output Current | ICT | 150 | — | — | μA | VDD=1.50V, VCT=0.5V |
| Minimum Operating Voltage | VOPL | 1.0 | — | — | V | VOL≤0.4V, RL=470kΩ |
| [WDT] | | | | | | |
| Watchdog Monitor Time | TWH | 7.0 | 10.0 | 20.0 | ms | CTW=0.01 μF ※2 |
| Watchdog Reset Time | TWL | 2.4 | 3.3 | 7.0 | ms | CTW=0.01 μF ※3 |
| Clock Pulse Width | TWCLK | 500 | — | — | ns | |
| CLK High Threshold Voltage | VCLKH | VDD×0.8 | — | VDD | V | |
| CLK Low Threshold Voltage | VCLKL | 0 | — | VDD×0.3 | V | |
| INH High Threshold Voltage | VINH | VDD×0.8 | — | VDD | V | |
| INH Low Threshold Voltage | VINHL | 0 | — | VDD×0.3 | V | |
| CTW Charge Current | ICTWC | 0.25 | 0.50 | 0.75 | μA | VCTW=0.2V |
| CTW Discharge Current | ICTWO | 0.75 | 1.50 | 2.00 | μA | VCTW=0.8V |

※1 TPLH can be varied by changing the CT capacitance value.

$$TPLH(s) \approx 0.69 \times Rrst (M\Omega) \times CT(\mu F) \quad Rrst=10M\Omega (Typ.)$$

※2 TWH can be varied by changing the CTW capacitance value.

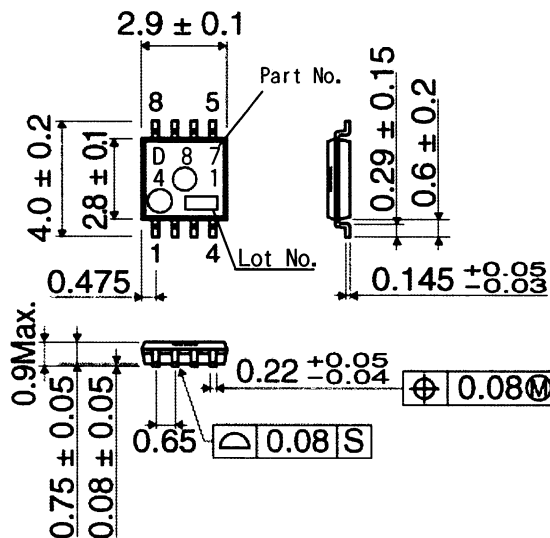
$$TWH(s) \approx (0.5 \times CTW(\mu F)) / ICTWC(\mu A) \quad ICTWC=0.5\mu A (Typ.)$$

※3 TWL can be varied by changing the CTW capacitance value.

$$TWL(s) \approx (0.5 \times CTW(\mu F)) / ICTWO(\mu A) \quad ICTWO=1.5\mu A (Typ.)$$

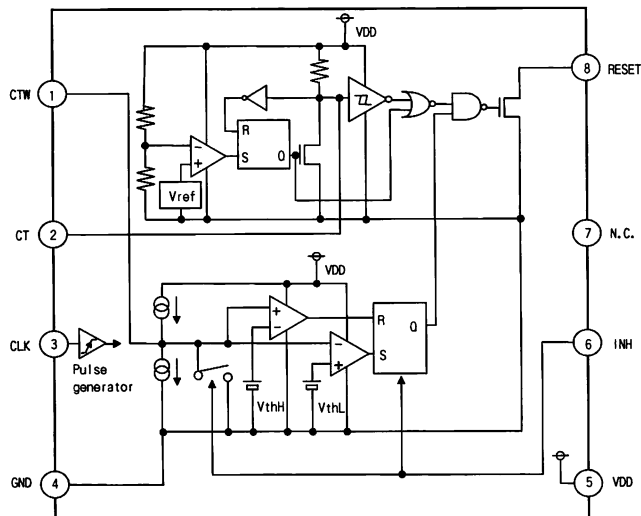
This product is not designed for protection against radio active rays.

○PHYSICAL DIMENSIONS · MARKING



MSOP8 (Unit : mm)

○BLOCK DIAGRAM



○PIN No. • PIN NAME

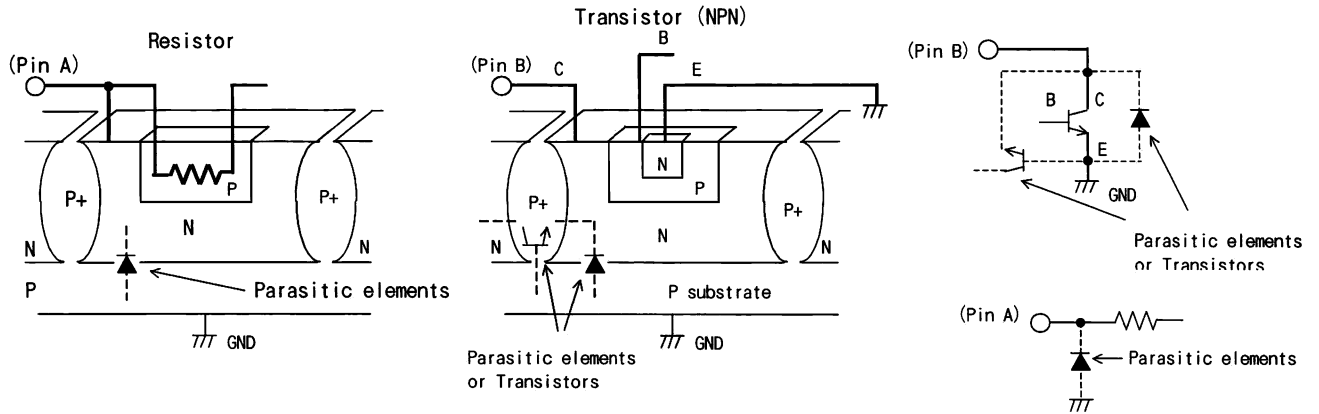
| Pin No. | Pin Name |
|---------|----------|
| 1 | CTW |
| 2 | CT |
| 3 | CLK |
| 4 | GND |
| 5 | VDD |
| 6 | INH |
| 7 | N.C. |
| 8 | RESET |

※Refer to the Technical Note about the details of the application.

○OPERATING NOTES

- 1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.
- 2) GND potential
Ensure a minimum GND pin potential in all operating conditions.
- 3) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
- 4) Pin short and mistake mounting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC. Ensure a minimum GND pin potential in all operating conditions.
- 5) Actions in strong magnetic field
Keep in mind that the IC may malfunction in strong magnetic fields.
- 6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.
- 7) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when the resistors and transistors are connected to the pins as shown in the following figure,
 - The P/N junction functions as a parasitic diode when GND > Pin A for the resistor or GND > Pin B for the transistor (NPN).
 - Similarly, when GND > Pin B for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

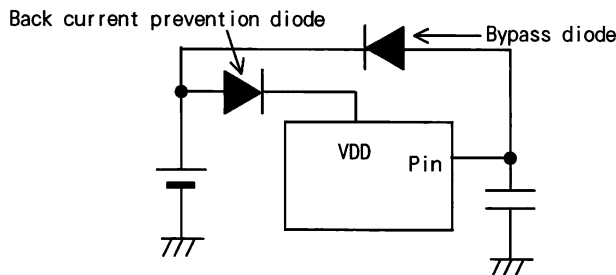
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input pins. Keep in mind that the IC may malfunction in strong magnetic fields.



8) Ground patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external parts, either.

9) Applications or inspection processes where the potentials of the VDD pin and other pins may be reversed from their normal states may cause damage to the IC's internal circuitry or elements. Use an CT pin capacitance of $3.3\mu\text{F}$ or lower and CTW pin capacitance of $10\mu\text{F}$ or lower in case VDD is shorted with the GND pin while the external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VDD or bypass diodes between VDD and each pin.



10) When VDD falls below the operating marginal voltage, output will be open. When output is being pulled up to VDD, output will be equivalent to VDD.

11) Input Pin

CLK and INH pins comprise inverter gates and should not be left open. (These pins should be either pulled up or down.) Input to CLK pin is detected using a positive edge trigger and does not affect CLK signal duty. Input the trigger to CLK pin within TWH time.

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