HAT1048R

Silicon P Channel Power MOS FET
Power Switching

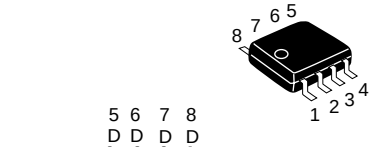
ADE-208-1223A (Z)
2nd. Edition
Jan. 2001

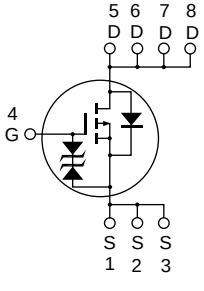
Features

- Capable of -4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 6.0 mΩ typ (at V_{GS} = -10V)

Outline

SOP-8





1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	-16	A
Drain peak current	$I_{D(pulse)}$ Note1	-128	A
Body-drain diode reverse drain current	I_{DR}	-16	A
Channel dissipation	Pch Note2	2.5	W
Channel to Ambient Thermal Impedance	θch-a Note2	50	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	– 55 to + 150	°C

Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

Electrical Characteristics (Ta = 25°C)

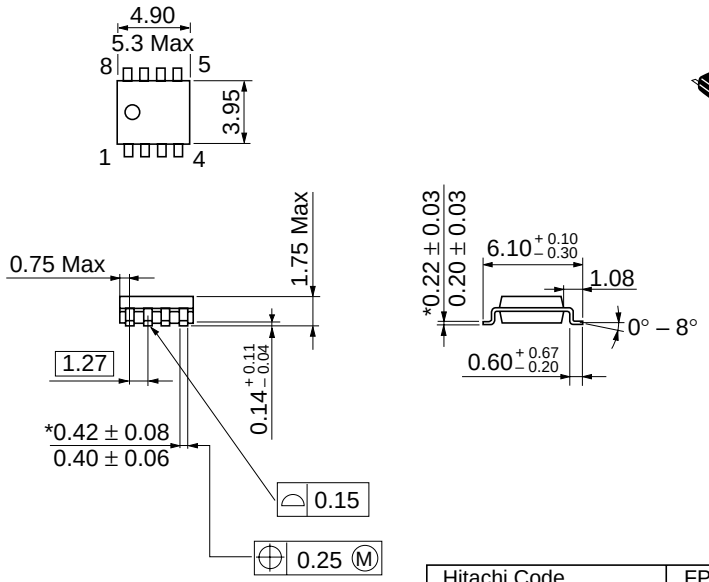
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	I_D = -10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	± 10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	-1	µA	V_{DS} = -30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	V_{DS} = -10 V, I_D = -1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(6.0)	(7.0)	mΩ	I_D = -8 A, V_{GS} = -10 V Note3
	$R_{DS(on)}$	—	(9.5)	(13.5)	mΩ	I_D = -8 A, V_{GS} = -4.5V Note3
Forward transfer admittance	$\|y_{fs}\|$	(18)	(30)	—	S	I_D = -8 A, V_{DS} = -10 V Note3
Input capacitance	Ciss	—	(5700)	—	pF	V_{DS} = -10 V
Output capacitance	Coss	—	(1250)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(710)	—	pF	f = 1 MHz
Total gate charge	Qg	—	(105)	—	nc	V_{DD} = -10 V
Gate to source charge	Qgs	—	(14)	—	nc	V_{GS} = -10 V
Gate to drain charge	Qgd	—	(20)	—	nc	I_D = -16 A
Turn-on delay time	$t_{d(on)}$	—	(25)	—	ns	V_{GS} = -10 V, I_D = -8 A
Rise time	t_r	—	(45)	—	ns	V_{DD} ≅ 10 V
Turn-off delay time	$t_{d(off)}$	—	(140)	—	ns	R_L = 1.25 Ω
Fall time	t_f	—	(55)	—	ns	R_g = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	(-0.85)	(-1.10)	V	IF = -16 A, V_{GS} = 0 Note3
Body–drain diode reverse recovery time	t_{rr}	—	(50)	—	ns	IF = -16 A, V_{GS} = 0 diF/ dt = 50 A/ µs

Note: 3. Pulse test

Package Dimensions

As of January, 2001

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.085 g

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