Si3226/7 and Si3208/9

Dual ProSLIC® with DC-DC Controller

Description

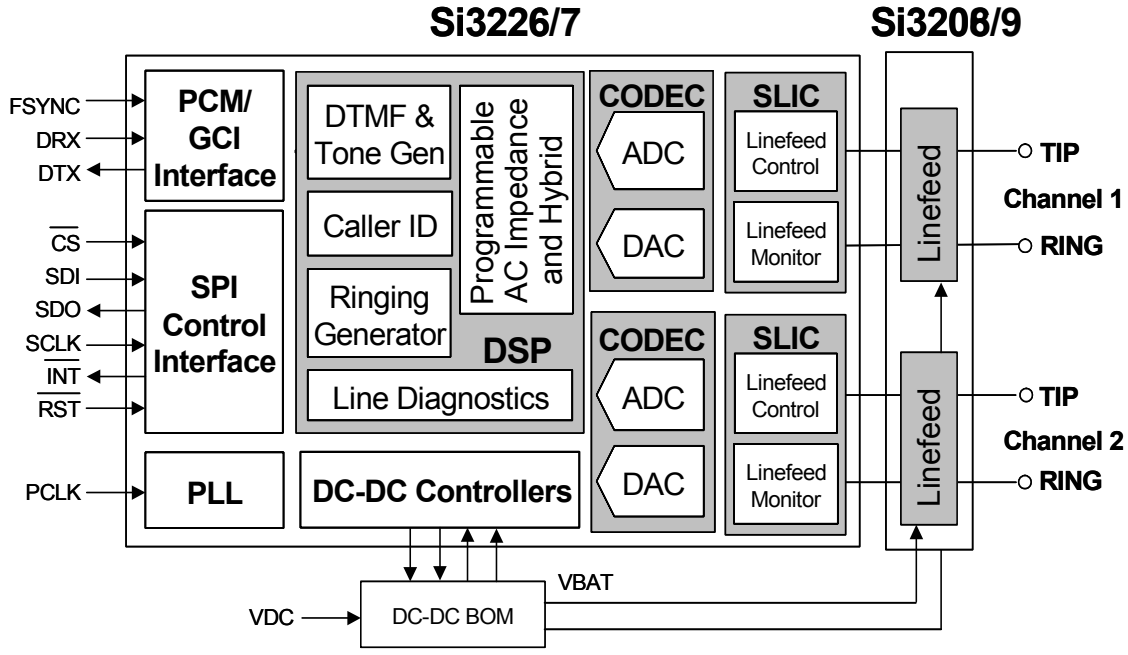
The Dual ProSLIC® is a family of low-voltage CMOS devices that integrate both SLIC and CODEC functionality into a single IC. In combination with a linefeed IC (LFIC), they provide a complete two-channel analog telephone interface in accordance with all relevant LSSGR, ITU, and ETSI specifications. The Dual ProSLIC devices (Si3226/7) operate from a single 3.3 V supply and interface to standard PCM/SPI or GCI bus digital interfaces. The LFICs (Si3208/9) perform all high-voltage functions and operate from a 3.3 V supply as well as high-voltage battery supplies. The Si3208 is rated for –110 V, and the Si3209 is rated for –135 V. The Dual ProSLIC devices are available in a 64-pin thin quad flat package (TQFP), and the LFICs are available in a 40-pin, quad flat no-lead package (QFN).

Features

- Performs all BORSCHT functions
- Ideal for short- or long-loop applications
- Internal balanced or unbalanced ringing
- Low power consumption
- Integrated dc-dc controller
- Wideband CODEC (Si3227)
- Low-power sleep mode
- On-hook transmission
- Software-programmable parameters:
  - Ringing frequency, amplitude, cadence, and wave-shape
  - Two-wire ac impedance
  - Transhybrid balance
  - DC current loop feed (10–45 mA)
  - Loop closure and ring trip thresholds
  - Ground key detect threshold
- Loop or ground start operation
- Smooth polarity reversal
- DTMF generator/decoder
- A-Law/μ-Law companding, linear PCM
- PCM and SPI bus digital interfaces with programmable interrupts
- GCI/IOM-2 mode support
- 3.3 V operation
- GR-909 loop diagnostics
- Audio diagnostics with loopback
- Pb-free/RoHS-compliant packaging

Applications

- Customer Premises Equipment (CPE)
- Optical Network Terminals (ONT)
- Private Branch Exchange (PBX)
- Cable EMTAs, ATAs, VoIP Gateways

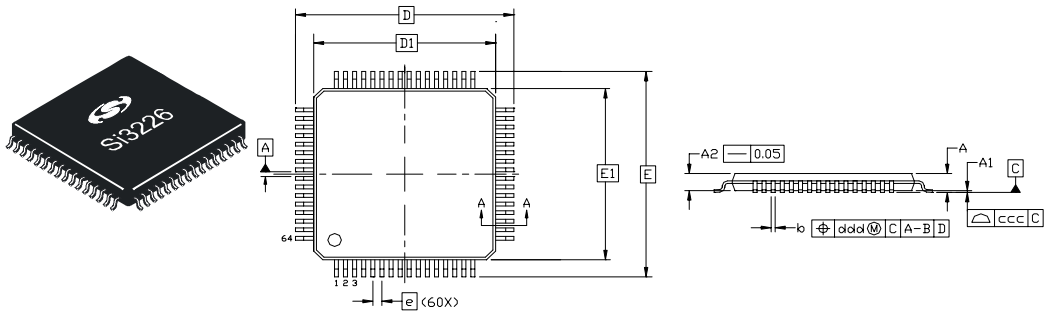


Selected Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typical	Max	Unit
Ambient Temperature	T_A	F-Grade	0	25	70	°C
		G-Grade	–40	25	85	°C
Supply Voltage, Si322x	V_{DD}		3.13	3.3	3.47	V
Supply Voltage, Si3209/8	V_{DD}		3.13	3.3	3.47	V
Battery Voltage, Si3209/8	V_{BAT}		–9	—	–135/–110	V
Maximum Loop Resistance (loop + load)	R_{LOOP}	I_{LOOP}=18 mA, V_{BAT} = –48 V	—	—	2000	Ω
DC Differential Output Resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	160	—	640	Ω
Idle Channel Noise		C-Message weighted	—	8	12	dBrnC
PSRR from V_{DD}		RX and TX, dc to 3.4 kHz	40	—	—	dB
Longitudinal to Metallic/PCM Balance (forward or reverse)		200 Hz to 1 kHz	58	60	—	dB
		1 kHz to 3.4 kHz	53	58	—	dB
Metallic/PCM to Longitudinal Balance		200 Hz to 3.4 kHz	40	—	—	dB
Longitudinal Impedance		200 Hz to 3.4 kHz at TIP or RING	—	50	—	Ω
Longitudinal Current per Pin		Active off-hook 200 Hz to 3.4 kHz	—	—	30	mApk
DC Current		V_{TR} = 0 V	—	—	45	mA
2-Wire Return Loss		200 Hz to 3.4 kHz	26	30	—	dB
Transhybrid Balance		300 Hz to 3.4 kHz	26	30	—	dB
Thermal Resistance (QFN-40)	θ_{JA}		—	32	—	°C/W
Continuous Power Dissipation (QFN-40)	P_D	T_A = 85 °C	—	1.7	—	W

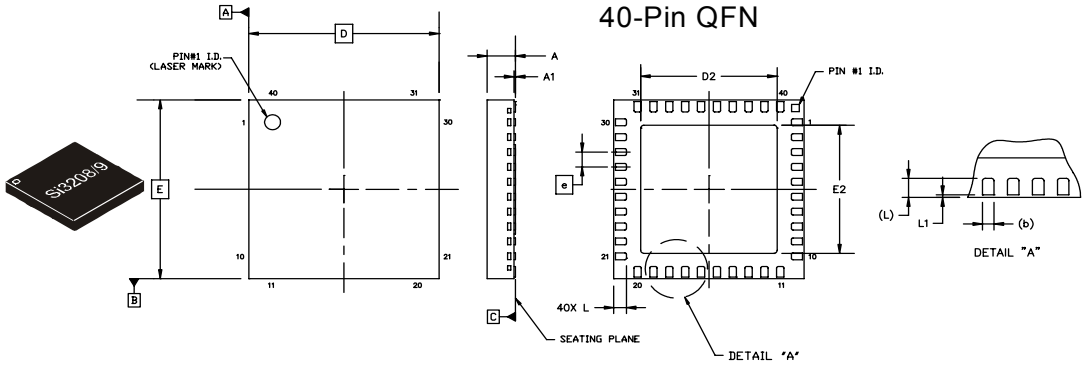
Package Information

64-Pin TQFP



	MM		
	Min	Typ	Max
A	—	—	1.20
b	0.17	0.22	0.27
D		12.00 BSC	
D1		10.00 BSC	
e		0.50 BSC	
E		12.00 BSC	
E1		10.00 BSC	

40-Pin QFN



	MM		
	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.10	4.30	4.40
e		0.50 BSC	
E		6.00 BSC	
E2	4.10	4.30	4.40
L	0.30	0.40	0.50
L1	0.03	0.05	0.08