

## SWITCHING REGULATOR APPLICATIONS

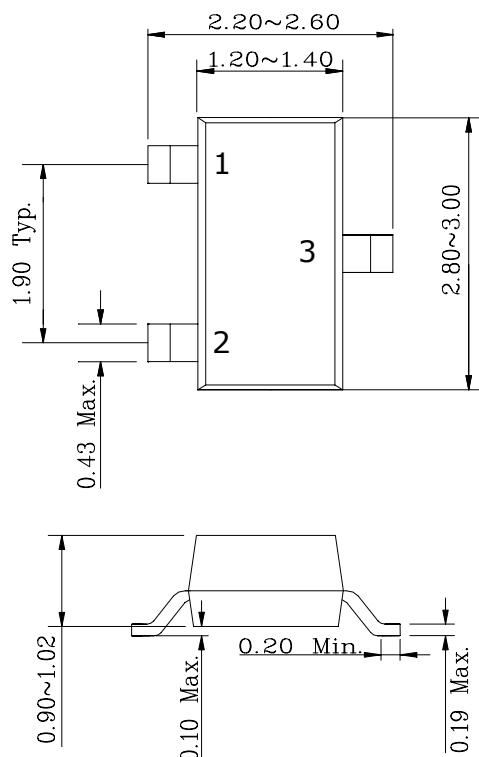
### Features

- High Voltage:  $BV_{DSS}=60V$ (Min.)
- Low  $C_{rss}$  :  $C_{rss}=3.1\text{pF}$ (Typ.)
- Low gate charge :  $Q_g=2.8\text{nC}$ (Typ.)
- Low  $R_{DS(on)}$  :  $R_{DS(on)}=2.8\Omega$ (Typ.)

### Ordering Information

Type NO.	Marking	Package Code
STK7002B	72B	SOT-23

### Outline Dimensions

**unit : mm**


**PIN Connections**  
1. Gate  
2. Source  
3. Drain

**Absolute maximum ratings**

(Ta=25°C)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V <sub>DSS</sub>	60	V
Gate-source voltage	V <sub>GSS</sub>	±20	V
Drain current (DC)	I <sub>D</sub>	(T <sub>c</sub> =25°C)	380
		(T <sub>c</sub> =100°C)	240
Drain current (Pulsed) *	I <sub>DP</sub>	1.52	A
Drain Power dissipation **	P <sub>D</sub>	350	mW
Avalanche current (Single) ②	I <sub>AS</sub>	380	mA
Single pulsed avalanche energy ②	E <sub>AS</sub>	3.8	mJ
Avalanche current (Repetitive) ①	I <sub>AR</sub>	380	mA
Repetitive avalanche energy ①	E <sub>AR</sub>	0.1	mJ
Junction temperature	T <sub>J</sub>	150	°C
Storage temperature range	T <sub>stg</sub>	-55~150	

\* Limited by maximum junction temperature

\*\* Device mounted on 99.5% Alumina 10 x 8 x 0.6mm

Characteristic	Symbol	Typ.	Max	Unit
Thermal resistance	R <sub>th(J-a)</sub>	-	357	°C/W

## Electrical Characteristics

(Ta=25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV <sub>DSS</sub>	I <sub>D</sub> =10μA, V <sub>GS</sub> =0	60	-	-	V
Gate-threshold voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250μA, V <sub>DS</sub> = V <sub>GS</sub>	1.0	-	2.5	V
Drain-source leakage current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	-	-	±100	nA
Drain-Source on-resistance ④	R <sub>DS(ON)</sub>	V <sub>GS</sub> =5V, I <sub>D</sub> =50mA	-	2.8	4.2	Ω
	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =180mA		2.7	4.0	
Forward transfer admittance ④	g <sub>fs</sub>	V <sub>DS</sub> =3V, I <sub>D</sub> =180mA	-	353		mS
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz	-	20	30	pF
Output capacitance	C <sub>oss</sub>		-	7.8	11.7	
Reverse transfer capacitance	C <sub>rss</sub>		-	3.1	4.7	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V I <sub>D</sub> =380mA, R <sub>G</sub> =25Ω	-	7	10.5	ns
Turn-off delay time	t <sub>d(off)</sub>		-	11	16.5	
Total gate charge	Q <sub>g</sub>	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V I <sub>D</sub> =380mA	-	2.8	4.2	nC
Gate-source charge	Q <sub>gs</sub>		-	0.4	0.6	
Gate-drain charge	Q <sub>gd</sub>		-	0.2	0.3	

## Source-Drain Diode Ratings and Characteristics

(Ta=25°C)

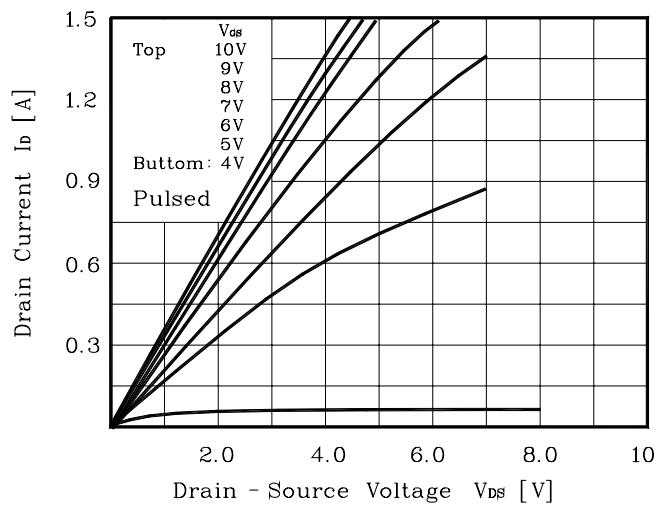
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Continuous source current	I <sub>S</sub>	Integral reverse diode in the MOSFET	-	-	380	mA
Source current (Pulsed) ①	I <sub>SM</sub>		-	-	1520	
Forward voltage ④	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =0.38A	-	-	1.4	V
Reverse recovery time	t <sub>rr</sub>	I <sub>s</sub> =380mA, V <sub>GS</sub> =0V dI <sub>s</sub> /dt=10A/us	-	39	-	ns
Reverse recovery charge	Q <sub>rr</sub>		-	10	-	uC

Note :

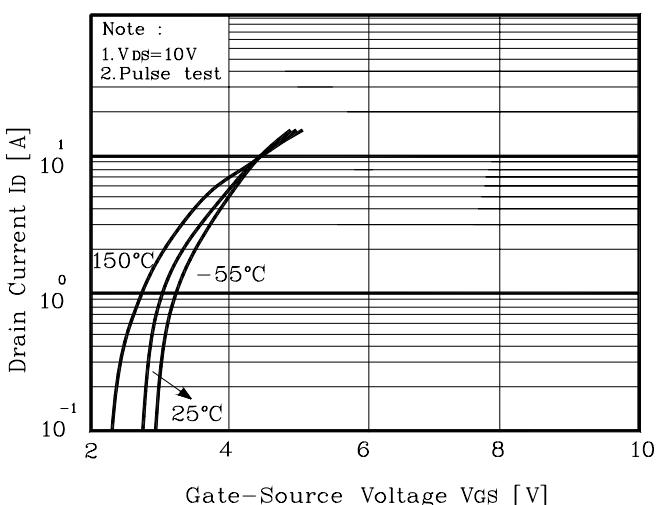
- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=10mH, I<sub>AS</sub>=0.38A, V<sub>DD</sub>=20V, R<sub>G</sub>=25Ω
- ③ Pulse Test : Pulse Width < 300us, Duty cycle≤ 2%
- ④ Essentially independent of operating temperature

## Electrical Characteristic Curves

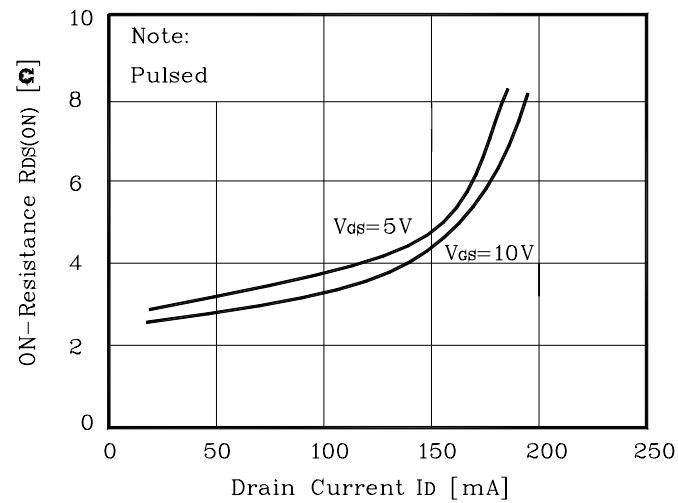
**Fig. 1  $I_D$  -  $V_{DS}$**



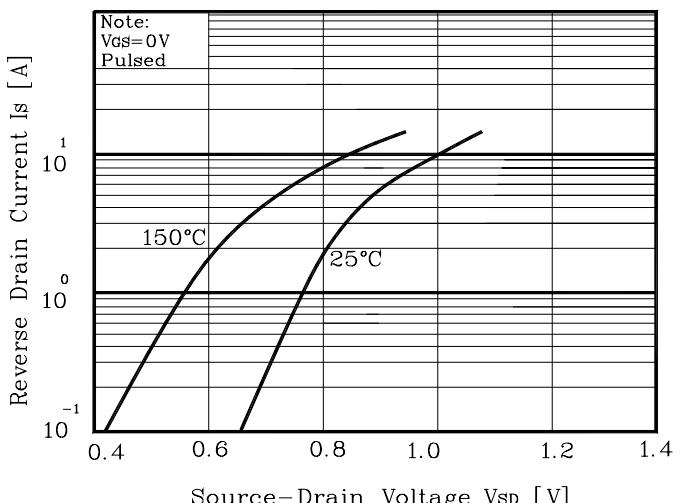
**Fig. 2  $I_D$  -  $V_{GS}$**



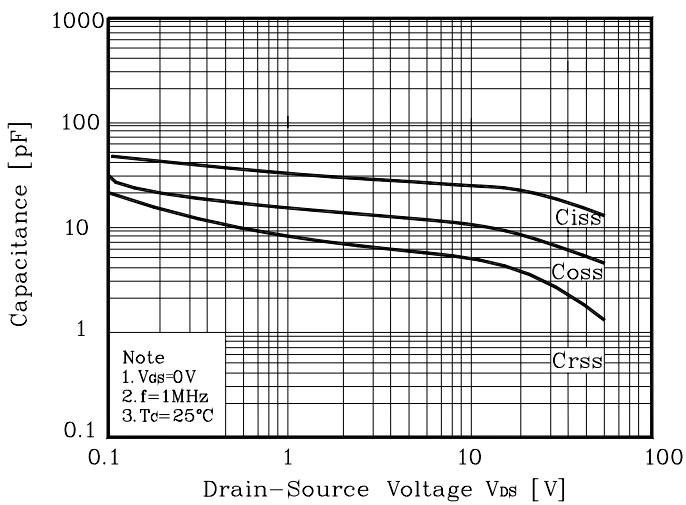
**Fig. 3  $R_{DS(on)}$  -  $I_D$**



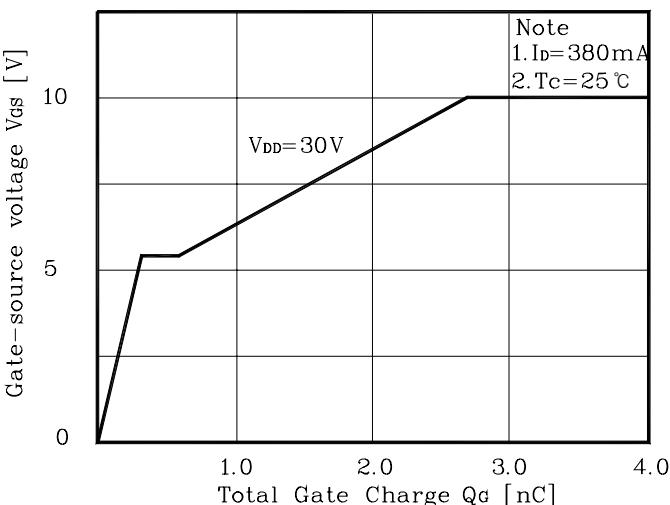
**Fig. 4  $I_S$  -  $V_{SD}$**



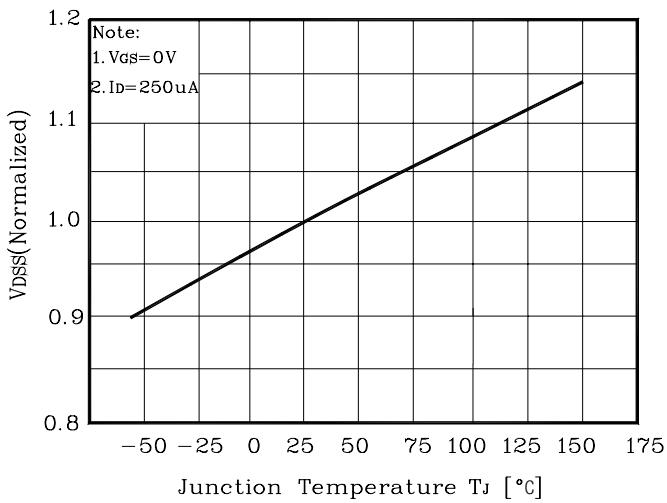
**Fig. 5 Capacitance -  $V_{DS}$**



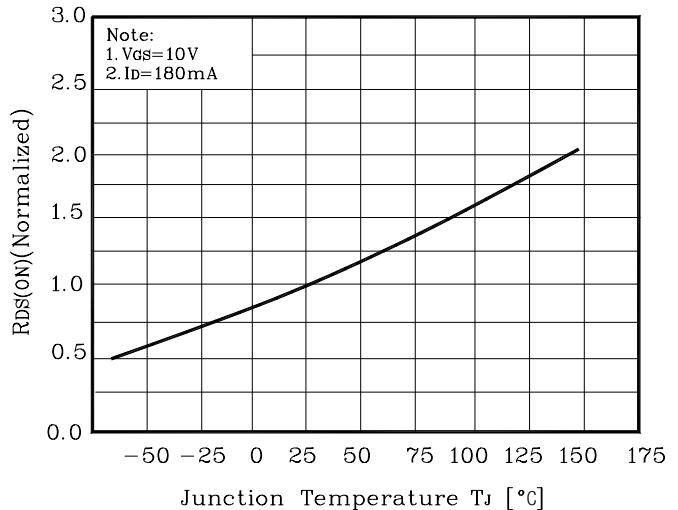
**Fig. 6  $V_{GS}$  -  $Q_G$**



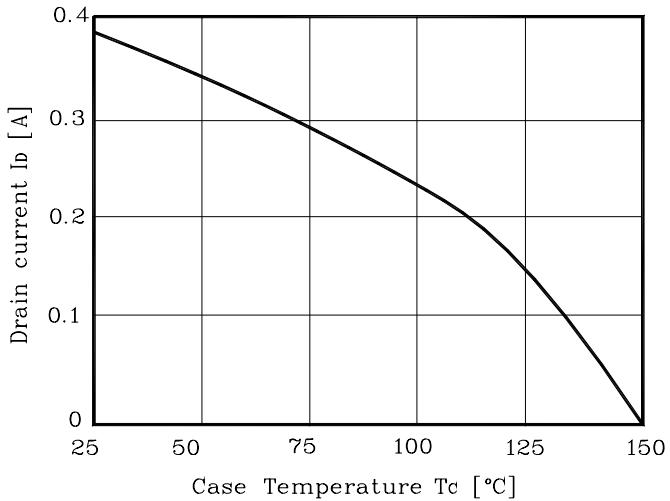
**Fig. 7  $V_{DSS}$  -  $T_J$**



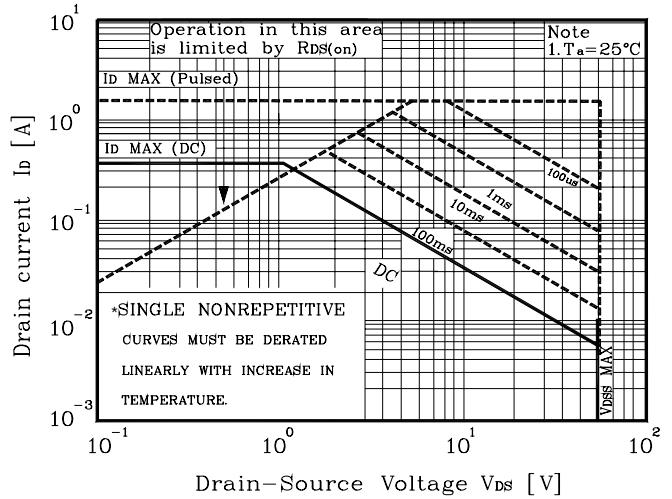
**Fig. 8  $R_{DS(on)}$  -  $T_J$**



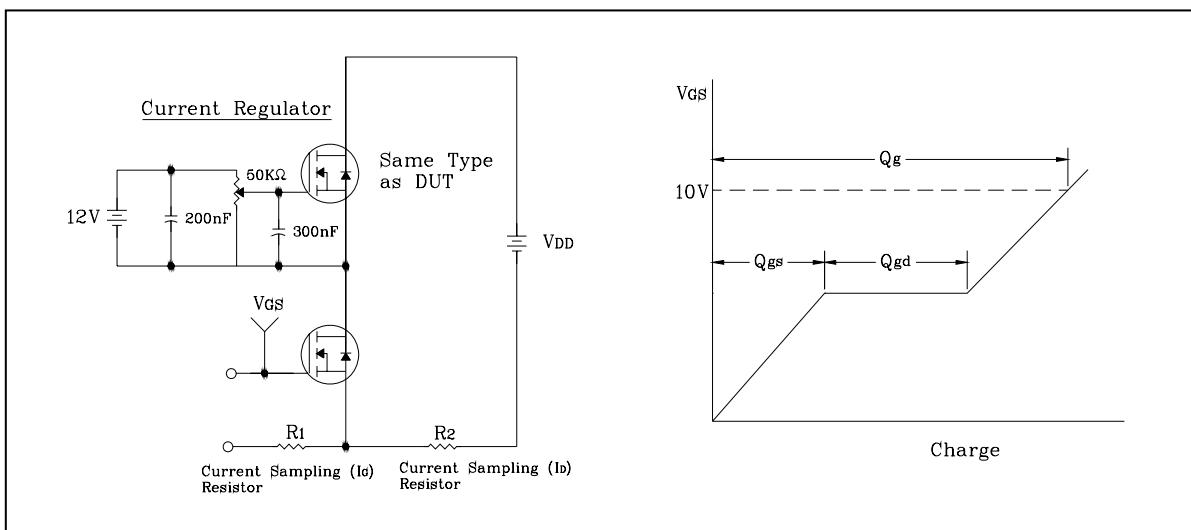
**Fig. 9  $I_D$  -  $T_C$**



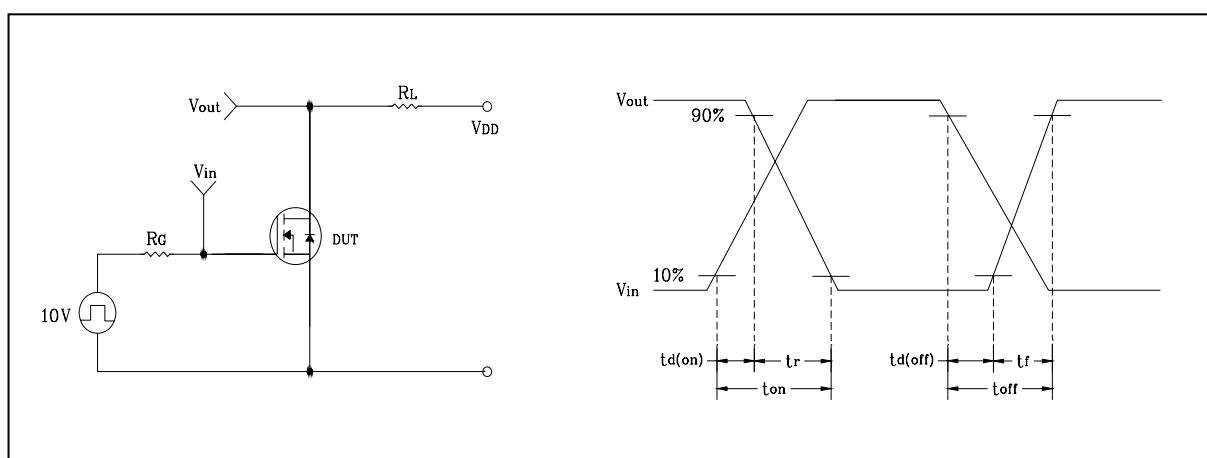
**Fig. 10 Safe Operating Area**



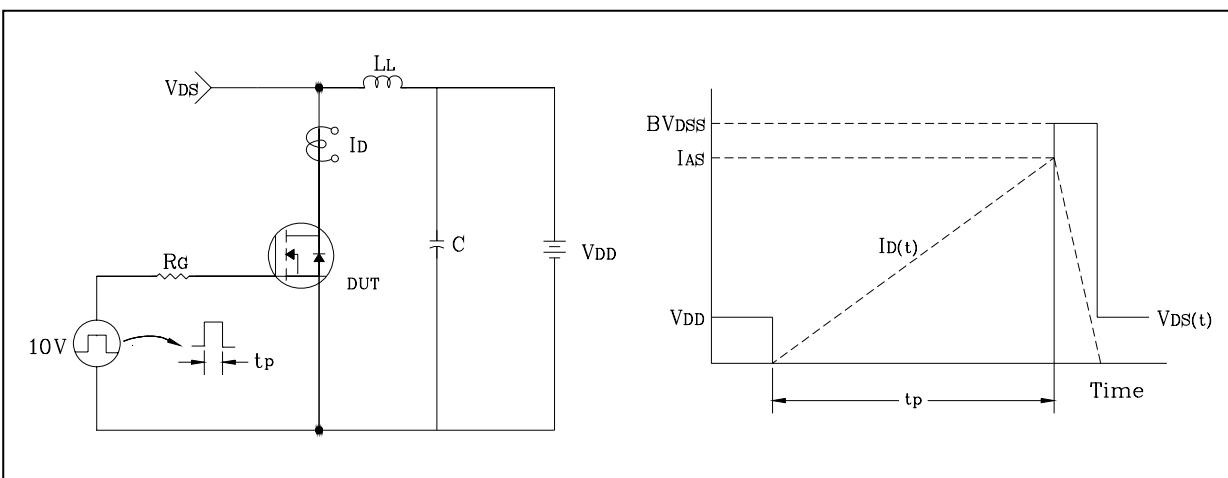
**Fig. 11 Gate Charge Test Circuit & Waveform**



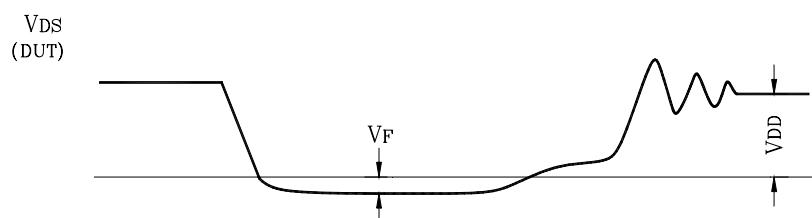
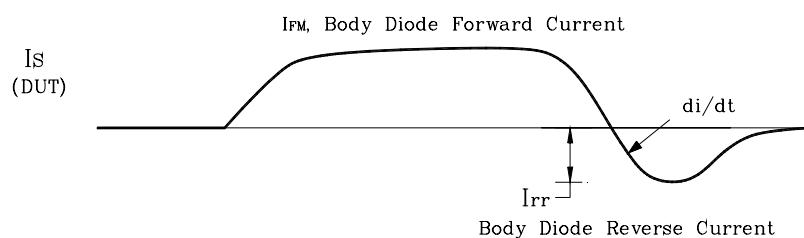
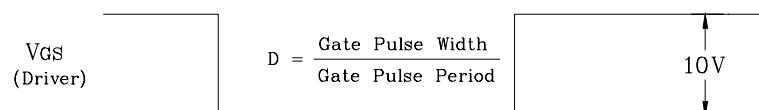
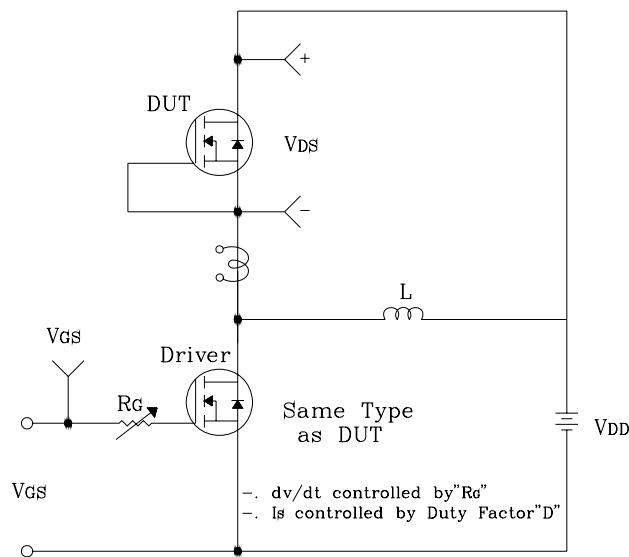
**Fig. 12 Resistive Switching Test Circuit & Waveform**



**Fig. 13 E<sub>AS</sub> Test Circuit & Waveform**



**Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform**



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