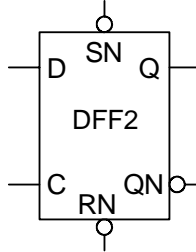


DFF2 is a fast, static, master-slave D flip-flop with 2x drive strength. SET and RESET are asynchronous and active low.

Truth Table

SN	RN	D	C	Q	QN
L	H	X	X	H	L
H	L	X	X	L	H
H	H	H	↑	H	L
H	H	L	↑	L	H
H	H	X	↓	no change	
L	L	X	X	illegal	



Capacitance

	Ci (pF)
D	0.020
C	0.020
SN	0.034
RN	0.041

Area

2.30 mils²

Power

7.19 μW/MHz

Delay [ns] = tpd.. = f(SL, L)

with SL = Input Slope [ns] ; L = Output Load [pF]

Output Slope [ns] = op_sl.. = f(L)

with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.2	L = 1.4	L = 2.0	L = 0.2	L = 1.4	L = 2.0
Delay C to Q	tpdcqr	0.88	1.84	2.29	1.04	2.00	2.46
	tpdcqf	0.80	1.71	2.15	0.96	1.88	2.31
Delay C to QN	tpdcqnr	1.20	2.14	2.65	1.37	2.31	2.82
	tpdcqnf	1.18	2.09	2.54	1.35	2.25	2.70
Delay SN to Q	tpdsnq	0.88	1.83	2.32	1.20	2.18	2.65
Delay SN to QN	tpdsnqn	1.18	2.07	2.50	1.50	2.40	2.83
Delay RN to Q	tpdrnq	2.15	3.04	3.49	2.34	3.25	3.67
Delay RN to QN	tpdrnqn	0.95	1.88	2.33	1.27	2.22	2.67
Output Slope C to Q	op_slcqr	0.67	3.51	5.01	0.67	3.53	5.03
	op_slcqf	0.60	2.85	4.25	0.61	3.00	4.08
Output Slope C to QN	op_slcqnr	0.71	3.55	5.08	0.71	3.60	5.00
	op_slcqnf	0.58	2.93	4.03	0.56	2.93	4.03
Output Slope SN to Q	op_slsnq	0.73	3.70	5.11	0.71	3.63	5.25
Output Slope SN to QN	op_slsnqn	0.60	2.88	4.08	0.58	2.91	4.12
Output Slope RN to Q	op_slrnq	0.66	3.05	4.13	0.65	2.95	4.06
Output Slope RN to QN	op_slrnqn	0.70	3.48	5.12	0.70	3.58	5.11

Characteristics		Symbol	[ns]	Characteristics		Symbol	[ns]
Min D Setup Time to C	High	tsudch	0.16	Min D Hold Time to C	High	thdch	0.00
	Low	tsudcl	0.16		Low	thdcl	0.00
Min SN Setup Time to C	Low	tsusnc	0.00	Min SN Hold Time to C	Low	thsnc	0.51
Min RN Setup Time to C	Low	tsurnc	0.00	Min RN Hold Time to C	Low	thrnc	1.33
Min C Width	High	twch	0.48				
	Low	twcl	0.88				
Min SN Width	Low	twsn	1.07				
Min RN Width	Low	twrn	3.91				