EMIF02-USB03F2

IPAD™

2 LINES EMI FILTER INCLUDING ESD PROTECTION

PRODUCT CHARACTERISTICS
ESD protection and EMI filtering for:

■ USB OTG port

DESCRIPTION
The EMIF02-USB03F2 is a highly integrated array designed to suppress EMI / RFI noise for USB OTG (On The Go).
The EMIF02-USB03F2 Flip-Chip packaging means the package size is equal to the die size.
Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV on external contacts.

BENEFITS
■ 2 lines low-pass-filter + 2 lines ESD protection
■ High efficiency in EMI filtering
■ Lead Free package
■ Very low PCB space consuming: < 3.25 mm^2
■ Very thin package: 0.65 mm
■ High efficiency in ESD suppression (IEC61000-4-2 level 4)
■ High reliability offered by monolithic integration
■ High reducing of parasitic elements through
■ integration and wafer level packaging.

COMPLIES WITH THE FOLLOWING STANDARDS:
IEC61000-4-2
Level 4 on external pins 15kV (air discharge)
                          8kV (contact discharge)

Level 1 on internal pins 2kV (air and contact discharge)

**Flip-Chip
(11 Bumps)**

Figure 1: Pin Configuration (ball side)

Figure 2: Schematic

Table 1: Order Code

Part Number	Marking
EMIF02-USB03F2	FU

TM: IPAD is a trademark of STMicroelectronics.
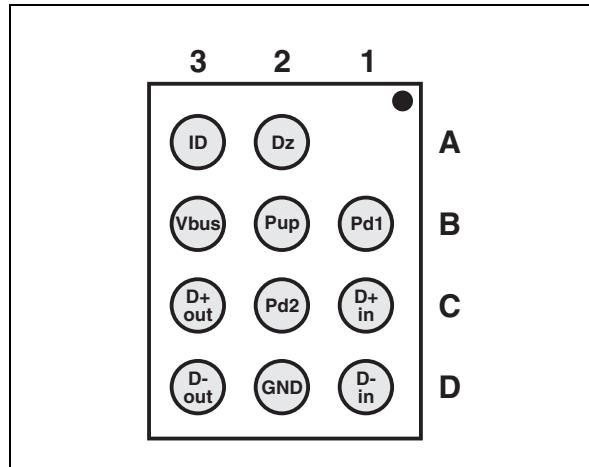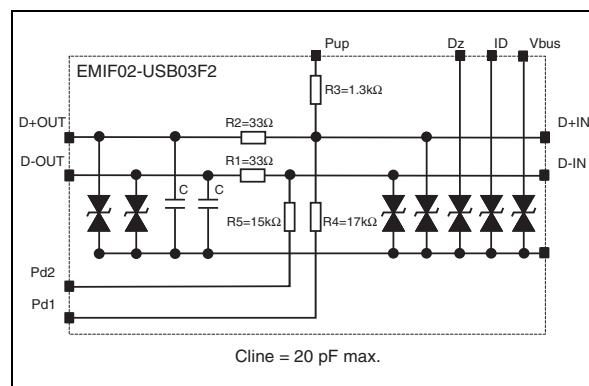
Table 2: Absolute Ratings ($T_{amb} = 25°C$))

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	External pins (D1, C1, A2, A3, B3) ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge Internal pins (D3, C3, C2, B2, B1) ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharg	15 8 2 2	kV
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 3: Electrical Characteristics ($T_{amb} = 25°C$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
Rd	Dynamic impedance
I_{PP}	Peak pulse current
C_{line}	Input line capacitance per line
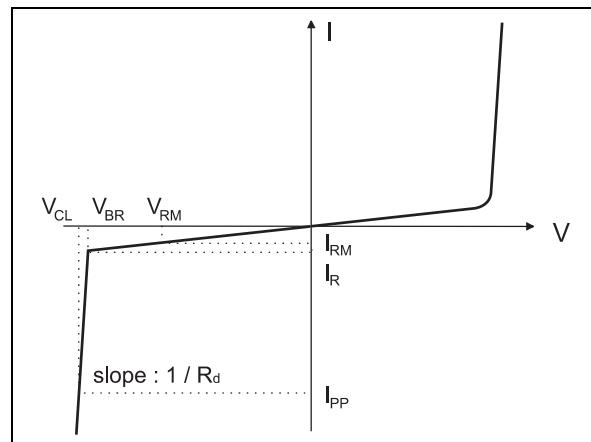
Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1$ mA	14			V
I_{RM}	$V_{RM} = 3V$		0.1	0.5	µA
C_{line}	@ 0V			20	pF
R_1, R_2	Tolerance ± 5%		33		Ω
R_3	Tolerance ± 5%		1.30		kΩ
R_4	Tolerance ± 5%		17		kΩ
R_5	Tolerance ± 5%		15		kΩ

**Figure 3: Application Schematic**
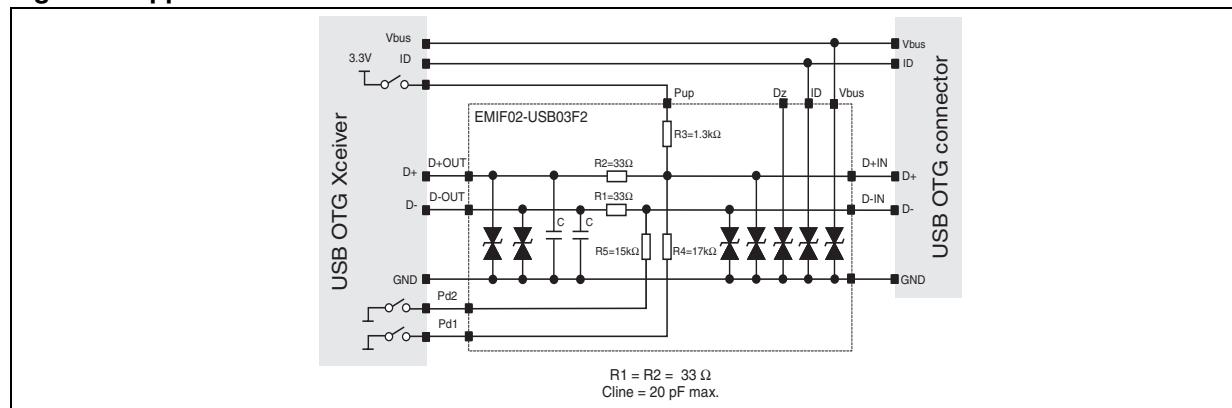
Figure 4: Filtering measurements
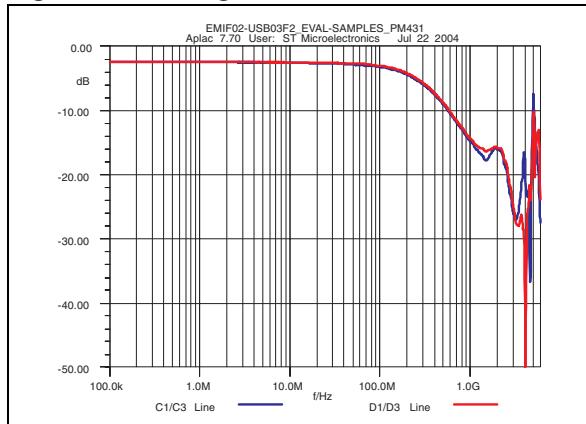
**Figure 5: Analog crosstalk measurements**
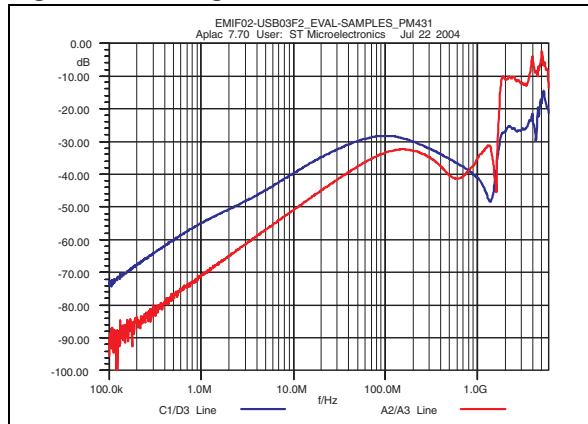
Figure 6: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout)
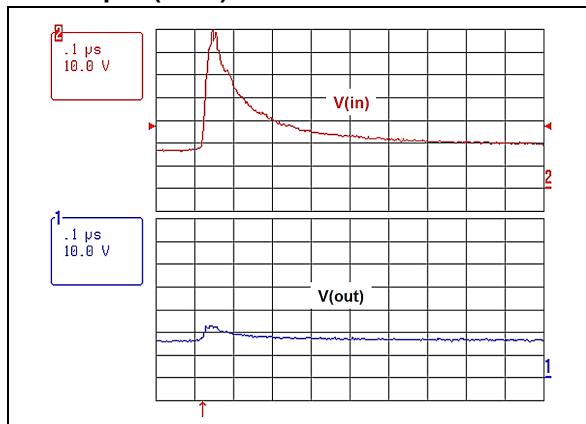

Figure 7: ESD response to IEC61000-4-2 (-15kV air discharge) on one input V(in) and on one output (Vout)
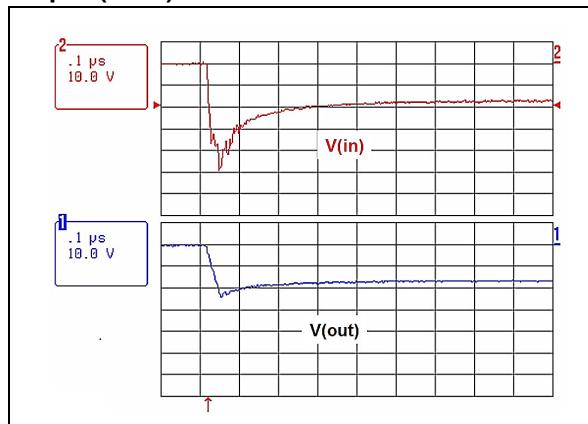

**Figure 8: Junction capacitance versus reverse voltage applied (typical values)**
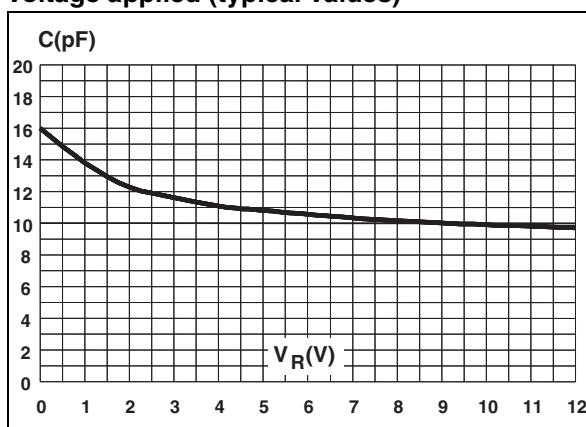
Figure 9: Aplac model
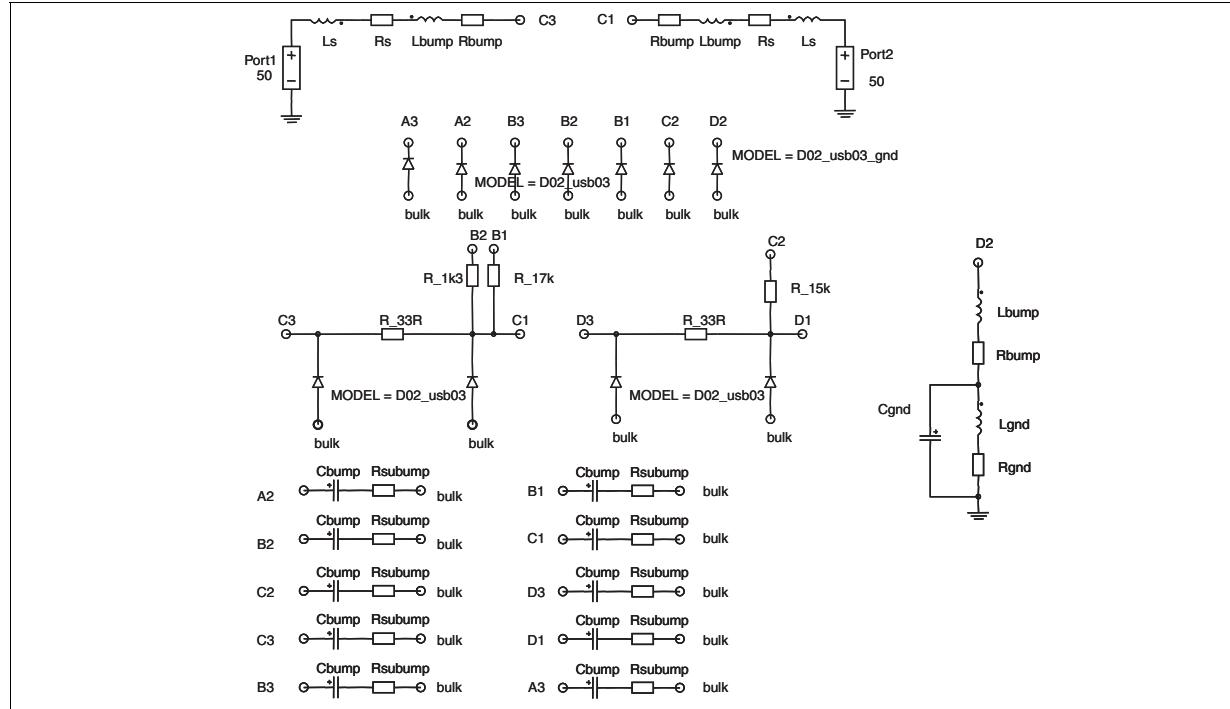
Figure 10: Aplac parameters

Ls 950pH	Rs_usb03_gnd 0.9
Rs 150m	Lgnd 50pH
R_33R 33	Rgnd 100m
R_1k3 1.3k	Cgnd 0.15pF
R_15k 15k	Lbump 50pH
R_17k 17k	Rbump 20m
Cz_usb03 11pF	Cbump 2.4pF
Rs_usb03 1	Rsubump 100m
Cz_usb03_gnd 220pF	

Figure 11: Order Code

EMIF yy - xxx zz Fx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10(pF)
or
3 letters = application
2 digits = version

Package
F = Flip-Chip
x = 1: 500µm, Bump = 315µm
   = 2: Leadfree Pitch = 500µm, Bump = 315µm
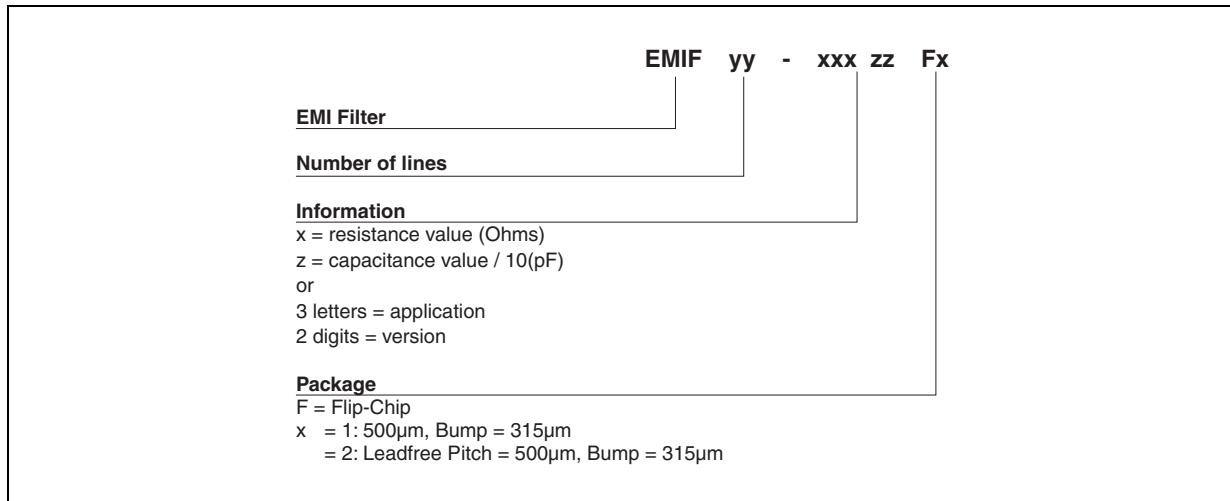
Figure 12: FLIP-CHIP Package Mechanical Data
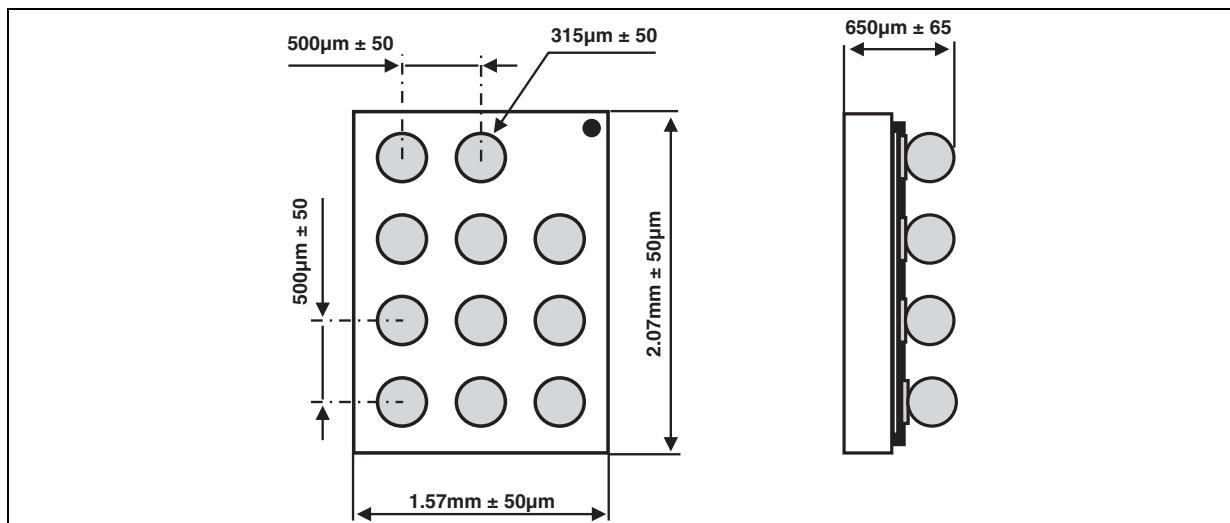
Figure 14: Foot Print Recommendations

Copper pad Diameter :
250µm recommended, 300µm max.

Solder stencil opening :
330µm recommended

Solder mask opening recommendation :
340µm min. for 300µm copper pad diameter

Figure 15: Marking

Dot, ST logo
xx = marking
z = packaging location
yww = datecode
(y = year
ww = week)

All dimensions in µm

Figure 14: Packing

Dot identifying Pin A1 location

4 +/- 0.1

Ø 1.5 +/- 0.1

1.75 +/- 0.1

3.5 +/- 0.1

8 +/- 0.3

0.73 +/- 0.05

4 +/- 0.1

All dimensions in mm
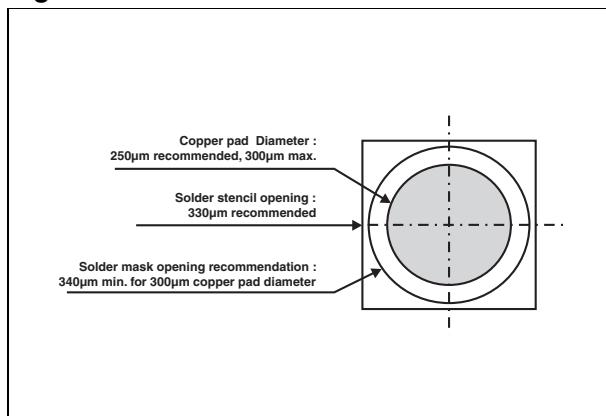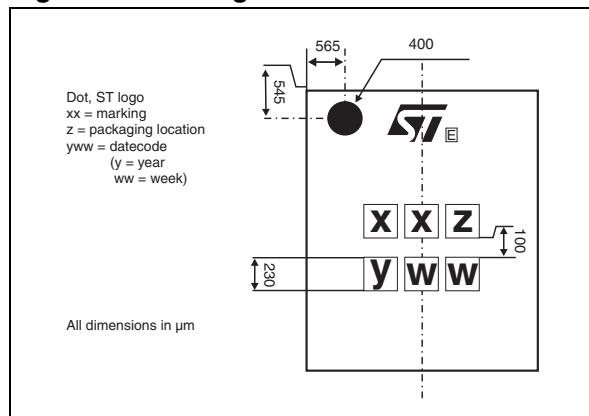
User direction of unreeling
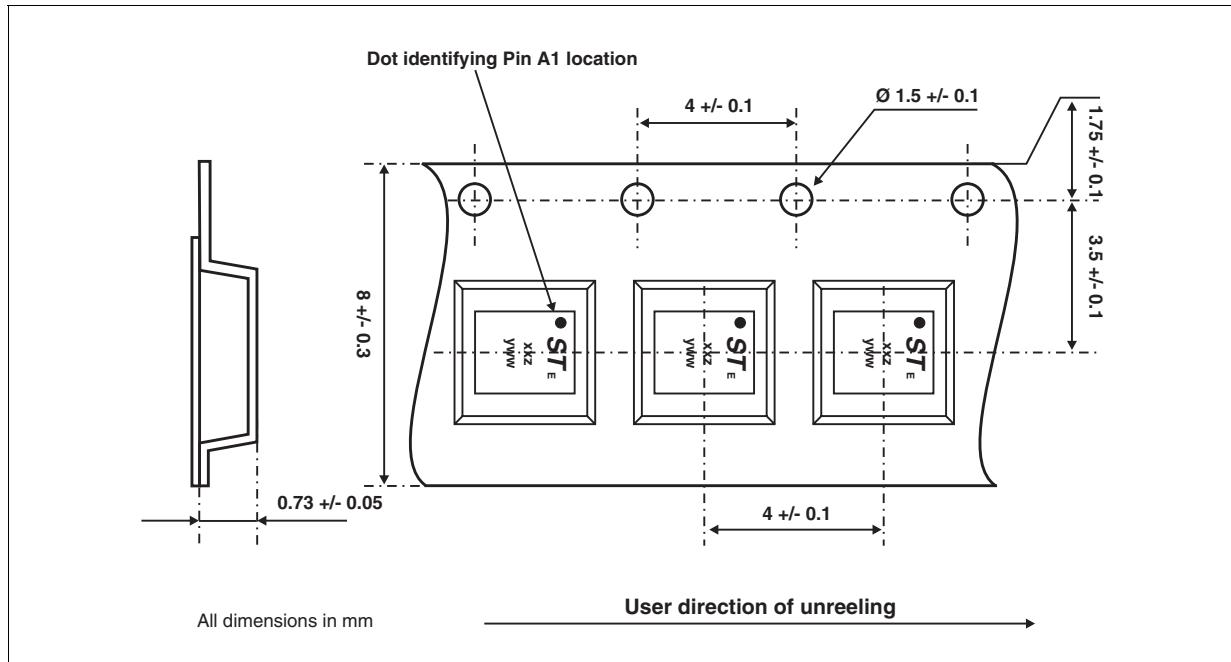
Table 4: Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-USB03F2	FU	Flip-Chip	4.5 mg	5000	Tape & reel 7"

Note: More packing informations are available in the application note
AN1235: "Flip-Chip: Package description and recommendations for use"
AN1751: "EMI Filters: Recommendations and measurements"

Table 5: Revision History

Date	Revision	Description of Changes
14-Oct-2004	1	First issue.
25-Oct-2004	2	Figure 13 on page 5: Flip-Chip marking dimensions updated.
27-Oct-2004	3	Minor layout update. No content change.

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