



FP203

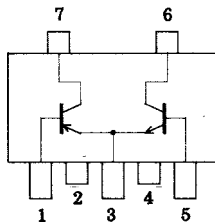
PNP/NPN Epitaxial Planar Silicon Transistors

Push-Pull Circuits

Features

- Composite type with 2 transistors of PNP transistor and NPN transistor, facilitating high-density mounting.
- The FP203 is formed with chips, being equivalent to the 2SB1122 and 2SD1622, placed in one package.

Electrical Connection

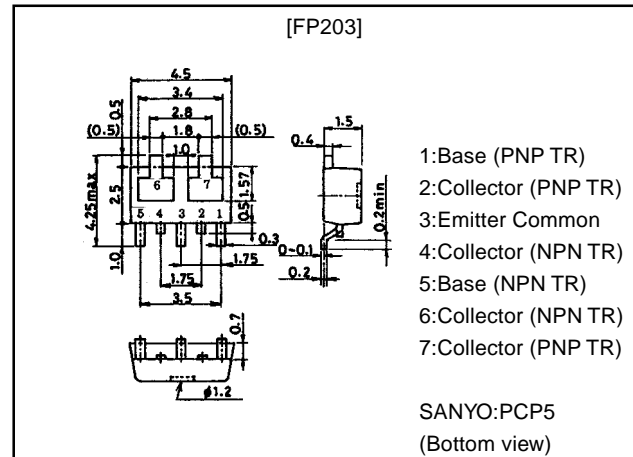


- 1:Base (PNP TR)
 2:Collector (PNP TR)
 3:Emitter Common
 4:Collector (NPN TR)
 5:Base (NPN TR)
 6:Collector (NPN TR)
 7:Collector (PNP TR)
 (Top view)

Package Dimensions

unit:mm

2097A



Specifications

Absolute Maximum Ratings at Ta = 25°C

() : PNP

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CB0}		(-)60	V
Collector-to-Emitter Voltage	V_{CEO}		(-)50	V
Emitter-to-Base Voltage	V_{EBO}		(-)5	V
Collector Current	I_C		(-)1	A
Collector Current (Pulse)	I_{CP}		(-)2	A
Base Current	I_B		(-)0.2	A
Collector Dissipation	P_C	Mounted on ceramic board (250mm ² ×0.8mm) 1unit	0.75	W
Total Dissipation	P_T	Mounted on ceramic board (250mm ² ×0.8mm)	1.0	W
Junction Temperature	T_j		150	°C
Storage Temperature	T_{stg}		-55 to +150	°C

Electrical Characteristics at Ta=25°C

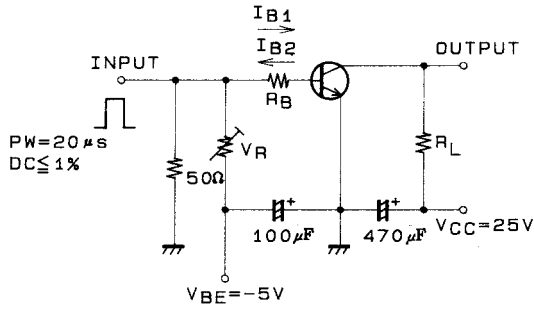
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	$V_{CB} = (-)50V, I_E = 0$			(-)100	nA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = (-)4V, I_C = 0$			(-)100	nA
DC Current Gain	h_{FE}	$V_{CE} = (-)2V, I_C = (-)100mA$	140		400	
Gain-Bandwidth Product	f_T	$V_{CE} = (-)10V, I_C = (-)50mA$		150		MHz
Output Capacitance	C_{ob}	$V_{CB} = (-)10V, f = 1MHz$		(12)		pF
C-E Saturation Voltage	$V_{CE(sat)}$	$I_C = (-)500mA, I_B = (-)50mA$		(-180)	(-400)	mV
B-E Saturation Voltage	$V_{BE(sat)}$	$I_C = (-)500mA, I_B = (-)50mA$		(-)0.9	(-)1.2	V
C-B Breakdown Voltage	$V_{(BR)CBO}$	$I_C = (-)10\mu A, I_E = 0$	(-)60			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	$I_C = (-)1mA, R_{BE} = \infty$	(-)50			V
E-B Breakdown Voltage	$V_{(BR)EBO}$	$I_E = (-)10\mu A, I_C = 0$	(-)5			V
Turn-ON Time	t_{on}	See specified Test Circuit		40		ns
Storage Time	t_{stg}	See specified Test Circuit		(300) 350		ns
Fall Time	t_f	See specified Test Circuit		30		ns

Marking:203

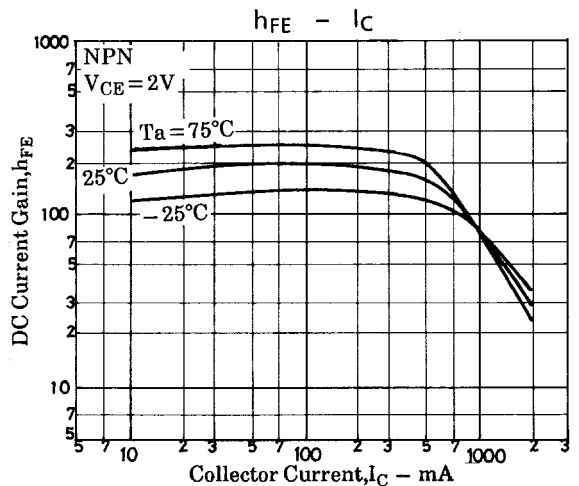
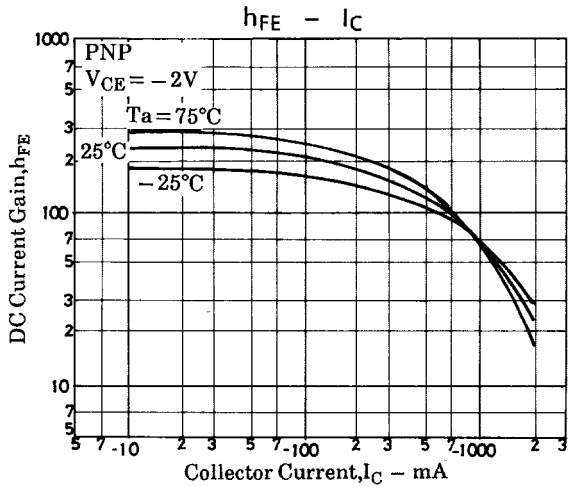
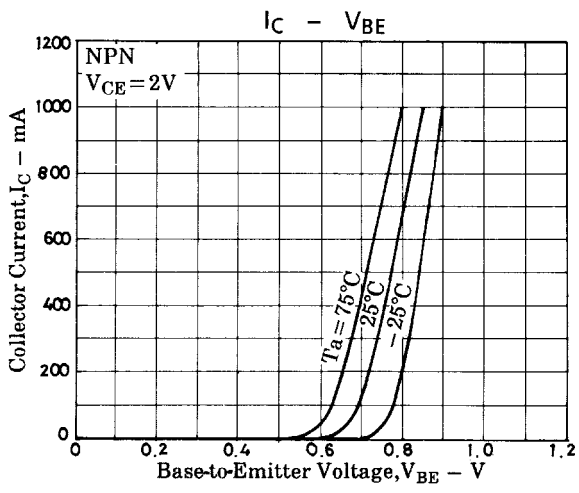
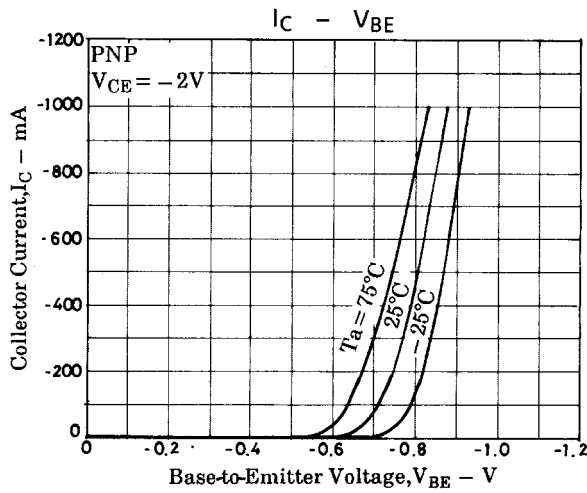
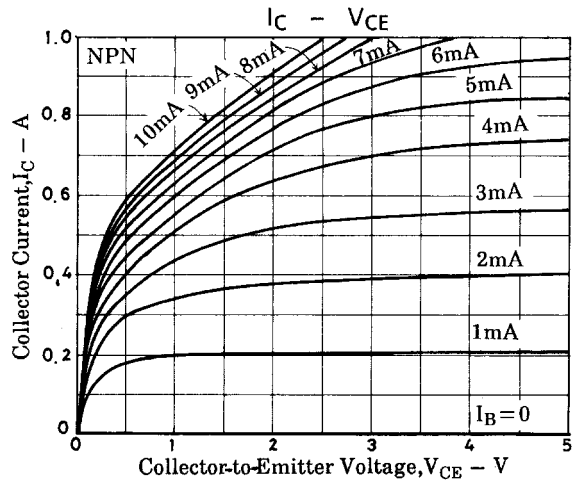
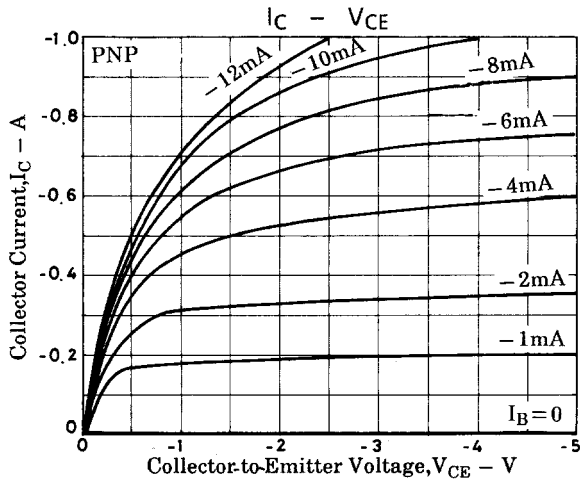
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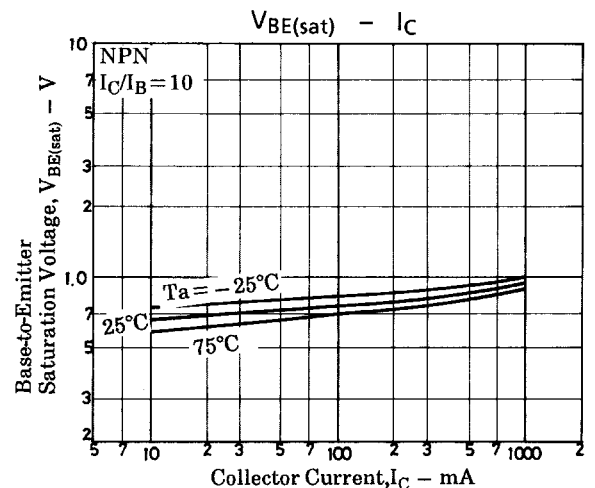
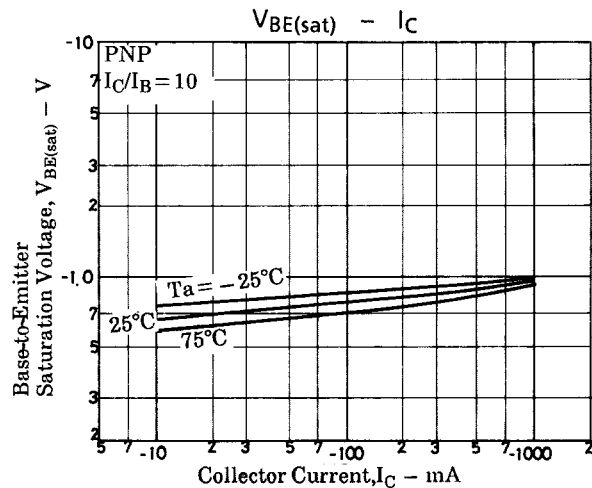
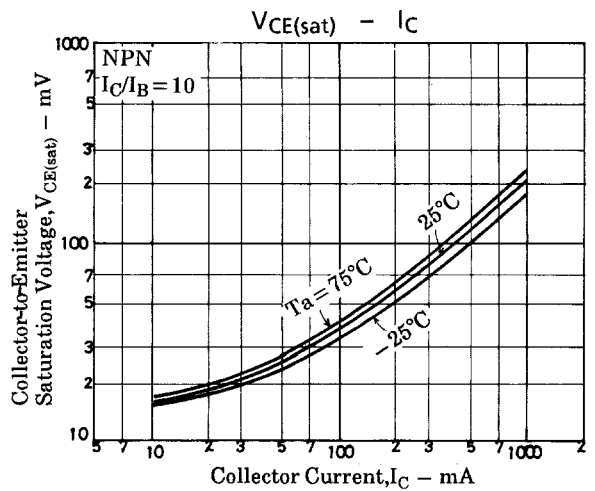
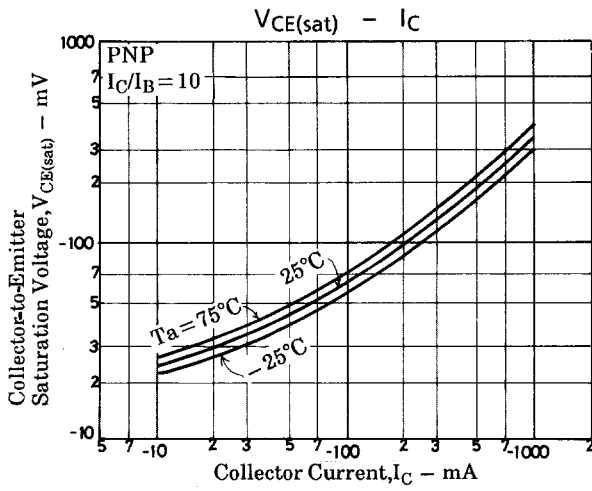
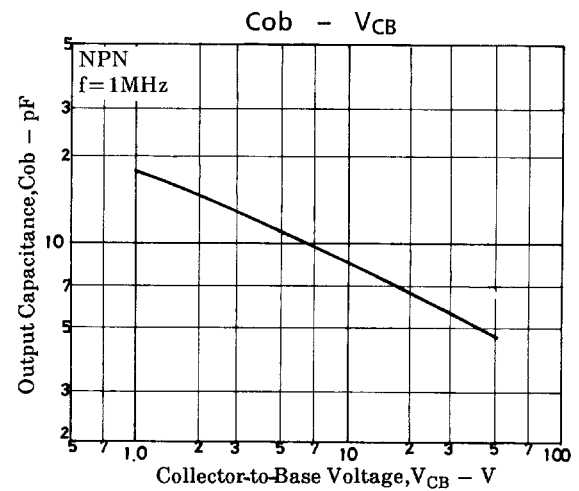
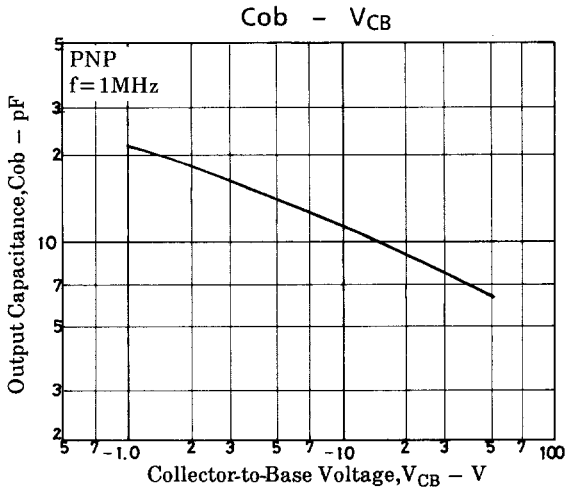
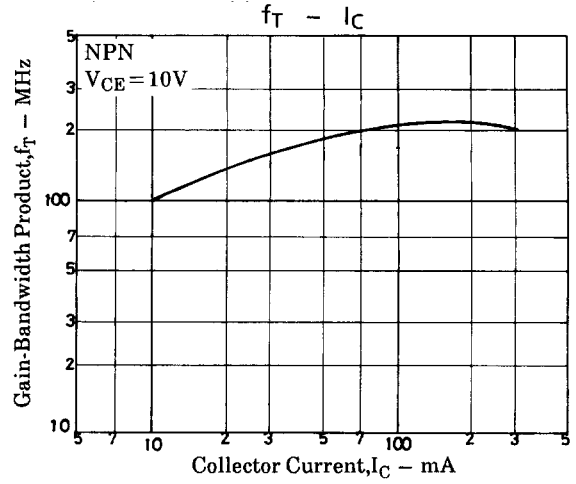
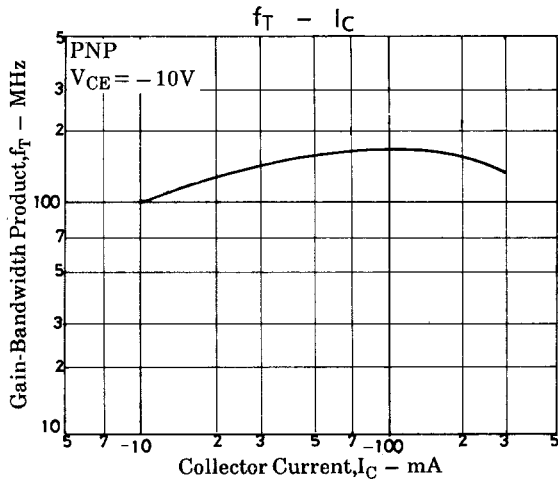
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Switching Time Test Circuit

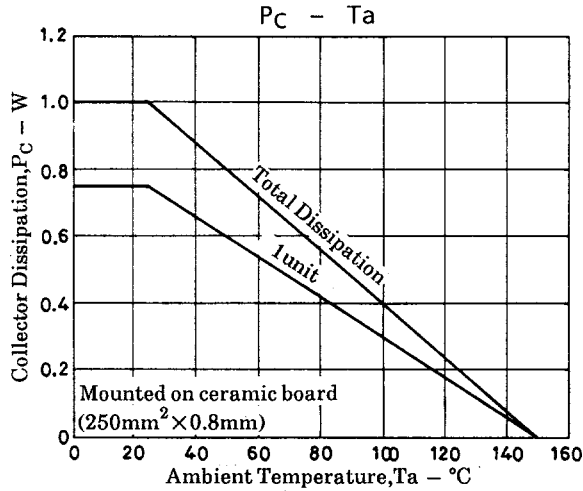
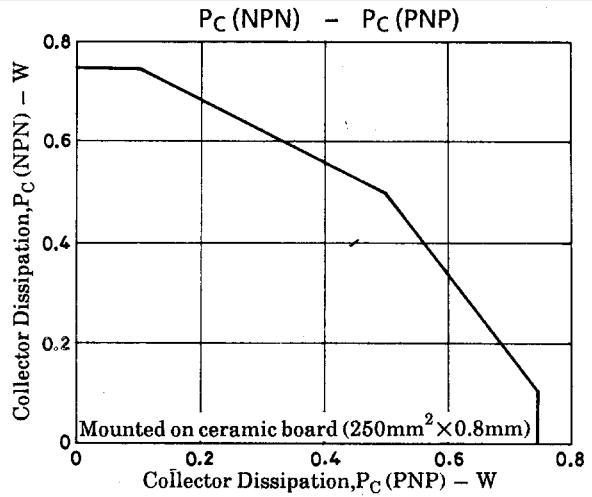
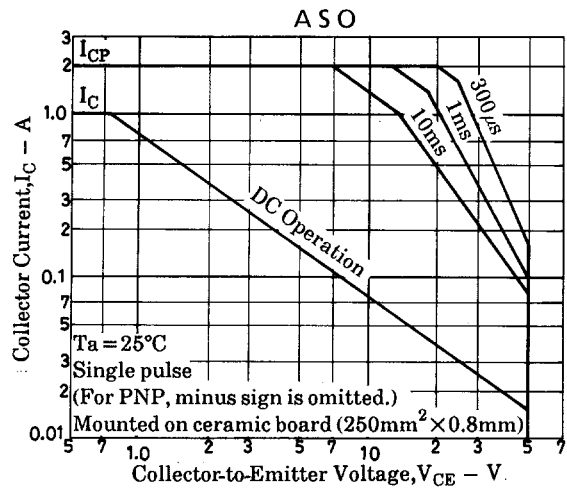


$10I_{B1} = -10I_{B2} = I_C = 500\text{mA}$
 For PNP, the polarity is reversed.





FP203



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