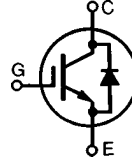


Preliminary data

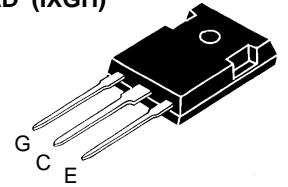
Low $V_{CE(sat)}$ High speed IGBT with Diode

IXGH25N100U1
IXGH25N100AU1

V_{CES}	I_{C25}	$V_{CE(sat)}$
1000 V	50 A	3.5 V
1000 V	50 A	4.0 V



TO-247 AD (IXGH)



G = Gate C = Collector
E = Emitter TAB = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ\text{C}$ to 150°C	1000	V
V_{CGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GE} = 1\text{ M}\Omega$	1000	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ\text{C}$	50	A
I_{C90}	$T_C = 90^\circ\text{C}$	25	A
I_{CM}	$T_C = 25^\circ\text{C}$, 1 ms	100	A
SSOA (RBSOA)	$V_{GE} = 15\text{ V}$, $T_{VJ} = 125^\circ\text{C}$, $R_G = 33\ \Omega$ Clamped inductive load, $L = 100\ \mu\text{H}$	$I_{CM} = 50$ @ $0.8 V_{CES}$	A
P_C	$T_C = 25^\circ\text{C}$	200	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
M_d	Mounting torque (M3)	1.13/10	Nm/lb.in.
Weight		TO-204 = 18 g, TO-247 = 6 g	
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	$^\circ\text{C}$

Features

- International standard package JEDEC TO-247 AD
- IGBT and anti-parallel FRED in one package
- 2nd generation HDMOS™ process
- Low $V_{CE(sat)}$
 - for minimum on-state conduction losses
- MOS Gate turn-on
 - drive simplicity
- Fast Recovery Epitaxial Diode (FRED)
 - soft recovery with low I_{RM}

Applications

- AC motor speed control
- DC servo and robot drives
- DC choppers
- Uninterruptible power supplies (UPS)
- Switch-mode and resonant-mode power supplies

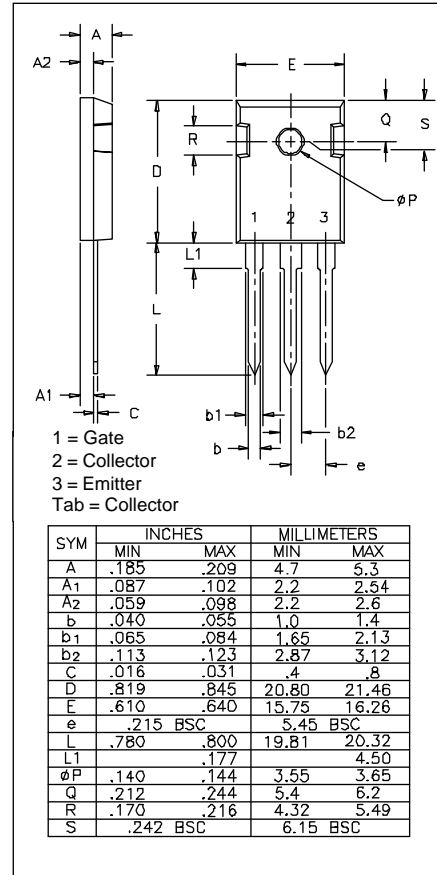
Advantages

- Saves space (two devices in one package)
- Easy to mount (isolated mounting screw hole)
- Reduces assembly time and cost

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
BV_{CES}	$I_C = 4.5\text{ mA}$, $V_{GE} = 0\text{ V}$	1000		V
$V_{GE(th)}$	$I_C = 500\ \mu\text{A}$, $V_{CE} = V_{GE}$	2.5		5.5 V
I_{CES}	$V_{CE} = 0.8 \cdot V_{CES}$ $V_{GE} = 0\text{ V}$			500 μA 8 mA
I_{GES}	$V_{CE} = 0\text{ V}$, $V_{GE} = \pm 20\text{ V}$			$\pm 100\text{ nA}$
$V_{CE(sat)}$	$I_C = I_{C90}$, $V_{GE} = 15\text{ V}$			25N100U1: 3.5 V 25N100AU1: 4.0 V

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
g_{fs}	$I_C = I_{C90}$; $V_{CE} = 10\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$	8	15	S
C_{ies} C_{oes} C_{res}	$V_{CE} = 25\text{ V}$, $V_{GE} = 0\text{ V}$, $f = 1\text{ MHz}$		2750	pF
			270	pF
			50	pF
Q_g Q_{ge} Q_{gc}	$I_C = I_{C90}$, $V_{GE} = 15\text{ V}$, $V_{CE} = 0.5 V_{CES}$		130	nC
			25	nC
			55	nC
$t_{d(on)}$ t_{ri} $t_{d(off)}$ t_{fi} E_{off}	Inductive load, $T_J = 25^\circ\text{C}$ $I_C = I_{C90}$, $V_{GE} = 15\text{ V}$, $L = 300\ \mu\text{H}$, $V_{CE} = 0.8 V_{CES}$, $R_G = R_{off} = 33\ \Omega$ Remarks: Switching times may increase for V_{CE} (Clamp) $> 0.8 \cdot V_{CES}$, higher T_J or increased R_G		100 200 500 500 5	ns ns ns ns mJ
$t_{d(on)}$ t_{ri} E_{on} $t_{d(off)}$ t_{fi} E_{off}	Inductive load, $T_J = 125^\circ\text{C}$ $I_C = I_{C90}$, $V_{GE} = 15\text{ V}$, $L = 300\ \mu\text{H}$, $V_{CE} = 0.8 V_{CES}$, $R_G = R_{off} = 33\ \Omega$ Remarks: Switching times may increase for V_{CE} (Clamp) $> 0.8 \cdot V_{CES}$, higher T_J or increased R_G		100 250 3.5 720 950 800 10 6	ns ns mJ ns ns ns mJ mJ
R_{thJC} R_{thCK}			0.25	0.62 K/W K/W

TO-247 AD Outline



Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_F	$I_F = I_{C90}$, $V_{GE} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			2.5 V
I_{RM} t_{tr}	$I_F = I_{C90}$, $V_{GE} = 0\text{ V}$, $-di_F/dt = 240\text{ A}/\mu\text{s}$ $V_R = 540\text{ V}$ $T_J = 125^\circ\text{C}$ $I_F = 1\text{ A}$; $-di/dt = 100\text{ A}/\mu\text{s}$; $V_R = 30\text{ V}$ $T_J = 25^\circ\text{C}$		16	18 A
			120	ns
			35	50 ns
R_{thJC}				1 K/W

IXYS reserves the right to change limits, test conditions, and dimensions.

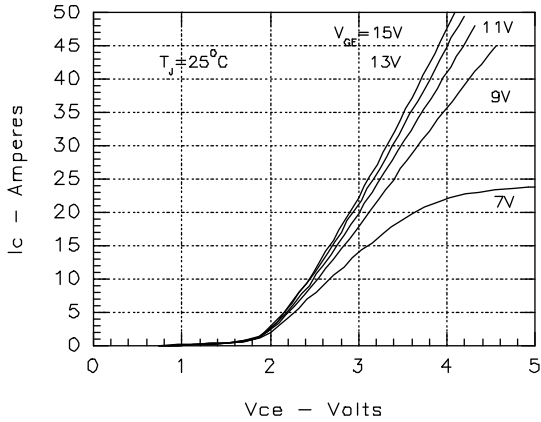
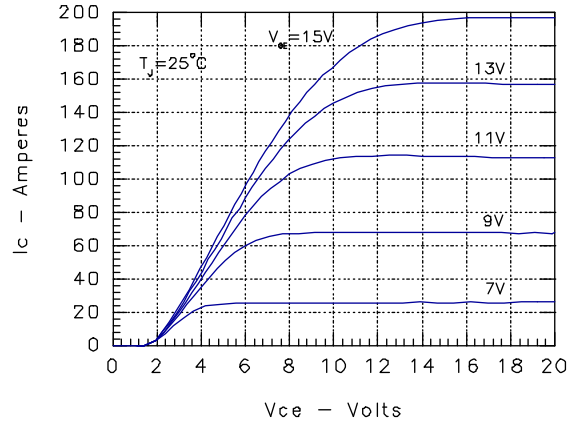
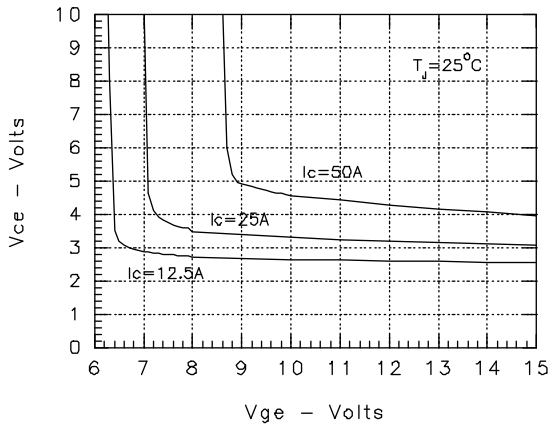
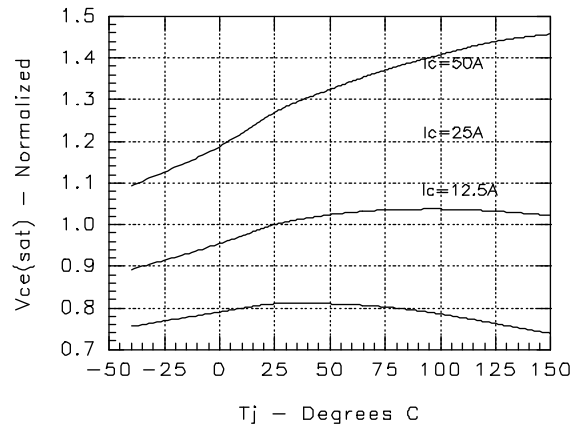
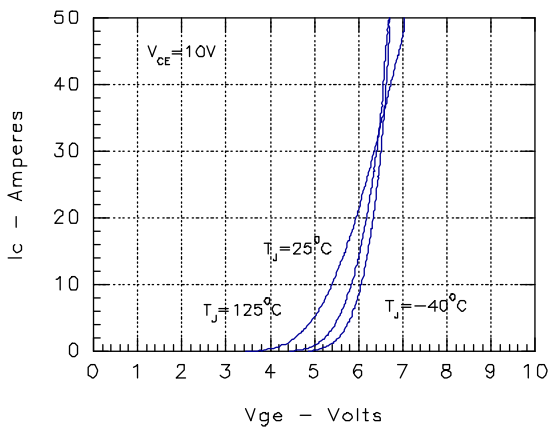
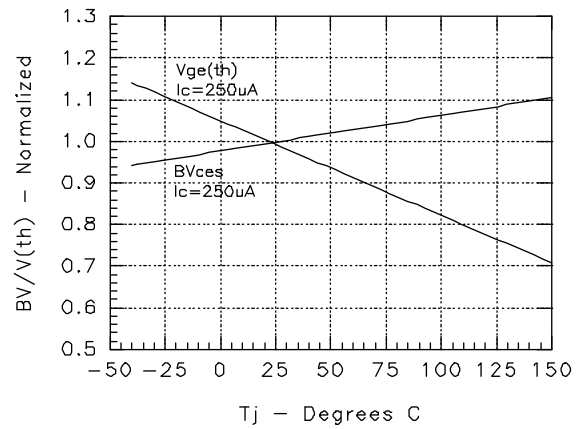
Fig. 1. Saturation Characteristics

Fig. 2. Output Characteristics

Fig. 3. Collector-Emitter Voltage vs. Gate-Emitter Voltage

Fig. 4. Temperature Dependence of Output Saturation Voltage

Fig. 5. Input Admittance

Fig. 6. Temperature Dependence Breakdown and Threshold Voltage


Fig. 7. Gate Charge

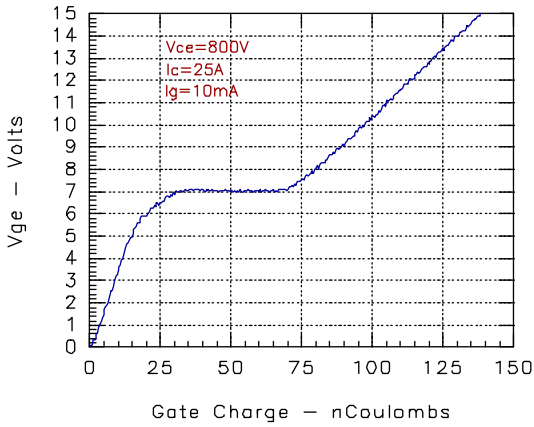


Fig. 8. Turn-Off Safe Operating Area

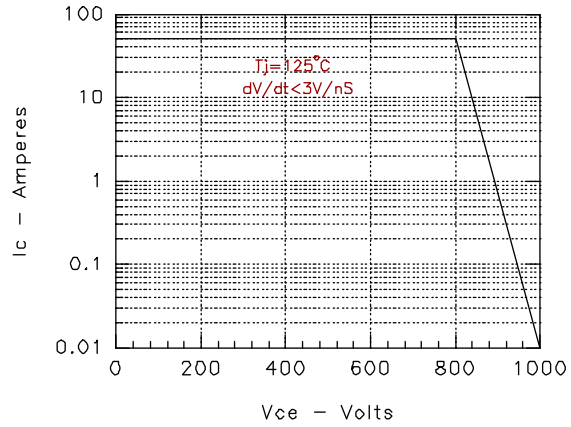


Fig. 9. Capacitance Curves

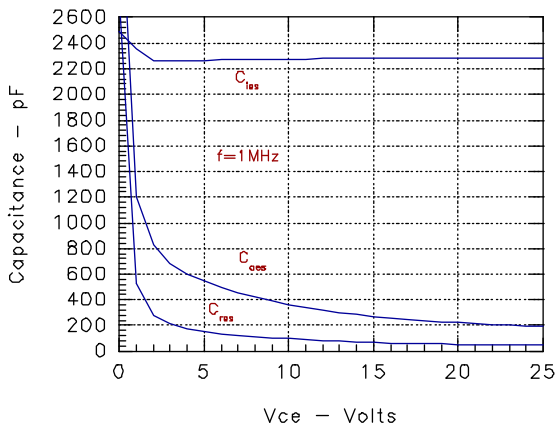
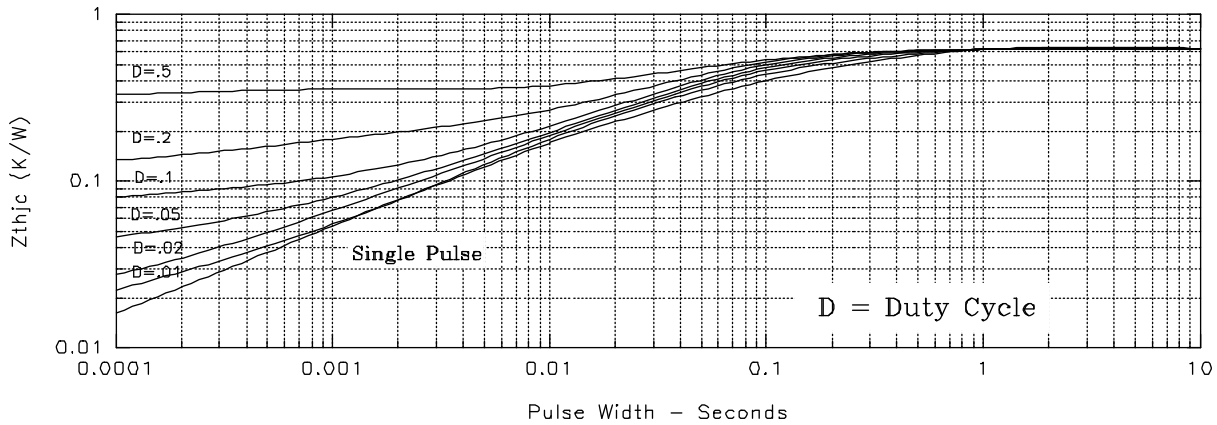


Fig. 10. Transient Thermal Impedance



IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,881,106	5,017,508	5,049,961	5,187,117	5,486,715
4,850,072	4,931,844	5,034,796	5,063,307	5,237,481	5,381,025

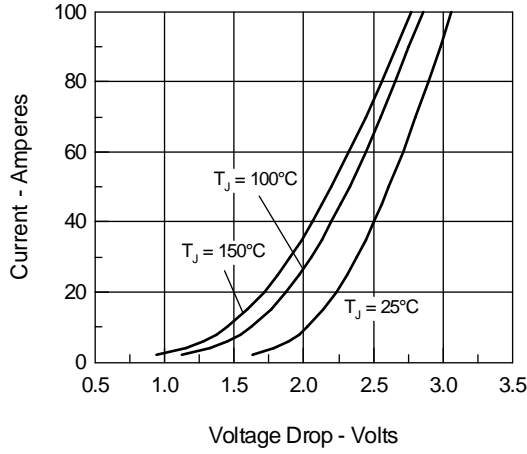
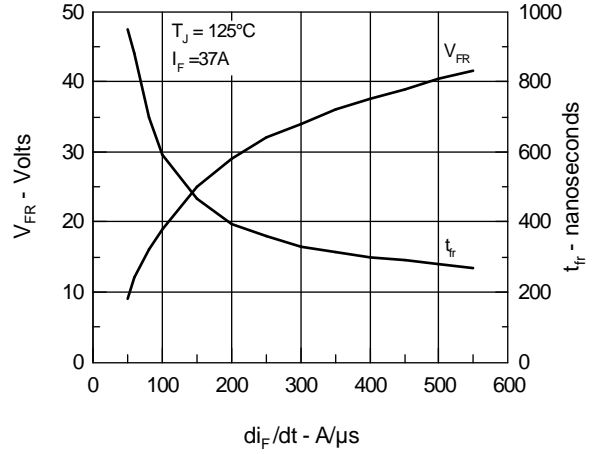
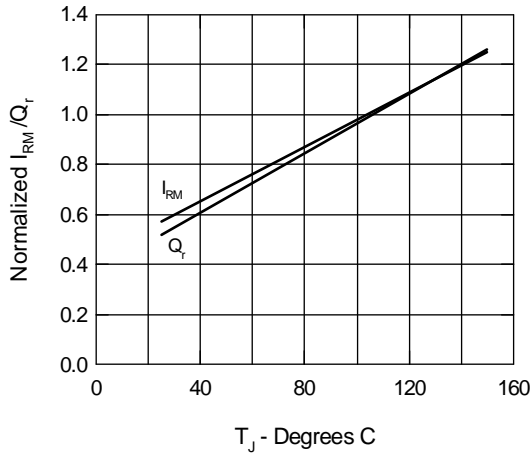
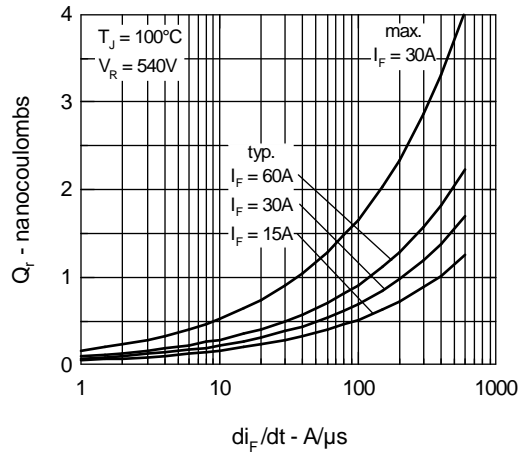
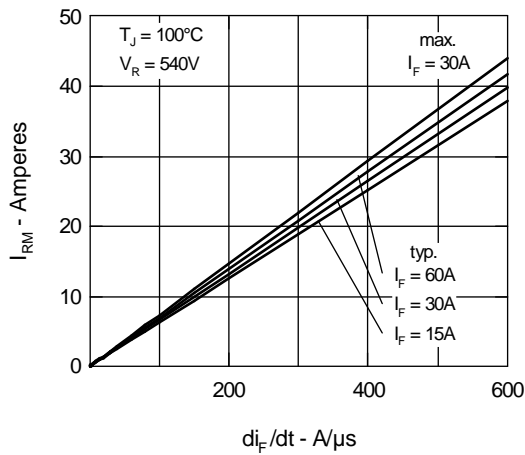
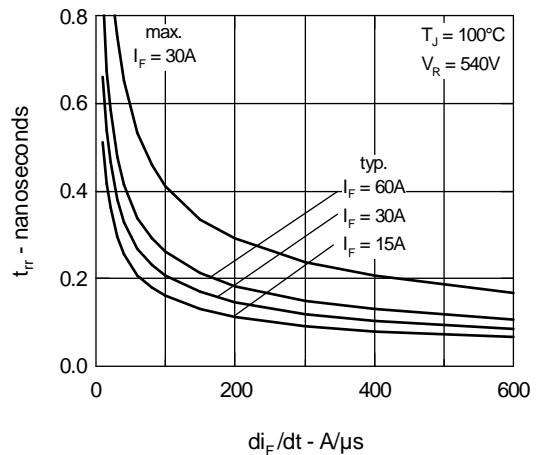
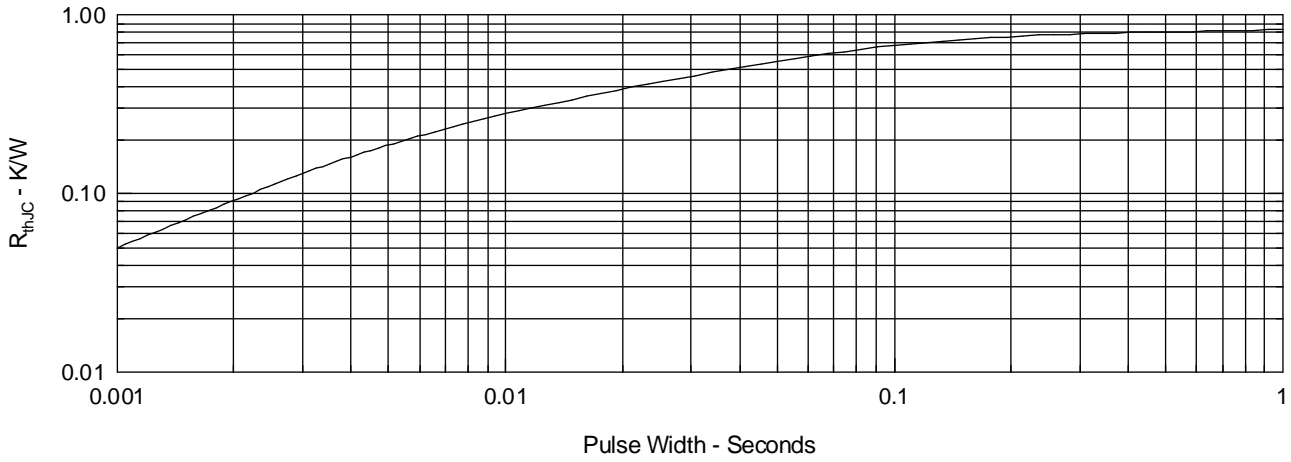
Fig.11 Maximum Forward Voltage Drop

Fig.12 Peak Forward Voltage V_{FR} and Forward Recovery Time t_{FR}

Fig.13 Junction Temperature Dependence of I_{RM} and Q_r

Fig.14 Reverse Recovery Charge Q_r

Fig.15 Peak Reverse Recovery Current

Fig.16 Reverse Recovery Time


Fig.17 Diode Transient Thermal resistance junction to case



IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,881,106	5,017,508	5,049,961	5,187,117	5,486,715
4,850,072	4,931,844	5,034,796	5,063,307	5,237,481	5,381,025