

Power-Charge-Pump and Low-Drop Voltage Regulator

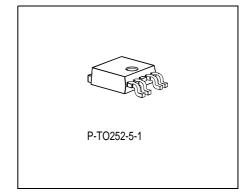
TLE 4307

Power Charge Pump Circuit Features

- High Current Capability
- Short Circuit Protection
- Overtemperature Protection
- Active Zener Circuit

Very Low Drop Voltage Regulator Features

- 3.3 V or 3.8 V output voltage
- Low Output Voltage Tolerance
- High Current Capability 800 mA
- Short Circuit Protection
- Overtemperature Protection



General Features

Optimized SMD Package

	Туре	Ordering Code	Package			
•	TLE 4307 DV33	Q67006-A9444	P-TO252-5-1 (D-PAK)			
•	TLE 4307 DV38	Q67006-A9415	P-TO252-5-1 (D-PAK)			

• New Type

Functional Description

The TLE 4307 is a monolithic integrated power charge pump with a Low Drop Voltage Regulator. The power charge pump loads an energy storage capacitor at pin C. The voltage regulator supplies 3.3 V or 3.8 V out of this storage capacitor with up to 800 mA output current. The TLE 4307 is intended for use with DC supplies for consumer or industrial applications.



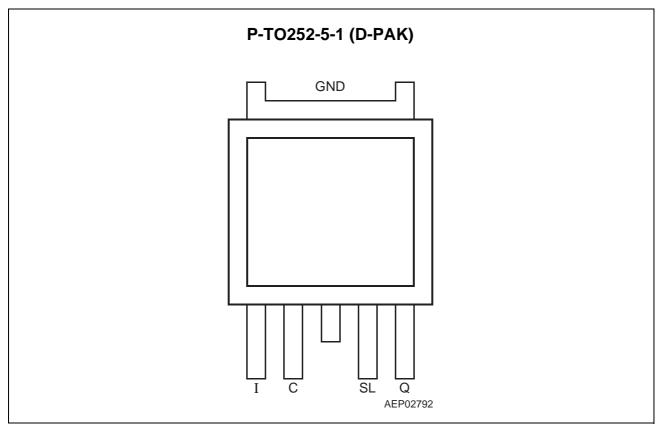


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	Input; Connect to the input voltage source
2	С	Charge-Pump Output; Connect to the energy reservoir capacitor to GND
3	GND	Ground
4	SL	Slewrate Control Input; a capacitor from this pin to the Input pin I controls the slewrate during recirculation
5	Q	Regulator Output; connect to GND with a capacitor as specified for $C_{\rm Q}$



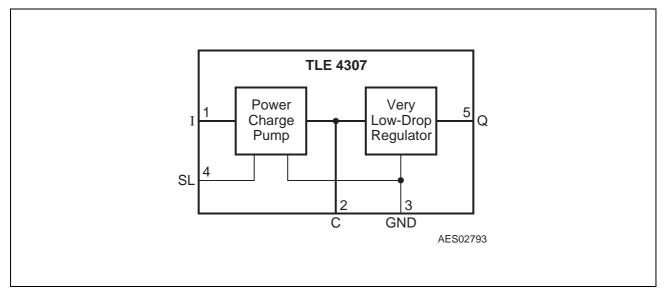


Figure 2 Block Diagram

Circuit Description

The TLE 4307 consists of 2 stages, the charge pump and the very low drop voltage regulator.

Charge Pump

The power stage is used as a switching element, that is driven by a buffer. A current source keeps the power stage on. When the output C of the charge pump reaches $V_{\rm C,off}$, the power stage is switched off. It is active clamped, when the input I reaches $V_{\rm I,cl}$. Optional, an external capacity can be connected between pin SL and I to limit the slew rate at the input, when an inductive load drives the IC. Saturation control as a function of the load current prevents any over-saturation of the power element. The regulator is additionally protected against overload and overtemperature.

Very Low Drop Regulator

The control amplifier compares a reference voltage, made highly accurate by resistance balancing, with a voltage proportional to the output voltage and drives the base of the series PNP transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. The regulator is additionally protected against overload and overtemperature.

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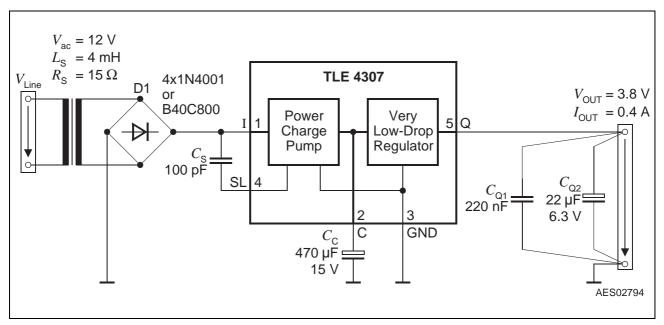


Figure 3 Application Example

Application Description

The IC is meant to be used with a DC power supply. The power charge pump limits the energy that is needed to drive the load at the output Q of the IC. The energy is stored to a capacity $C_{\rm C}$, connected to pin C. When pin C reaches $V_{\rm C,off}$, the power charge pump is switched off. Since the power supply consists of the inductance and a parasitic series resistance, the remaining available energy is dissipated in the external power supply and therefore does not stress the IC with this dispensable energy. The very low drop regulator is provided with the energy, stored in $C_{\rm C}$. The regulator requires an output capacitor $C_{\rm Q}$ for the stability of the regulating circuit. Stability is guaranteed at values above 22 μ F and an ESR \leq 1 Ω within the operating temperature range.



Parameter	Symbol	Limi	t Values	Unit	Notes
		min.	max.		
Input					
Input voltage	V_{l}	- 0.3	V_{ICL}	V	$V_{\rm ICL}$ = zener clamp voltage
Input current (during pump cycle)	I_{I}	- 5	_	mA	internally limited
Input current (during active zener operation)	I	- 5	1000	mA	$t_{\rm p}$ < 1 ms; duty cycle 10%
Charge-Pump Output					
Voltage	V_{C}	- 0.3	20	V	_
Current	I_{C}	_	_	mA	internally limited
Slewrate Input					
Voltage	V_{SL}	- 0.3	4.0	V	_
Current	I_{SL}	- 0.5	0.5	mA	_
Regulator Output					
Voltage	V_{Q}	- 0.3	25	V	_
Current	I_{Q}	_	_	mA	internally limited
Temperature					
Junction temperature	T_{j}	- 40	150	°C	_
Storage temperature	T_{Stg}	- 50	150	°C	_
Thermal Data					
Junction-ambient	R_{thj-a}	_	70	K/W	_
	R_{thj-c}	_	4	K/W	_



Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Symbol Limit Value		Unit	Notes	
			max.			
ESD						
All pins to GND	V_{ESD}	-2	2	kV	HBM Model	
Operating Bongs						
Operating Range						
Input voltage	V_{l}	0	V_{ICL}	V	-	
Output current	I_{I}	0	600	mA	_	
Junction temperature	T_{i}	- 40	150	°C		



Electrical Characteristics

 $V_{
m I}$ = 12 V; 40 °C < $T_{
m j}$ < 150 °C

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Measuring
		min.	typ.	max.		Condition
Current consumption; $I_{q} = I_{l} - I_{Q}$	I_{q}	_	1.2	2.5	mA	$I_{\rm Q}$ = 0 mA $V_{\rm I}$ = 6 V
Current consumption; $I_{q} = I_{l} - I_{Q}$	$I_{q,10}$	_	1.4	3.0	mA	$I_{\rm Q}$ = 10 mA $V_{\rm I}$ = 6 V
Current consumption; $I_{q} = I_{l} - I_{Q}$	$I_{q,250}$	_	4	10	mA	$I_{\rm Q}$ = 250 mA $V_{\rm I}$ = 6 V

Charge Pump

Switch off threshold	$V_{C,off}$	7.7	8.2	8.7	V	_
Input Clamp Voltage	$V_{I,cl}$	21	23	25	V	I _I = 250 mA
Current limit	$I_{C,max}$	0.7	1.2	1.6	Α	$V_{\rm C}$ = 5 V
Drop voltage; $V_{\rm I} - V_{\rm C}$	V_{DR025}	_	0.8	1.1	V	$I_{\rm C}$ = 0.25 A
Drop voltage; $V_{\rm I} - V_{\rm C}$	V_{DR06}	_	1.2	1.5	V	$I_{\rm C} = 0.6 \; {\rm A}$
Drop voltage; $V_{\rm I} - V_{\rm C}$	V_{DR07}	_	1.4	2.0	V	$I_{\rm C} = 0.7 \; {\rm A}$

Main-Regulator

Output voltage	V_{Q}	3.7	3.8	3.9	V	$0 < I_{\rm Q} < 250$ mA, TLE 4307 DV38
Output voltage	V_{Q}	3.2	3.3	3.4	V	$0 < I_{\rm Q} < 250$ mA, TLE 4307 DV33
Current limit	$I_{Q,max}$	0.8	1.2	1.6	Α	_
Drop voltage; $V_{\rm C} - V_{\rm Q}$	V_{DR025}		0.2	0.4	V	$I_{\rm Q} = 0.25 \; {\rm A}^{1)}$
Drop voltage; $V_{\rm C} - V_{\rm Q}$	V_{DR06}	1	0.4	0.7	V	$I_{\rm Q} = 0.6 {\rm A}^{\rm 1)}$
Drop voltage; $V_{\rm C} - V_{\rm Q}$	V_{DR08}	_	1.0	2.0	V	$I_{\rm Q} = 0.8 {\rm A}^{\rm 1)}$
Over all Drop voltage; $V_{\text{I}} - V_{\text{Q}}$	V_{DR}	_	1.1	1.3	V	$I_{\rm Q} = 0.25 {\rm A}^{1)}$
Load regulation	$\Delta V_{ m QLO}$	_	20	40	mV	$200~\mathrm{mA} < I_\mathrm{Q} < \\ 600~\mathrm{mA}$



Electrical Characteristics (cont'd)

 $V_{\rm I}$ = 12 V; 40 °C < $T_{\rm j}$ < 150 °C

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified.

Parameter	Symbol	Li	mit Val	ues	Unit	Measuring
		min.	typ.	max.		Condition
Line regulation	ΔV_{QLI}	_	_	20	mV	$5 \text{ V} < V_{\text{C}} < 8.7 \text{ V}$ $I_{\text{Q}} = 10 \text{ mA}$
Power Supply Ripple rejection	PSRR	- 40	_	_	dB	$f_{\rm r}$ = 100 Hz; $V_{\rm r}$ = 0.5 $V_{\rm SS}$
Output Capacitor	C_{Q}	22	_	_	μF	ESR < 1 Ω

Slewrate Input

Input Resistance	R_{SL}	60	120	200	kΩ	$V_{\rm SL}$ = 0.2 V

¹⁾ Drop Voltage measured when the output voltage has dropped 100 mV from the nominal value.

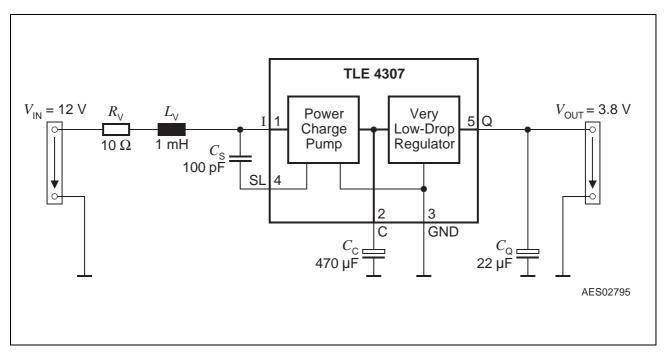


Figure 4 Measurement Circuit

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Package Outlines

P-TO252-5-1 (D-PAK) (Plastic Transistor Single Outline Package) 2.3 +0.05 6.5 +0.15 $0.9^{+0.08}_{-0.04}$ 5.4 ± 0.1 1±0.1 0...0.15 0.51 min 0.15 max per side 0.5 +0.08 5x0.6±0.1 1.14 - □ 0.1 4.56 ⊕ 0.25 M A B GPT09161 All metal surfaces tin plated, except area of cut.

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm



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