



GENERAL DESCRIPTION



The ICS8421002I is a 2 output HSTL Synthesizer optimized to generate Fibre Channel reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 26.5625MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 212.5MHz, 187.5MHz, 159.375MHz, 106.25MHz and 53.125MHz. The ICS8421002I uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Fibre Channel jitter requirements. The ICS8421002I is packaged in a small 20-pin TSSOP package.

FEATURES

- Two HSTL outputs (VOHmax = 1.5V)
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 212.5MHz, 187.5MHz, 159.375MHz, 106.25MHz, 53.125MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 212.5MHz, using a 26.5625MHz crystal (637kHz - 10MHz): 0.59ps (typical)
- Power supply modes:
Core/Output
3.3V/1.8V
2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

FREQUENCY SELECT FUNCTION TABLE

| Input Frequency (MHz) | Inputs | | | | | Output Frequency (MHz) |
|-----------------------|--------|--------|-----------------|-----------------|-------------------|------------------------|
| | F_SEL1 | F_SEL0 | M Divider Value | N Divider Value | M/N Divider Value | |
| 26.5625 | 0 | 0 | 24 | 3 | 8 | 212.5 |
| 26.5625 | 0 | 1 | 24 | 4 | 6 | 159.375 |
| 26.5625 | 1 | 0 | 24 | 6 | 4 | 106.25 |
| 26.5625 | 1 | 1 | 24 | 12 | 2 | 53.125 |
| 23.4375 | 0 | 0 | 24 | 3 | 8 | 187.5 |

PIN ASSIGNMENT

| | | | |
|----------|----|----|-----------|
| nc | 1 | 20 | VDD0 |
| VDD0 | 2 | 19 | Q1 |
| Q0 | 3 | 18 | nQ1 |
| nQ0 | 4 | 17 | GND |
| MR | 5 | 16 | VDD |
| nPLL_SEL | 6 | 15 | nXTAL_SEL |
| nc | 7 | 14 | REF_CLK |
| VDDA | 8 | 13 | XTAL_IN |
| F_SEL0 | 9 | 12 | XTAL_OUT |
| VDD | 10 | 11 | F_SEL1 |

ICS8421002I

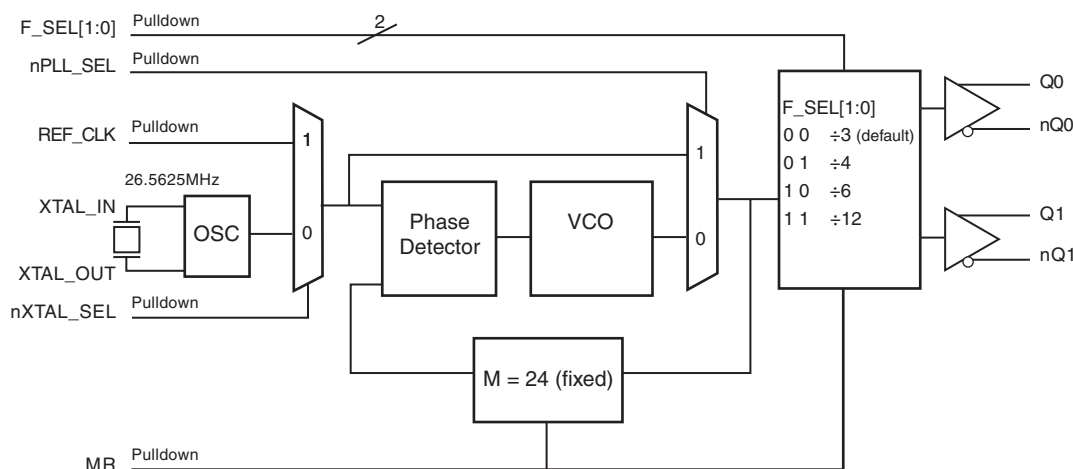
20-Lead TSSOP

6.5mm x 4.4mm x 0.92mm
package body

G Package

Top View

BLOCK DIAGRAM



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------|----------------------|--------|----------|---|
| 1, 7 | nc | Unused | | No connect. |
| 2, 20 | V _{DDO} | Power | | Output supply pins. |
| 3, 4 | Q0, nQ0 | Output | | Differential output pair. HSTL interface levels. |
| 5 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 6 | nPLL_SEL | Input | Pulldown | Selects between the PLL and REF_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels. |
| 8 | V _{DDA} | Power | | Analog supply pin. |
| 9, 11 | F_SEL0, F_SEL1 | Input | Pulldown | Frequency select pins. LVCMOS/LVTTL interface levels. |
| 10, 16 | V _{DD} | Power | | Core supply pin. |
| 12, 13 | XTAL_OUT, XTAL_IN | Input | | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. |
| 14 | REF_CLK | Input | Pulldown | LVCMOS/LVTTL reference clock input. |
| 15 | nXTAL_SEL | Input | Pulldown | Selects between crystal or REF_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels. |
| 17 | GND | Power | | Power supply ground. |
| 18, 19 | nQ1, Q1 | Output | | Differential output pair. HSTL interface levels. |

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |



ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, I_O | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, θ_{JA} | 73.2°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | | | | 110 | mA |
| I_{DDA} | Analog Supply Current | | | | 12 | mA |
| I_{DDO} | Output Supply Current | No Load | | 0 | | mA |

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DDA} | Analog Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DDO} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | | | | 96 | mA |
| I_{DDA} | Analog Supply Current | | | | 12 | mA |
| I_{DDO} | Output Supply Current | No Load | | 0 | | mA |

TABLE 3C. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|--|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | $V_{DD} = 3.3V$ | 2 | | $V_{DD} + 0.3$ | V |
| | | $V_{DD} = 2.5V$ | 1.7 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | $V_{DD} = 3.3V$ | -0.3 | | 0.8 | V |
| | | $V_{DD} = 2.5V$ | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | REF_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL $V_{DD} = V_{IN} = 3.465V$ or 2.5V | | | 150 | μA |
| I_{IL} | Input Low Current | REF_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL $V_{DD} = 3.465V$ or 2.5V, $V_{IN} = 0V$ | -150 | | | μA |



TABLE 3D. HSTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|---------|---------|---------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | 1.0 | | 1.5 | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | 0 | | 0.5 | V |
| V_{OX} | Output Crossover Voltage; NOTE 2 | | 40 | | 60 | % |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.3 | V |

NOTE 1: Outputs terminated with 50Ω to ground.

NOTE 2: Defined with respect to output voltage swing at a given condition.

TABLE 3E. HSTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|---------|---------|---------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | 0.8 | | 1.5 | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | 0 | | 0.6 | V |
| V_{OX} | Output Crossover Voltage; NOTE 2 | | 40 | | 60 | % |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.5 | | 1.5 | V |

NOTE 1: Outputs terminated with 50Ω to ground.

NOTE 2: Defined with respect to output voltage swing at a given condition.

TABLE 4. CRYSTAL CHARACTERISTICS

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 23.33 | 26.5625 | 28.33 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 1 | mW |

NOTE: Characterized using an 18pF parallel resonant crystal.



TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|--------------------------------------|------------------------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | F_SEL[1:0] = 00 | 186.67 | | 226.66 | MHz |
| | | F_SEL[1:0] = 01 | 140 | | 170 | MHz |
| | | F_SEL[1:0] = 10 | 93.33 | | 113.33 | MHz |
| | | F_SEL[1:0] = 11 | 46.67 | | 56.66 | MHz |
| tsk(o) | Output Skew; NOTE 1, 3 | | | 20 | ps | |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 2 | 212.5MHz, (637kHz - 10MHz) | | 0.59 | | ps |
| | | 187.5MHz, (1.875MHz - 20MHz) | | 0.51 | | ps |
| | | 159.375MHz, (637kHz - 10MHz) | | 0.56 | | ps |
| | | 106.25MHz, (637kHz - 10MHz) | | 0.69 | | ps |
| | | 53.125MHz, (637kHz - 10MHz) | | 0.66 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 175 | | 875 | ps |
| odc | Output Duty Cycle | N Divider = 4, 6, 12 | 48 | | 52 | % |
| | | N Divider = 3 | 44 | | 56 | % |

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at $V_{DDO}/2$.

NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|--------------------------------------|------------------------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | F_SEL[1:0] = 00 | 186.67 | | 226.66 | MHz |
| | | F_SEL[1:0] = 01 | 140 | | 170 | MHz |
| | | F_SEL[1:0] = 10 | 93.33 | | 113.33 | MHz |
| | | F_SEL[1:0] = 11 | 46.67 | | 56.66 | MHz |
| tsk(o) | Output Skew; NOTE 1, 3 | | | 20 | ps | |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 2 | 212.5MHz, (637kHz - 10MHz) | | 0.60 | | ps |
| | | 187.5MHz, (1.875MHz - 20MHz) | | 0.70 | | ps |
| | | 159.375MHz, (637kHz - 10MHz) | | 0.64 | | ps |
| | | 106.25MHz, (637kHz - 10MHz) | | 0.70 | | ps |
| | | 53.125MHz, (637kHz - 10MHz) | | 0.68 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle | N Divider = 4, 6, 12 | 48 | | 52 | % |
| | | N Divider = 3 | 44 | | 56 | % |

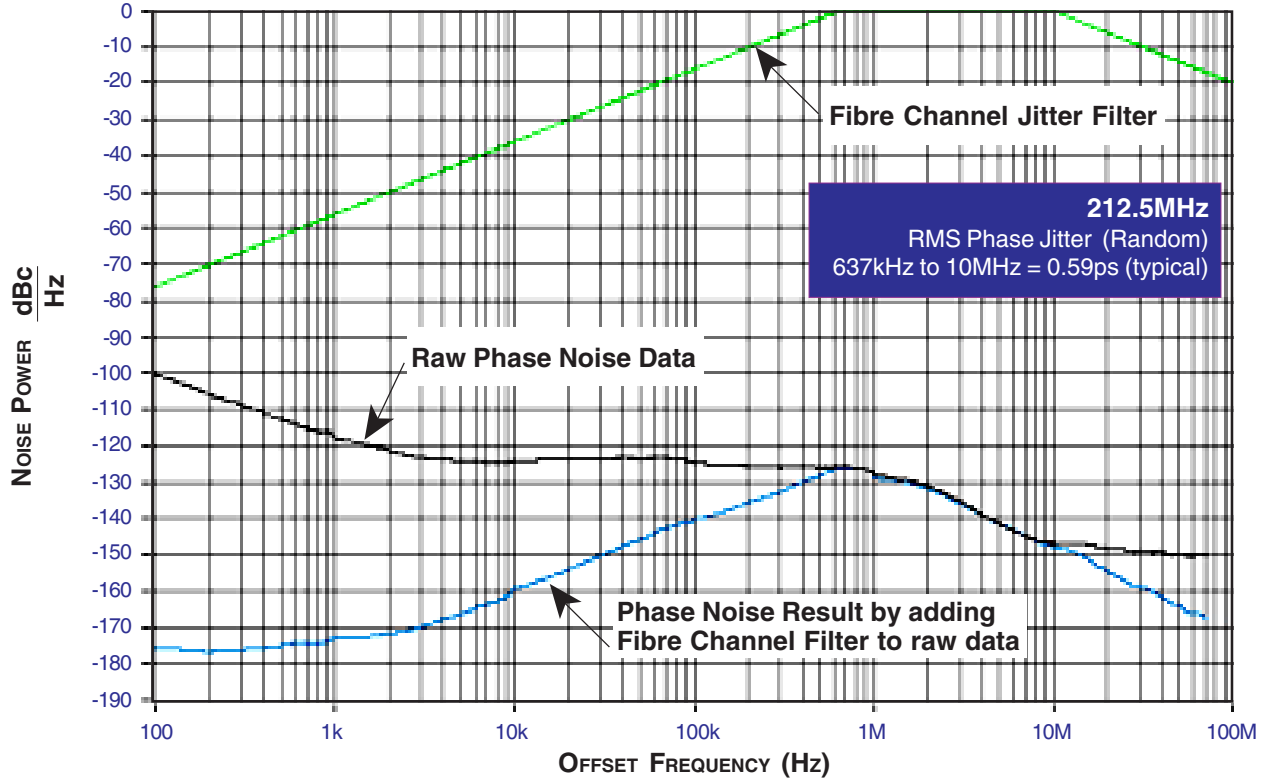
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at $V_{DDO}/2$.

NOTE 2: Please refer to the Phase Noise Plot.

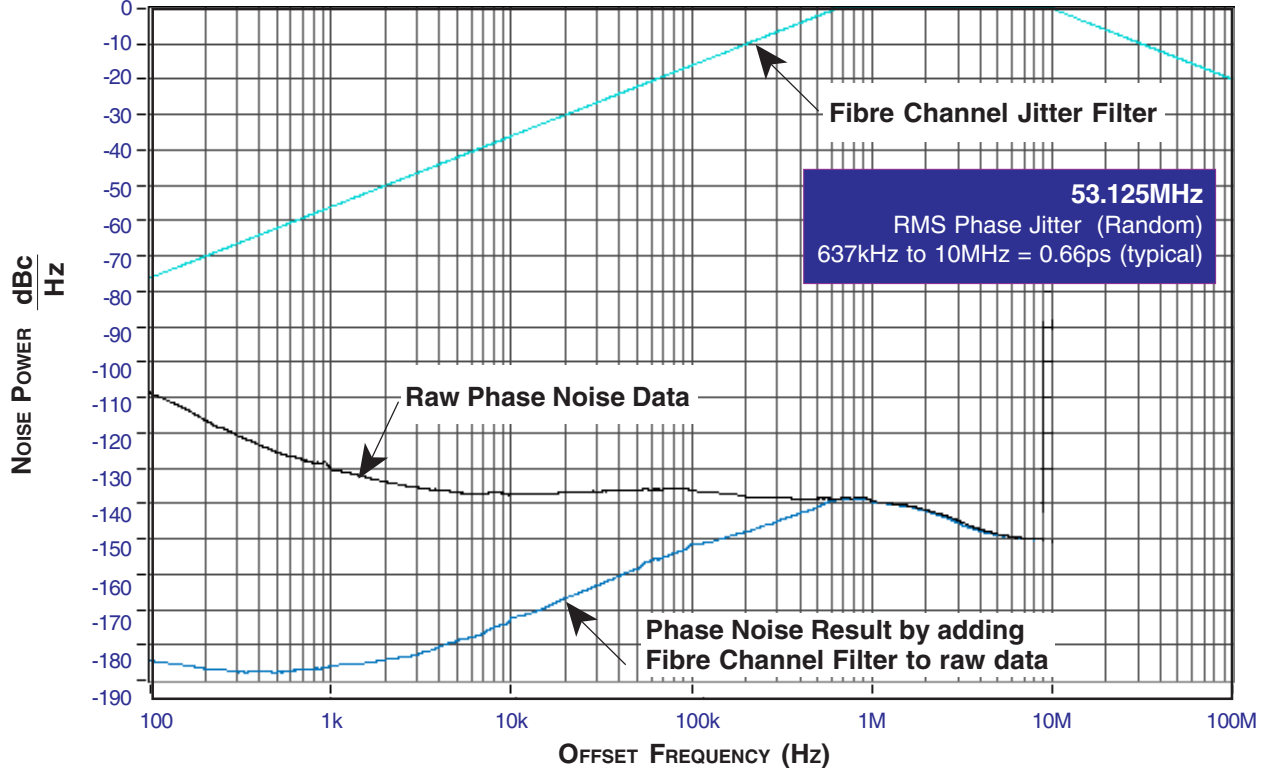
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.



TYPICAL PHASE NOISE AT 212.5MHz @ 3.3V

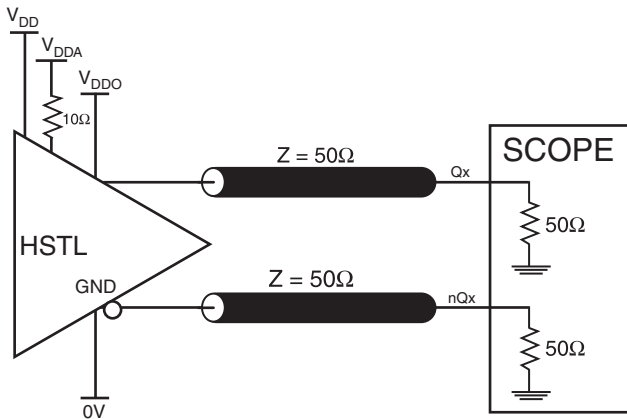


TYPICAL PHASE NOISE AT 53.125MHz @ 3.3V

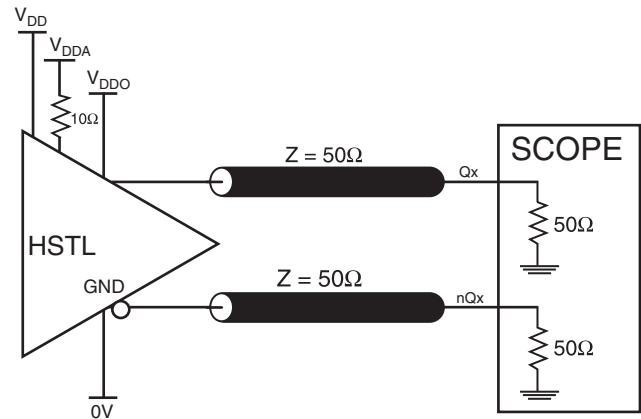




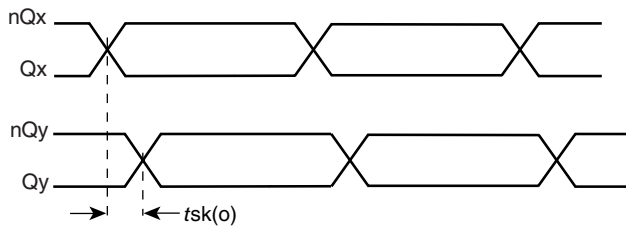
PARAMETER MEASUREMENT INFORMATION



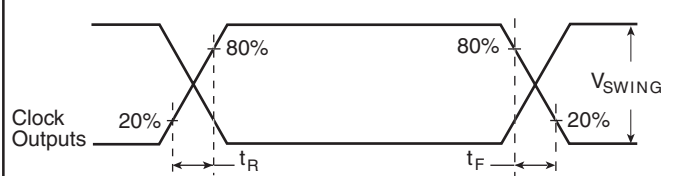
HSTL 3.3V/1.8V OUTPUT LOAD AC TEST CIRCUIT



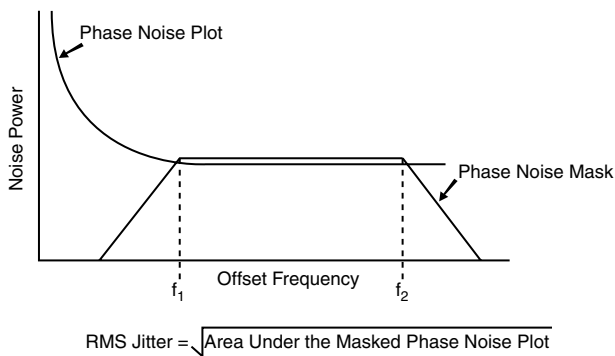
HSTL 2.5V/1.8V OUTPUT LOAD AC TEST CIRCUIT



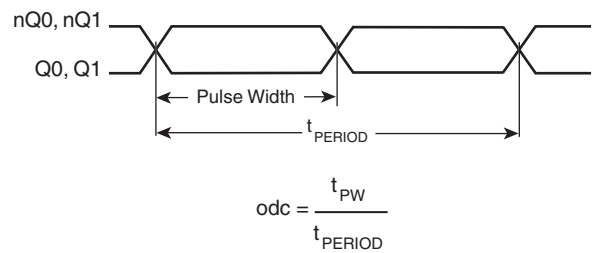
OUTPUT SKEW



OUTPUT RISE/FALL TIME



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8421002I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{DDA} .

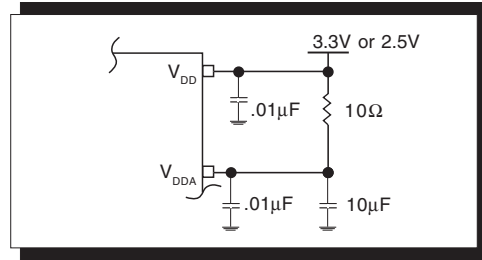


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS8421002I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2*

below were determined using a 26.5625MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

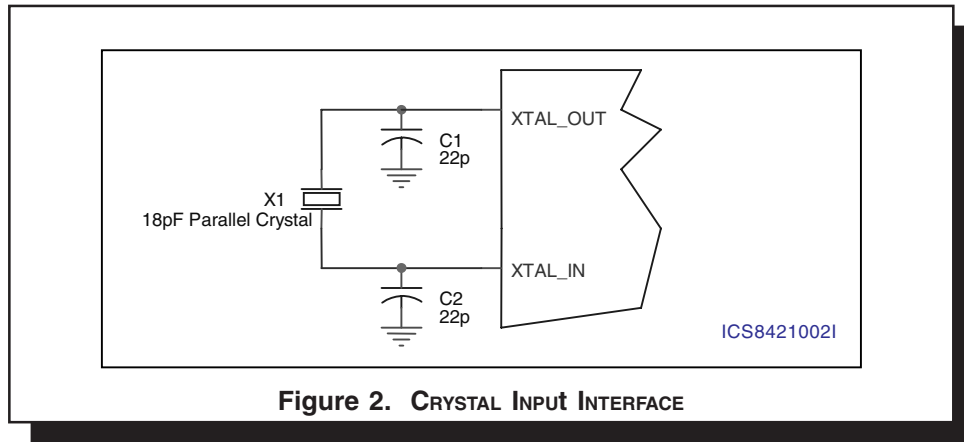


Figure 2. CRYSTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT:

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from the REF_CLK to ground.

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

OUTPUTS:

HSTL OUTPUT

All unused HSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8421002I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8421002I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{DD_MAX} * I_{DD_MAX} = 3.465V * 122mA = 422.7mW$
- Power (outputs)_{MAX} = **32.8mW/Loaded Output pair**
If all outputs are loaded, the total power is $2 * 32.8mW = 65.6mW$

Total Power_{MAX} (3.465V, with all outputs switching) = $422.7mW + 65.6mW = 488.3mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.488W * 66.6^\circ C/W = 117.5^\circ C$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|-----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

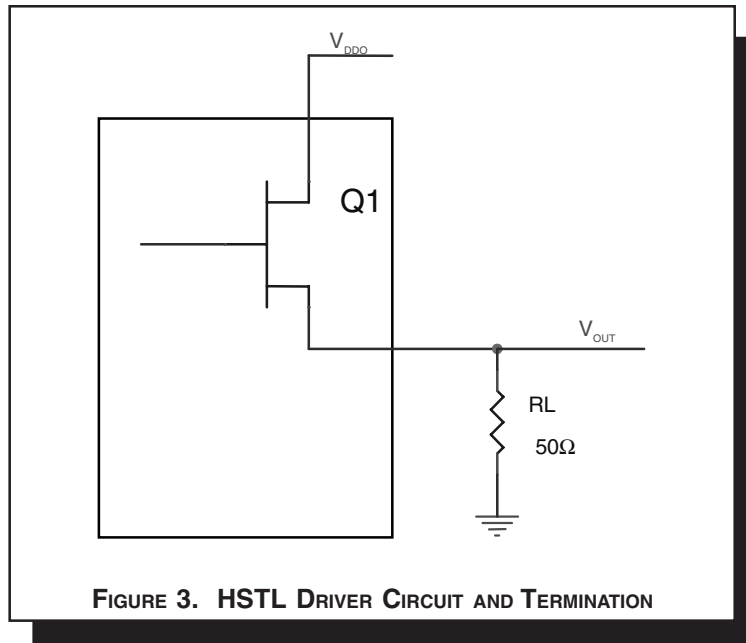
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 3*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = (V_{OH_MAX} / R_L) * (V_{DD_MAX} - V_{OH_MAX})$$

$$Pd_L = (V_{OL_MAX} / R_L) * (V_{DD_MAX} - V_{OL_MAX})$$

$$Pd_H = (1V/50\Omega) * (2V - 1V) = \mathbf{20mW}$$

$$Pd_L = (0.4V/50\Omega) * (2V - 0.4V) = \mathbf{12.8mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{32.8mW}$$



RELIABILITY INFORMATION

TABLE 7. θ_{JA} vs. AIR FLOW TABLE FOR 20 LEAD TSSOP

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|-----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8421002I is: 2951



PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

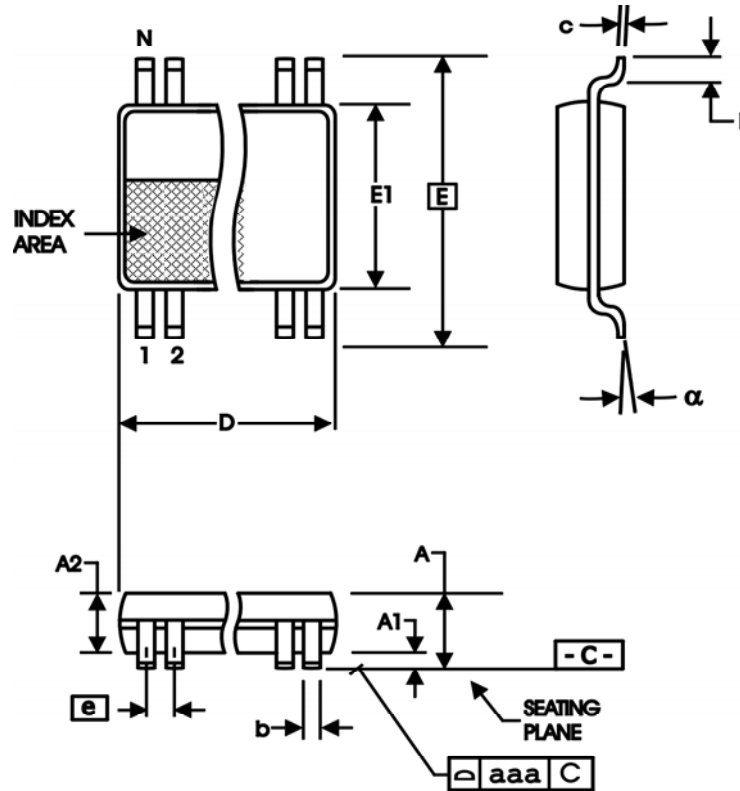


TABLE 8. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|------|
| | MIN | MAX |
| N | 20 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 6.40 | 6.60 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153



Integrated
Circuit
Systems, Inc.

ICS8421002I

FEMTOCLOCKS™ CRYSTAL-TO- HSTL FREQUENCY SYNTHESIZER

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|---------------------------|--------------------|---------------|
| ICS8421002AGI | ICS8421002AI | 20 Lead TSSOP | tube | -40°C to 85°C |
| ICS8421002AGIT | ICS8421002AI | 20 Lead TSSOP | 2500 tape & reel | -40°C to 85°C |
| ICS8421002AGILF | ICS421002AIL | 20 Lead "Lead-Free" TSSOP | tube | -40°C to 85°C |
| ICS8421002AGILFT | ICS421002AIL | 20 Lead "Lead-Free" TSSOP | 2500 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free Configuration and are RoHS compliant.

The aforementioned trademarks, HiPerClockS and FemtoClocks are trademarks of Integrated Circuit Systems, Inc. or its subsidiaries in the United States and/or other countries. While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.