

KM416S1021C

Preliminary CMOS SDRAM

512K x 16Bit x 2 Banks Synchronous DRAM with SSTL interface

FEATURES

- JEDEC standard 3.3V power supply
- SSTL_3 (Class II) compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

GENERAL DESCRIPTION

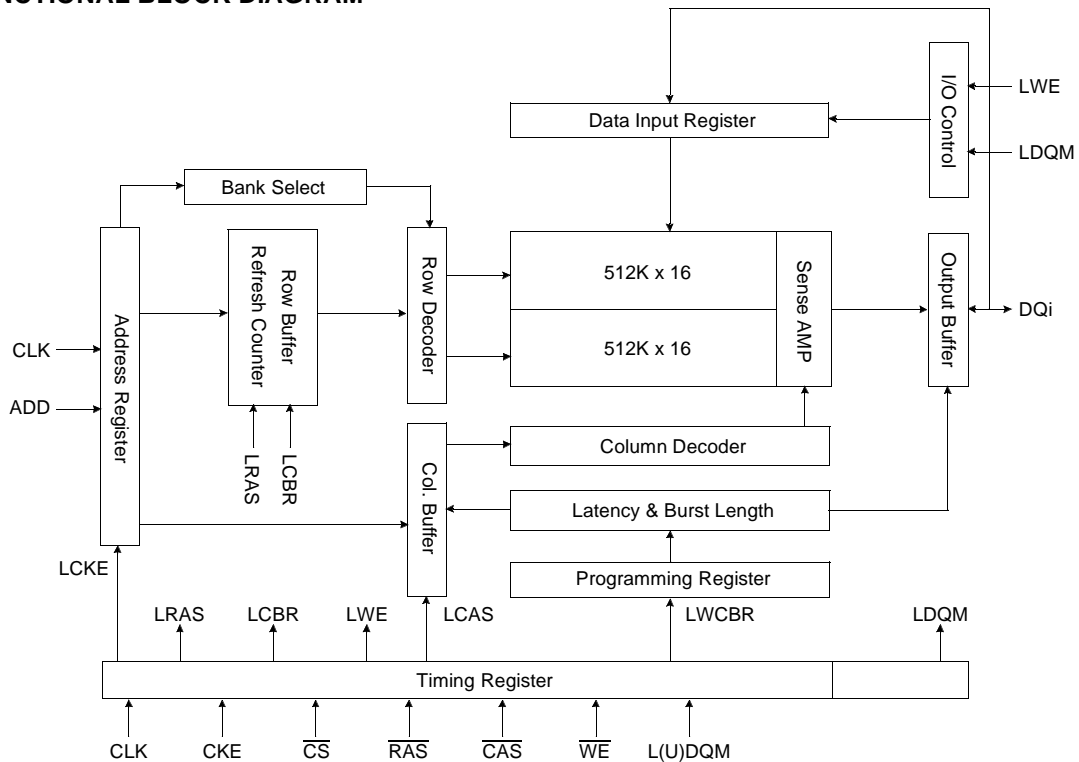
The KM416S1021C is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 524,288 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
KM416S1021CT-G7	143MHz	SSTL_3 (Class II)	54 TSOP(II)
KM416S1021CT-GS	100MHz(CL=2)		
KM416S1021CT-G8	125MHz		

* KM416S1021CT-GS : CL=2 only

FUNCTIONAL BLOCK DIAGRAM

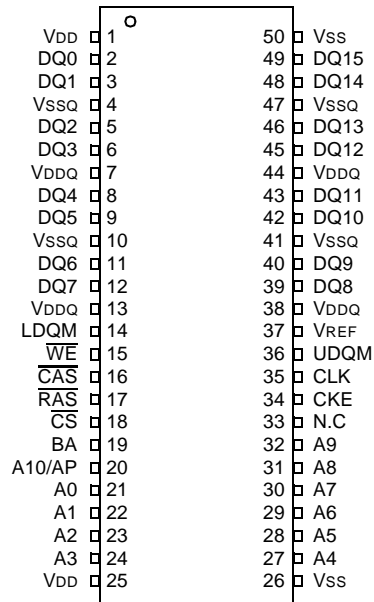


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PIN CONFIGURATION (Top view)



50Pin TSOP (II)
(400mil x 825mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
\overline{CS}	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A10/AP	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, Column address : CA0 ~ CA7
BA	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
\overline{RAS}	Row address strobe	Latches row addresses on the positive going edge of the CLK with \overline{RAS} low. Enables row access & precharge.
\overline{CAS}	Column address strobe	Latches column addresses on the positive going edge of the CLK with \overline{CAS} low. Enables column access.
\overline{WE}	Write enable	Enables write operation and row precharge. Latches data in starting from \overline{CAS} , \overline{WE} active.
L(U)DQM	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ 15	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
VREF	Reference voltage	Reference voltage for inputs.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device supply voltage	V _{DD}	V _{DDQ}	-	3.6	V	1
Output supply voltage	V _{DDQ}	3.0	3.3	3.6	V	1
		3.26	3.43	3.6	V	8
Input reference voltage	V _{REF}	1.3	1.5	1.7	V	2, 3
Termination voltage	V _{tt}	V _{REF} -0.05	V _{REF}	V _{REF} +0.05	V	
Input logic high voltage	V _{IH}	V _{REF} +0.2	-	V _{DD} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	V _{REF} -0.2	V	2
Output logic high voltage	V _{OH}	V _{tt} +0.8	-	-	V	5
Output logic low voltage	V _{OL}	-	-	V _{tt} -0.8	V	5
Input leakage current	I _{IL}	-5	-	5	uA	6
Output leakage current	I _{OL}	-5	-	5	uA	7

- Notes :**
- Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
 - Typically, the value of V_{REF} is expected to be about 0.45 * V_{DDQ} of the transmitting device.
V_{REF} is expected to track variations in V_{DDQ}.
 - Peak to peak AC noise on V_{REF} may not exceed 2% V_{REF} (DC)
 - V_{tt} of transmitting device must track V_{REF} of receiving device.
 - Voltage level measured at device pin with I_{OH}/I_{OL} = -16mA/16mA.
 - Any input 0V ≤ V_{IN} ≤ V_{DD}+0.3V, all other pins are not under test = 0V.
 - Dout buffer is disabled, 0V ≤ V_{OUT} ≤ V_{DD}.
 - Apply to only the KM416S1021CT-GS.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
CLK, CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ & L(U)DQM	C _{IN}	2	4	pF
Address	C _{ADD}	2	4	pF
DQ ₀ ~ DQ ₁₅	C _{OUT}	2	5	pF

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DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-7	-S	-8		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IOL = 0 mA		95	90	95	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 15ns		2			mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞		2				
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), \overline{CS} ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		20			mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		6				
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 15ns		3			mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞		2				
Active Standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), \overline{CS} ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		30			mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		20				
Operating current (Burst mode)	ICC4	IOL = 0 mA Page burst tccd = 2CLKs	3	150	140	130	mA	1
			2	105	100	100		
Refresh current	ICC5	trc ≥ trc(min)		90	85	80	mA	2
Self refresh current	ICC6	CKE ≤ VIL(max)		2			mA	3

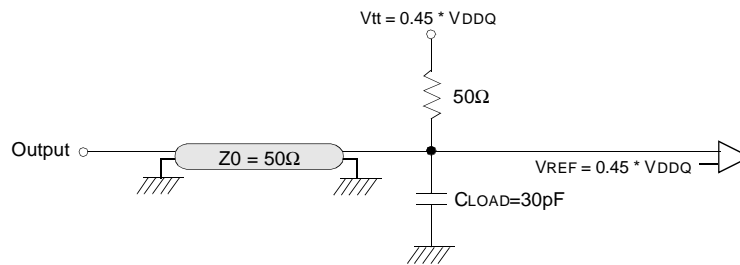
- Notes** :1. Measured with outputs open.
2. Refresh period is 64ms.

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AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V, 3.43V \pm 0.5\%$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
Input reference voltage	$0.45 * V_{DDQ}$	V
Input signal maximum peak swing	2.0	V
Input signal minimum slew rate	1.0	V/ns
AC input levels (V_{ih}/V_{il})	$V_{REF} + 0.4/V_{REF} - 0.4$	V
Input timing measurement reference level	V_{REF}	V
Output timing measurement reference level	V_{tt}	V
Output load condition	See Fig. 1	



(Fig. 1) Output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version			Unit	Note
		-7	-S	-8		
Row active to row active delay	$t_{RRD}(\min)$	14	20	16	ns	1
\overline{RAS} to \overline{CAS} delay	$t_{RCD}(\min)$	21	20	24	ns	1
Row precharge time	$t_{RP}(\min)$	21	20	24	ns	1
Row active time	$t_{RAS}(\min)$	49	50	56	ns	1
	$t_{RAS}(\max)$	100			us	
Row cycle time	$t_{RC}(\min)$	70	70	80	ns	1
Last data in to new col. address delay	$t_{CDL}(\min)$	1			CLK	2
Last data in to row precharge	$t_{RDL}(\min)$	1			CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1			CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1			CLK	3
Number of valid output data	CAS latency=3	2	-	2	ea	4
	CAS latency=2	1	1	1		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

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AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-7		-S		-8		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7	1000	-	1000	8	1000	ns	1
	CAS latency=2		12		10		13			
CLK to Valid Output Delay	CAS latency=3	tSAC		5.5	-		6	ns	1,2	
	CAS latency=2			7		6	8			
Output data hold time		tOH	2.5		2		2.5	ns	2	
CLK high pulse width		tCH	3		3.5		3	ns	3	
CLK low pulse width		tCL	3		3.5		3	ns	3	
Input setup time		tSS	2		2		2.5	ns	3	
Input hold time		tSH	1		1		1	ns	3	
CLK to output in Low-Z		tSLZ	1		1		1	ns	2	
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.5	-		6	ns		
	CAS latency=2			7		8	8			

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

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FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM416S1021BT-G7

(Unit : Number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	49ns	21ns	14ns	21ns	7ns	7ns	7ns
143MHz (7.0ns)	3	10	7	3	2	3	1	1	1
125MHz (8.0ns)	3	9	7	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	3	2	3	1	1	1
83MHz (12.0ns)	2	6	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	1	2	1	1	1

KM416S1021BT-GS

(Unit : Number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	50ns	20ns	20ns	20ns	10ns	10ns	10ns
100MHz (10.0ns)	2	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM416S1021BT-G8

(Unit : Number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	56ns	24ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	7	3	2	3	1	1	1
100MHz (10.0ns)	3	8	6	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	4	2	1	2	1	1	1

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	DQM	BA	A10/AP	A9 ~ A0	Note
Register	Mode register set	H	X	L	L	L	L	X		OP code		1,2
Refresh	Auto refresh	H	H	L	L	L	H	X		X		3
	Self refresh		Entry									L
		Exit	L	H	L	H	H	H	X	X		3
	H				X							X
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable									H		4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable									H		4,5
Burst stop		H	X	L	H	H	L	X		X		6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	Both banks								X	H		
Clock suspend or active power down	Entry	H	L	H	X	X	X	X		X		
				L	V	V	V					
Precharge power down mode	Entry	H	L	H	X	X	X	X		X		
				L	H	H	H					
	Exit	L	H	H	X	X	X	X		X		
				L	V	V	V					
DQM		H		X				V		X		7
No operation command		H	X	H	X	X	X	X		X		
				L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

- A0 ~ A10/AP, BA : Program keys. (@ MRS)
- 2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.
- 3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
- 4. BA : bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA is ignored and both banks are selected.
- 5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at tRP after the end of burst.
- 6. Burst stop command is valid at every burst length.
- 7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)