YAMAHA

YDA139

D-4

STEREO 2.5W DIGITAL AUDIO POWER AMPLIFIER

■Overview

YDA139 (D-4) is a digital audio power amplifier IC with maximum output of 2.5W (R_L=4Ω)×2ch.
YDA139 has a "Pure Pulse Direct Speaker Drive Circuit" which directly drives speakers while reducing distortion of pulse output signal and reducing noise on the signal, and realizes the highest standard low distortion rate characteristics and low noise characteristics as the same class of output digital amplifier IC.
In addition, circuit design with fewer external parts can be made depend on the condition of use because corresponds to filter less.
YDA139 has the power-down function which can minimize the power consumption in the standby state.
In addition, high speed recovery function provided realizes recovery time within 1ms from the power-down state. Moreover, Over-current Protection function for speaker output terminals, IC Thermal Protection function, and POP Noise Reduction function are provided.
YDA139 supports both digital signal input and analog signal input.

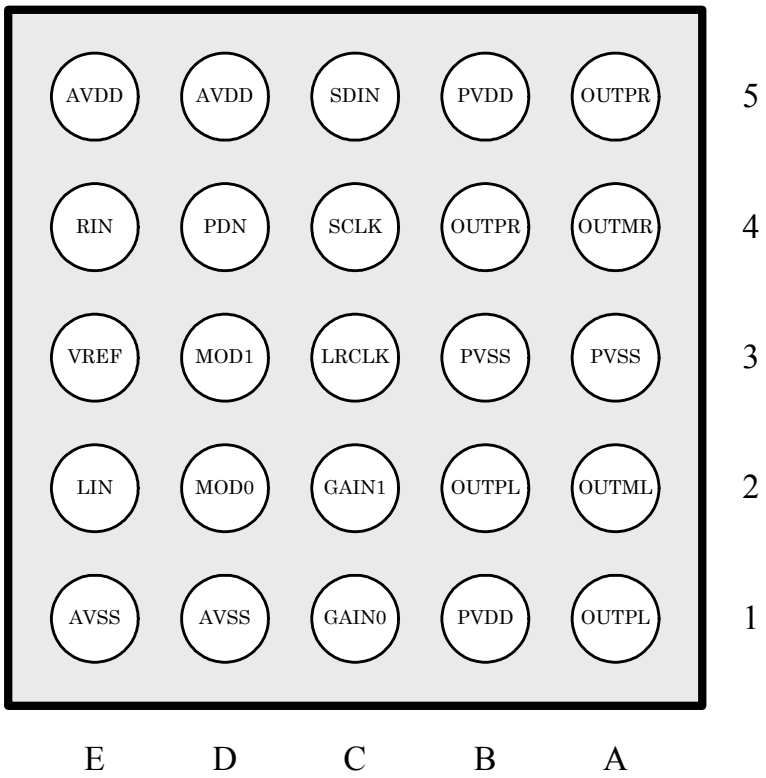
■Features

・Maximum output
WLCSP25
2.5 W×2ch (V_{DDP}=V_{DDA}=5.0V, R_L=4Ω, THD+N=10%)
1.5 W×2ch (V_{DDP}=V_{DDA}=5.0V, R_L=8Ω, THD+N=10%)
SSOP24
2.5 W×2ch (V_{DDP}=V_{DDA}=5.0V, R_L=4Ω, THD+N=10%)
1.3 W×2ch (V_{DDP}=V_{DDA}=5.0V, R_L=8Ω, THD+N=10%)
・Efficiency
WLCSP25
91 % (Analog input mode, V_{DDP}=V_{DDA}=5.0V, R_L=8Ω, Po=1.5W)
SSOP24
88 % (Analog input mode, V_{DDP}=V_{DDA}=5.0V, R_L=8Ω, Po=1.5W)
・Distortion Rate (THD+N)
0.03 % (Analog input mode, V_{DDP}=V_{DDA}=5.0V, R_L=8Ω, Po=0.65W)
・S/N Ratio
99dB (Analog input mode, V_{DDP}=V_{DDA}=5.0V, Gain[1:0]=L,L)
・Over-current Protection function
・Thermal Protection function
・Low voltage Malfunction Prevention function
・Power-down function by PDN terminal
・Power-down High speed Recovery function
・Package
Lead-free 25-ball WLCSP (YDA139-WZ)
Lead-free 24-pin SSOP (YDA139-EZ)

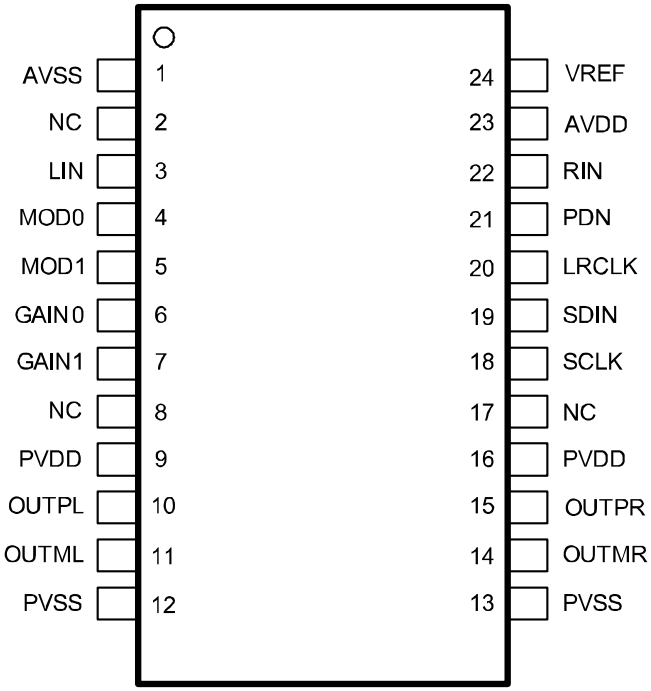
YAMAHA CORPORATION

YDA139 CATALOG
CATALOG No.:LSI-4DA139A30
2006.2

■Terminal configuration



<25-ball WLCSP Bottom View>



<24-pin SSOP Top View>

■Terminal function

・WLCSP25

No.	Name	I/O	Function
A1	OUTPL	O	Positive differential output terminal Lch 1
A2	OUTML	O	Negative differential output terminal Lch
A3	PVSS	GND	GND for output
A4	OUTMR	O	Negative differential output terminal Rch
A5	OUTPR	O	Positive differential output terminal Rch 1
B1	PVDD	Power	Power supply for output (non-regulated)
B2	OUTPL	O	Positive differential output terminal Lch 2
B3	PVSS	GND	GND 2 for output
B4	OUTPR	O	Positive differential output terminal Rch 2
B5	PVDD	Power	Power supply for output
C1	GAIN0	I	Gain setting terminal
C2	GAIN1	I	Gain setting terminal
C3	LRCLK	I	Word clock input terminal
C4	SCLK	I	Bit clock input terminal
C5	SDIN	I	Data clock input terminal
D1	AVSS	GND	GND for analog circuit
D2	MOD0	I	Analog /Digital /Mix mode switching terminal
D3	MOD1	I	Analog /Digital /Mix mode switching terminal
D4	PDN	I	Power-down terminal
D5	AVDD	Power	Power supply for analog circuit
E1	AVSS	GND	GND for analog circuit
E2	LIN	A	Analog input terminal Lch
E3	VREF	A	VREF terminal
E4	RIN	A	Analog input terminal Rch
E5	AVDD	Power	Power supply for analog circuit

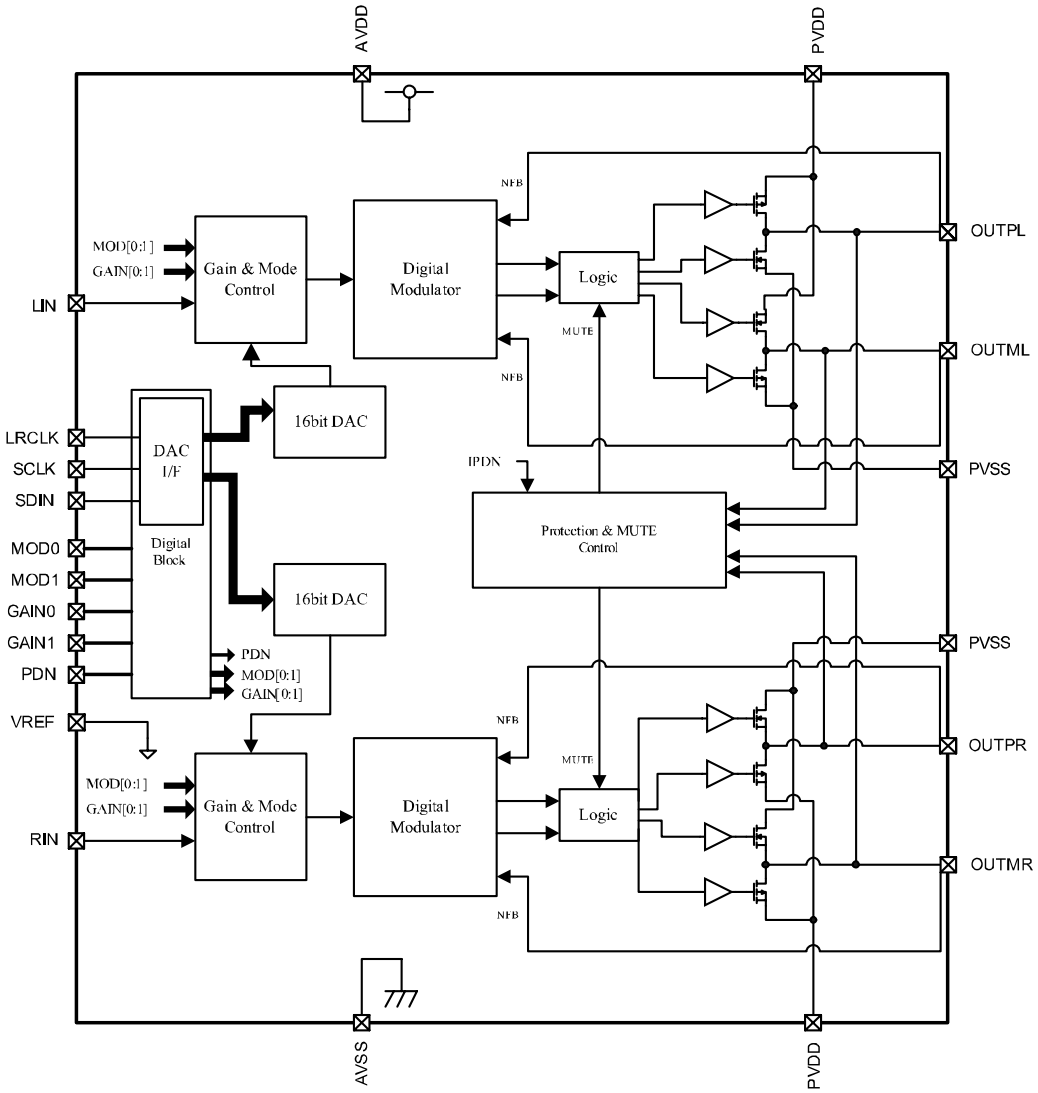
(Note) I: Input terminal O: Output terminal A: Analog terminal

・SSOP24

No.	Name	I/O	Function
1	AVSS	GND	GND for analog circuit
2	NC	-	Non connection.
3	LIN	A	Analog input terminal Lch
4	MOD0	I	Analog /Digital /Mix mode switching terminal
5	MOD1	I	Analog /Digital /Mix mode switching terminal
6	GAIN0	I	Gain setting terminal
7	GAIN1	I	Gain setting terminal
8	NC	-	Non connection.
9	PVDD	Power	Power supply for output
10	OUTPL	O	Positive differential output terminal Lch
11	OUTML	O	Negative differential output terminal Lch
12	PVSS	GND	GND for output
13	PVSS	GND	GND for output
14	OUTMR	O	Negative differential output terminal Rch
15	OUTPR	O	Positive differential output terminal Rch
16	PVDD	Power	Power supply for output
17	NC	-	Non connection.
18	SCLK	I	Bit clock input terminal
19	SDIN	I	Data clock input terminal
20	LRCLK	I	Word clock input terminal
21	PDN	I	Power-down terminal
22	RIN	A	Analog input terminal Rch
23	AVDD	Power	Power supply for analog circuit
24	VREF	A	VREF terminal

(Note) I: Input terminal O: Output terminal A: Analog terminal

■Block diagram



■Description of operating functions

●Digital Amplifier Function

YDA139 has digital amplifiers with analog and digital input, PWM pulse output, Maximum output of 2.5W(R_L=4Ω)×2ch. Distortion of PWM pulse output signal and noise of the signal is reduced by adopting "Pure Pulse Direct Speaker Drive Circuit"

First Stage Amplifier Gain Setting Function

YDA139is composed of the first stage amplifier with gain setting control and a 6dB fixed-gain digital amplifier. Gain of the first stage amplifier can be set by GAIN[1:0] terminal.

Digital Amplifier Gain Setting (Analog Input –Digital Amplifier Output)

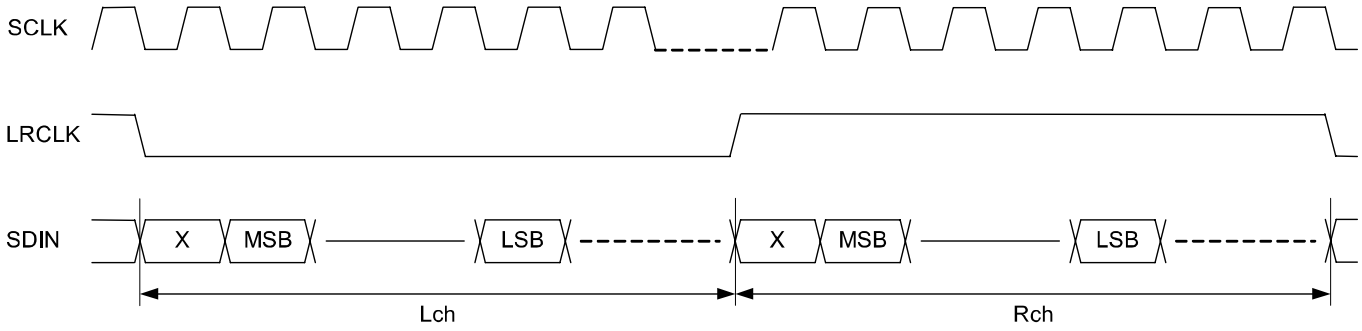
GAIN1	GAIN0	Gain	Input Sensitivity	Input Impedance(Z_{IN})
L	L	12dB	800mVrms	100kΩ
L	H	18dB	400mVrms	66.3kΩ
H	L	21.6dB	250mVrms	50kΩ
H	H	26dB	150mVrms	33.3kΩ

Note） H and L indicates logic High and logic Low, respectively.

Connect a 0.01μF or more capacitor to the audio signal input terminals (LIN and RIN) for the rejection of DC signal.
The input low region cutoff frequency is calculated by $1/(2\times\pi\times Z_{IN}\times C_{IN})$.
When GAIN[0:1]=L,L and C_{IN}=0.01μF, the input low region cutoff frequency becomes 159Hz.
And, half voltage (V_{REF}) of AVDD terminal voltage is output to the reference voltage terminals (VREF). Connect a 1μF or more capacitor to the terminals for voltage stabilization.
*When the input low region cutoff frequency is lowered, capacitor that is larger than 0.01μF (max. 0.1μF) can be connected. However, please note the following points.
(1) The pop noise when the power supply is disconnected might become large. Therefore, correspond by following method.
①After PDN terminal change to "L", disconnect power supply.
②VREF capacitor is set to $C_{REF}=C_{IN}\times 20$[μF].
(2) The recovery time from the power down becomes long. (Refer to the item "Power Down Function" for relation between the recovery time t_{PDR} and C_{IN} and C_{REF}.)

●DAC Function

YDA139 includes a stereo DAC with 44.1kHz, 48kHz/16bit. The output of DAC is amplified by the digital amplifier to output to speakers. The digital signal input supports the following format.
Gain from DAC output to the digital amplifier output is fixed to 12dB. The full scale voltage (V_{FS}) of DAC is depending on AVDD terminal voltage (V_{DDA}) and can be found with the following formula: $V_{FS}=V_{DDA}\times 0.56$.
V_{FS} is amplified 12dB, and it becomes an amplifier output. For example, V_{FS}=1.68V and amplifier output (BTL) =6.72Vpp at V_{DDA}=3V.
Do not input the DC signal to YDA139 because built-in DAC doesn't have the DC cutting function. And, do not stop each clock of SCLK, LRCLK and SDIN at the digital input mode and mixing mode.



Left channel is received when LRCLK is L.
Right channel is received when LRCLK is H.
SDIN and LRCLK are sampled at the rising edge of SCLK.

Digital Signal Input Format (16-bit format with left-justified and a one bit clock delay).

●Mode Selection Function

YDA139 has mode selection function for selecting analog input and digital input. In the digital input mode, DAC output signal is output in 12 dB(fixed) of gain. In the analog input mode, analog signal that was input to LIN/RIN is output in a gain in accordance with the setting of GAIN[1:0] terminal. In the mixing mode, the digital input and analog input is mixed and output.

MOD[1:0] Setting and Operation Mode

MOD1	MOD0	Function
L	L	Digital Input Mode
L	H	Analog Input Mode (DAC Power-down)
H	L	Mixing Mode
H	H	Reserved

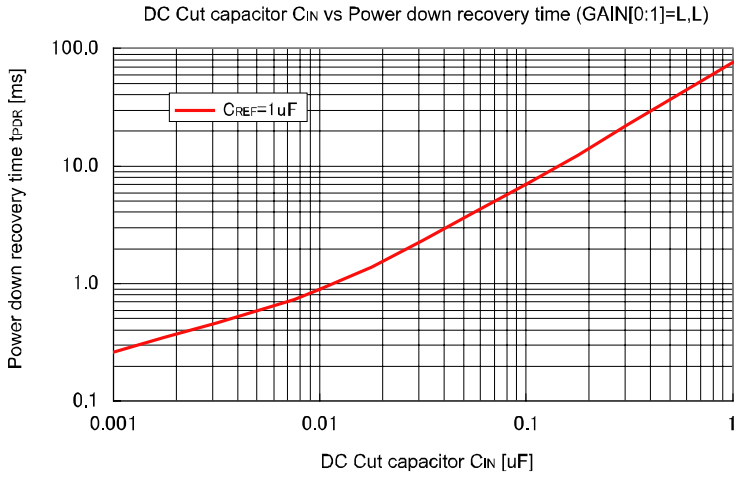
Note) MOD[1:0]=H,H is already reserved by the system.

●Power-down Function

When PDN terminal is L, the power-down mode is selected in YDA139. The mode stops all the circuit functions and minimizes power consumption. At this time, the output stage of the digital amplifier is disabled (WL[*1]). In addition, the High Speed Recovery function allows recovery to the normal operation at 0.8msec (t_{PDR}) when setting PDN to H in the power-down state.

Note)*1: "WL" means output disabled (weak pull-down output).

The relation between power down recovery time (t_{PDR}) and C_{IN} is as follows.



●Protection Function

YDA139 has the following protection functions for the digital amplifier: Over-current Protection function, Thermal Protection function, Low voltage Malfunction Prevention function, and Power supply voltage fluctuation protection function.

Over-current Protection function

This is a function to make the Over-current Protection Mode by detecting a short-circuiting (Ground short/Power supply short/Short between terminals) in the output stage of digital amplifier and to disable (WL) the output stage of the digital amplifier. When entering the Protection Mode, automatically it returns to the normal operation after a given waiting time(T_{WT}). If short circuiting in the output stage continues, the sequence is repeated: short circuit detection, protection mode (T_{WT}), and automatic recovery.

Thermal Protection function

This is a function to make the Thermal Protection Mode by detecting extraordinary high temperature of YDA139 and to disable (WL) the output stage of the digital amplifier. This Protection mode is automatically returned to the normal operation state when internal temperature of YDA139 is lowered sufficiently.

Low voltage Malfunction Prevention function

YDA139 has this Prevention function so as not to cause malfunction in the low power supply voltage. When AVDD voltage becomes lower than $V_{UVLL,}$ the Protection mode is operated to disable (WL) the output stage of the digital amplifier. When AVDD voltage becomes higher than $V_{UVLH,}$ the protection mode is cancelled after a given waiting time and turns into the normal mode.

Power supply Voltage Fluctuation Detection function

YDA139 has this detecting function so that noise may not be generated from speakers when AVDD voltage was lowered significantly. When AVDD voltage becomes lower than $V_{ML,}$ the protection mode is operated to disable (WL) the output stage of the digital amplifier. When AVDD voltage becomes higher than $V_{ML,}$ the protection mode is cancelled and turned into the normal operation mode.

●Pop noise reduction

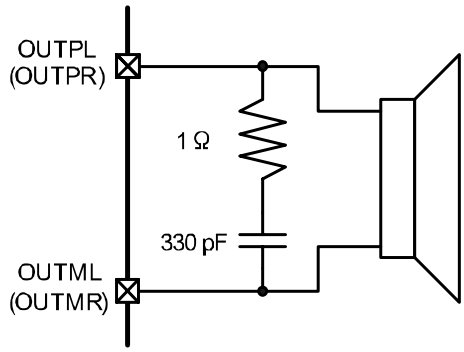
When used in Digital Input mode (MOD[1:0]=L,L) and Mixing mode (MOD[1:0]=H,L), cut power off after setting PDN terminal to “L” in order to reduce the pop noise.

●Snubber Circuit

When use in power supply voltage 4.5V or more, connect the RC snubber circuit between each output terminal (Lch: between OUTPL and OUTML, Rch: between OUTPR and OUTMR, near IC).
The constant and the snubber circuit are as follows.

Power supply voltage range	R	C
4.5 to 5.25V	1Ω	330pF *1

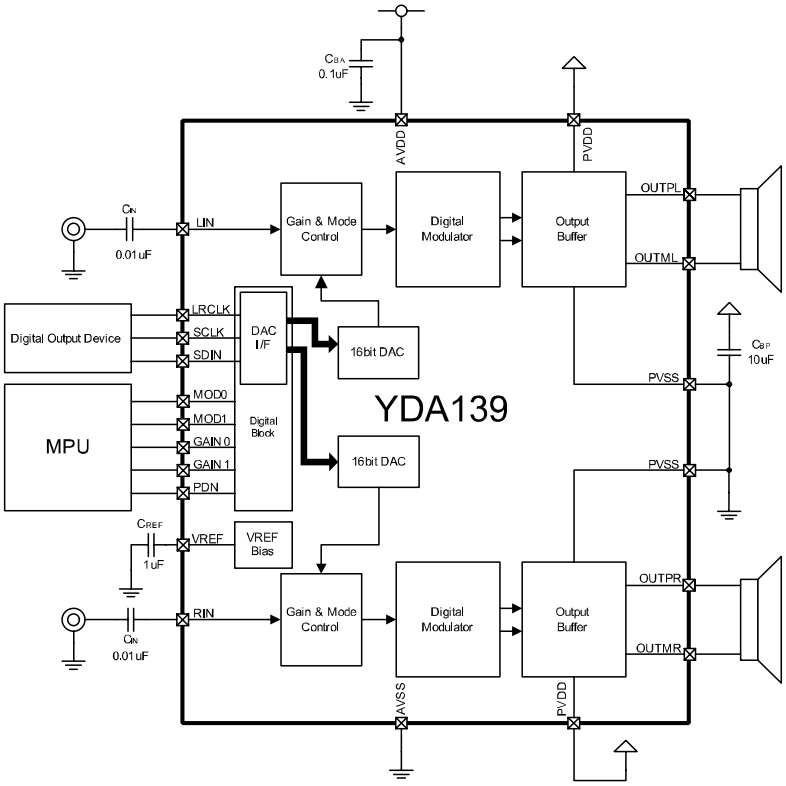
*1: Use the temperature compensated capacitor.



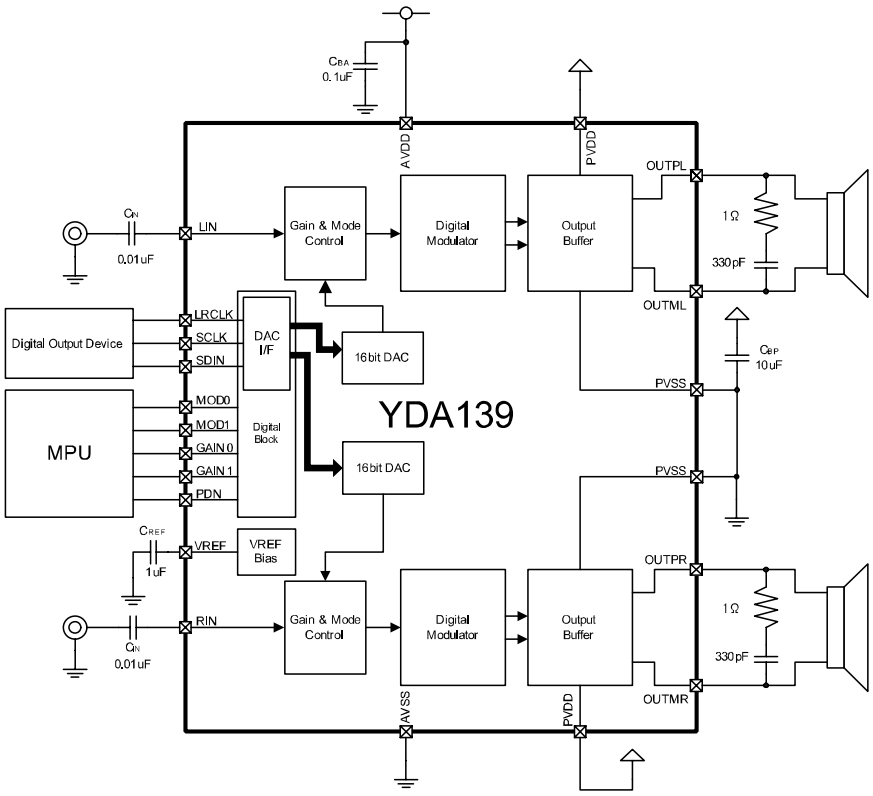
■Application circuit examples

●Correspond to Digital input/Analog input/Mixing mode

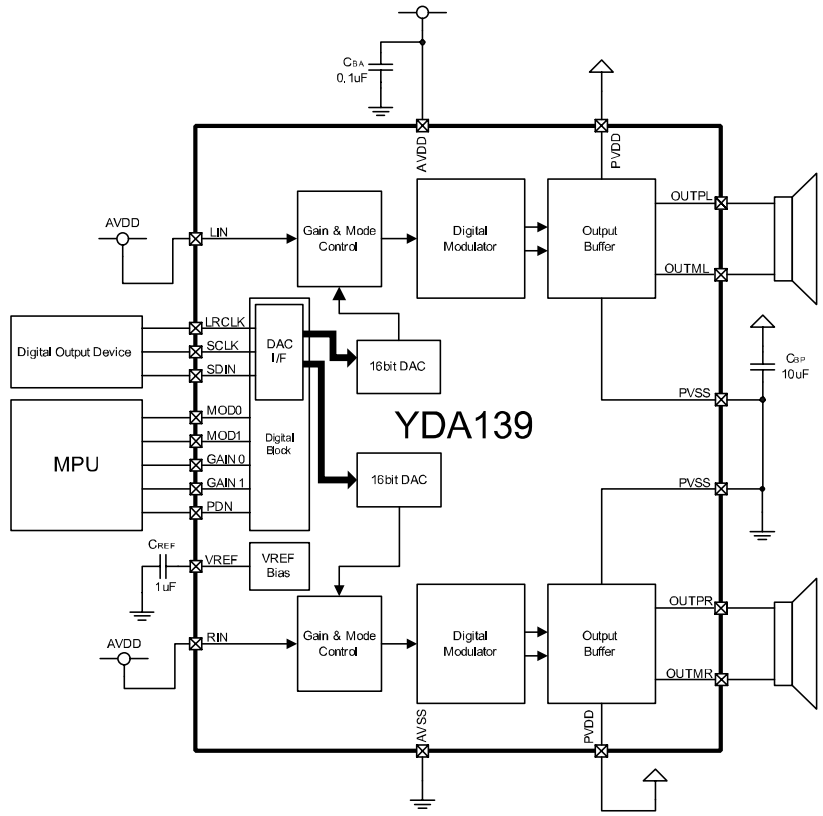
・Snubber circuit is unnecessary. (When use in power supply voltage under 4.5V)



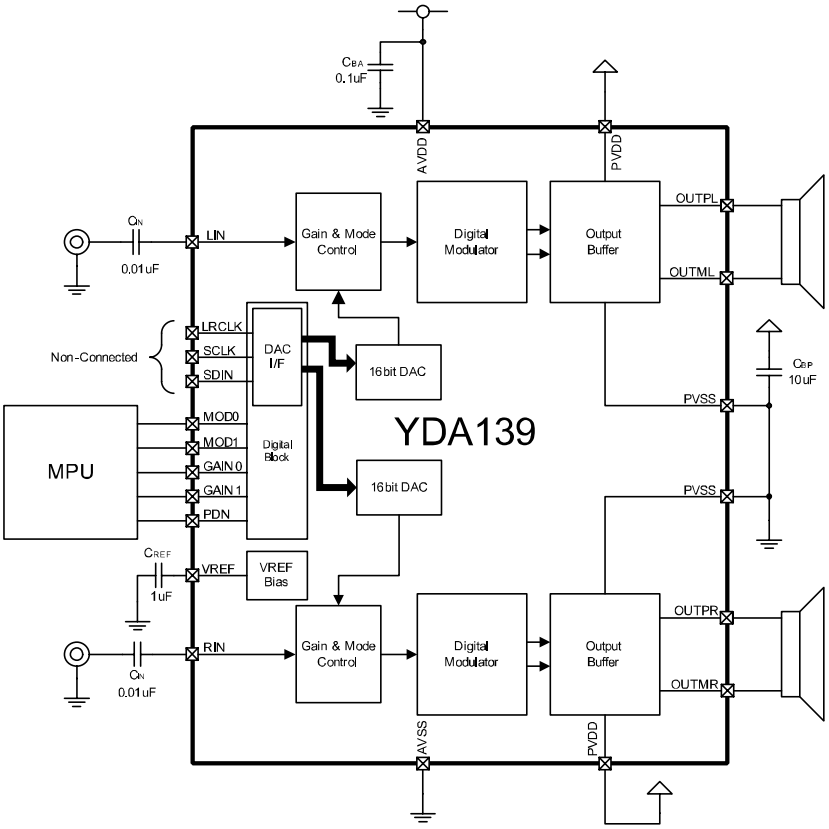
・Snubber circuit is necessary. (When use in power supply voltage 4.5V or more.)



●Correspond to Digital input mode (Without Snubber circuit)



●Correspond to Analog input mode (Without Snubber circuit)



■Electrical Characteristic

●Absolute Maximum Ratings[*1)]

Item	Symbol	Min.	Max.	Unit
Power supply terminal (PVDD) Voltage Range	V_{DDP}	−0.3	6.0	V
Power supply terminal (AVDD) Voltage Range	V_{DDP}	−0.3	6.0	V
Input terminal Voltage Range[*2)]	V_{IN}	V_{SS}−0.3	V_{DDP}+0.3	V
Allowable dissipation (WLCSP25,Ta=25℃)	P_{D25}		1.26	W
Allowable dissipation (WLCSP25,Ta=85℃)	P_{D85}		0.51	W
Allowable dissipation (WLCSP25,Ta=25℃)	P_{D25}		1.03	W
Allowable dissipation (WLCSP25,Ta=70℃)	P_{D70}		0.41	W
Storage Temperature	T_{STG}	−50	125	℃

Note) *1:Absolute Maximum Ratings is values which must not be exceeded to guarantee device reliability and life, and when using a device in excess even a moment, it may immediately cause damage to device or may significantly deteriorate its reliability

*2: Input terminal means MOD0, MOD1, GAIN0, GAIN1, SCLK, SDIN, LRCLK, and PDN terminal.

●Recommended Operating Condition

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage(PVDD)	V_{DDP}	2.7	5	5.25	V
Power Supply Voltage(AVDD)	V_{DDA}	2.7	5	5.25	V
Operating Ambient Temperature	T_a	−20	25	85	℃
Speaker Impedance	R_L	4	-	-	Ω

●DC Characteristics (V_{SS}=0V, V_{DDP}= V_{DDA} =2.7V to 5.25V, Ta=−20ºC to 85ºC, unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output buffer H level output voltage	V_{POH}	I_{OH}=100mA	V_{DDP}−0.1	-	-	V
Output buffer L level output voltage	V_{POL}	I_{OL}=100mA	-	-	0.05	V
AVDD terminal start-up threshold voltage	V_{UVLH}	-	-	2.2	-	V
AVDD terminal shut-down threshold voltage	V_{UVLL}	-	-	2.0	-	V
Power Supply fluctuation shut-down threshold voltage	V_{ML}	-	-	V_{REF} × 1.5[*3)]	-	V
Digital terminal [*4)] H level input voltage	V_{IH}	V_{DDA}=5.25V	2.16	-	-	V
Digital terminal [*4)] H level input voltage	V_{IH}	V_{DDA}=3.3V	1.32			V
Digital terminal [*4)] L level input voltage	V_{IL}	V_{DDA}=2.7V	-	-	0.32	V
VREF output voltage	V_{REF}	V_{DDA}=5V	-	2.5	-	V
Analog mode AVDD terminal consumption current	I_{DD}	V_{DDA}=5V, no load	-	3.3	-	mA
Analog mode PVDD terminal consumption current	I_{DD}	V_{DDP}=5V, no load	-	2.6	-	mA
Digital mode AVDD terminal consumption current	I_{DD}	V_{DDA}=5V, no load	-	6.1	-	mA
Digital mode PVDD terminal consumption current	I_{DD}	V_{DDP}=5V, no load	-	2.6	-	mA
Consumption current in power-down (PDN=L) AVDD terminal + PVDD terminal	I_{PD}	V_{DDA}=V_{DDP}=5V, Ta=25ºC	-	0.1	-	μA

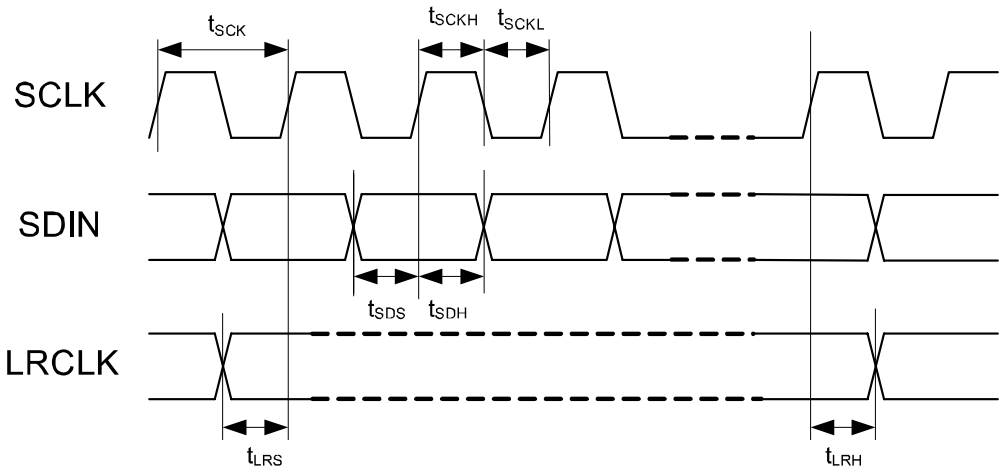
Note) *3: The value when the AVDD power supply voltage becomes 75% or less is meant.

*4: Digital terminal means MOD0, MOD1, GAIN0, GAIN1, SCLK, SDIN, LRCLK, and PDN terminal.

●AC characteristics (V_{SS}=0V, V_{DDP}= V_{DDA} =2.7V to 5.25V, Ta=－20ºC to 85ºC, unless otherwise specified)

Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	$1/T_{SCK}$ *5)	-	3.07	-	MHz
SCLK Hi time	T_{SCKH}	40	-	-	ns
SCLK Lo time	T_{SCKL}	40	-	-	ns
SDIN input set-up time	T_{SDS}	60	-	-	ns
SDIN input hold time	T_{SDH}	25	-	-	ns
LRCLK input set-up time	T_{LRS}	60	-	-	ns
LRCLK input hold time	T_{LRH}	25		-	ns

Note) *5 : $1/T_{SCLK}$=32Fs～64Fs（Fs=44.1kHz, 48kHz）



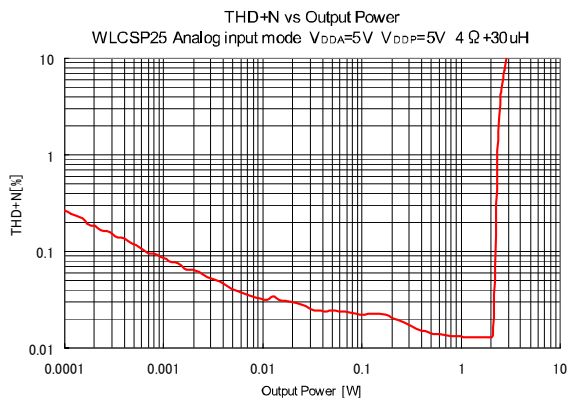
●Analog Characteristics[*6)] (V_{SS}=0V, V_{DDP}= V_{DDA} =5.0V, Ta=25ºC, R_L=8Ω, unless otherwise specified)

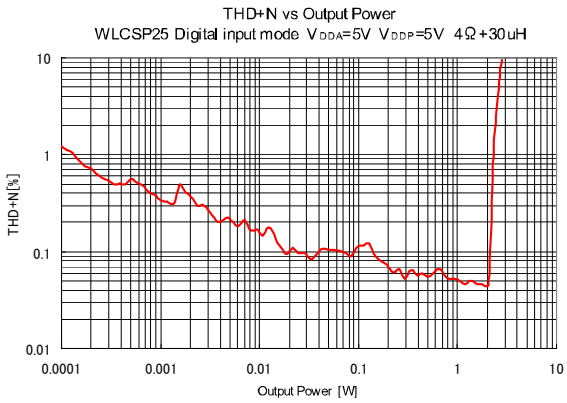
・Digital Amplifier Section

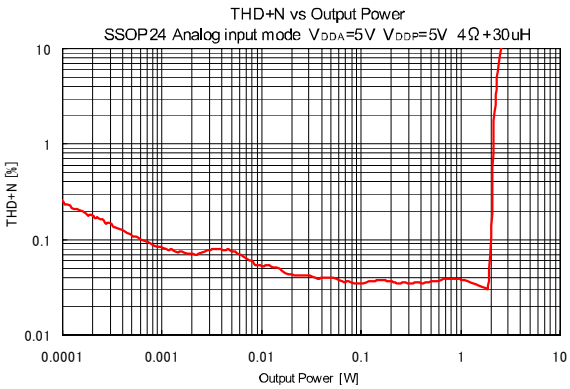
Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Maximum output (WLCSP25)	P_O	R_L=8Ω	V_{DDP}=5.0V,V_{DDA}=5.0V,f=1kHz,THD+N=10%		1.5		W
			V_{DDP}=3.6V,V_{DDA}=3.0V,f=1kHz,THD+N=10%		0.8		W
		R_L=4Ω	V_{DDP}=5.0V,V_{DDA}=5.0V,f=1kHz,THD+N=10%		2.5		W
			V_{DDP}=3.6V,V_{DDA}=3.0V,f=1kHz,THD+N=10%		1.2		W
Maximum output (SSOP24)	P_O	R_L=8Ω	V_{DDP}=5.0V,V_{DDA}=5.0V,f=1kHz,THD+N=10%		1.3		W
			V_{DDP}=3.6V,V_{DDA}=3.0V,f=1kHz,THD+N=10%		0.65		W
		R_L=4Ω	V_{DDP}=5.0V,V_{DDA}=5.0V,f=1kHz,THD+N=10%		2.5		W
			V_{DDP}=3.6V,V_{DDA}=3.0V,f=1kHz,THD+N=10%		1.0		W
Voltage Gain (Analog input mode)	A_V	GAIN[1:0]=L,L			12		dB
		GAIN[1:0]=L,H			18		dB
		GAIN[1:0]=H,L			21.6		dB
		GAIN[1:0]=H,H			26		dB
Total Harmonic Distortion Rate (Analog input mode)	THD+N	R_L=4Ω , P_O=1.25W, f=1kHz, GAIN[1:0]=L,L			0.03		%
		R_L=8Ω , P_O=0.65W, f=1kHz, GAIN[1:0]=L,L			0.03		%
Total Harmonic Distortion Rate (Digital input mode)	THD+N	R_L=4Ω , P_O=1.25W, f=1kHz			0.05		%
		R_L=8Ω , P_O=0.65W, f=1kHz			0.05		%
Signal /Noise Ratio (Analog input mode)	SNR	R_L=8Ω , P_O=1.5W, A-Weight, GAIN [1:0]=L,L			99		dB
Signal /Noise Ratio (Digital input mode)	SNR	R_L=8Ω , P_O=1.5W, A-Weight			98		dB
Channel Separation Ratio	CS	1kHz, GAIN[1:0]=L,L			85		dB
Power supply rejection ratio[*7)]	PSRR	V_{DDP}=5.0V, V_{DDA}=5.0V, f=217Hz			80		dB
		V_{DDP}=3.6V, V_{DDA}=3.0V, f=217Hz			90		dB
Maximum Efficiency (WLCSP25)	η	R_L=8Ω , P_O=1.5W			91		%
Maximum Efficiency (SSOP24)	η	R_L=8Ω , P_O=1.5W			88		%
Output offset voltage (Analog input mode)	Vo	-			±10		mV
Output offset voltage (Digital input mode)	Vo	-			±20		mV
Frequency characteristics (Analog input mode)	f_{RES}	C_{IN} =0.01uF , f=200Hz			−3/+1		dB
		C_{IN} =0.01uF , f=20kHz			±1		dB
Frequency characteristics (Digital input mode)	f_{RES}	f=20Hz			±1		dB
		f=20kHz			±1		dB
Carrier clock frequency	f_{SW}	AVDD=5V		-	920	-	kHz
Over-current protection mode recovery time	T_{WT}	C_{VREF}=1uF, C_{IN}=0.01uF		-	300	-	ms
Start-up time when power supply rise	T_{PS}	C_{VREF}=1uF, C_{IN}=0.01uF		-	400	-	ms
Power-down recovery time	T_{PDR}	C_{VREF}=1uF, C_{IN}=0.01uF		-	0.8	-	ms

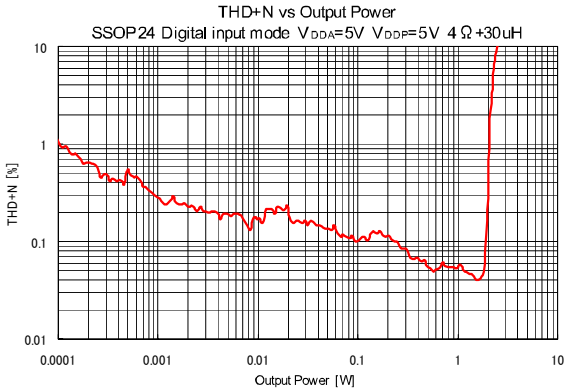
Note) *6:All the values of analog characteristics were obtained by using our evaluation circumstance.
Depending upon parts and pattern layout to use, characteristics may be changed.
*7:AVDD and PVDD are different power supply.
*8:Measurements in V_{DDP}=5V is the value in which snubber circuit (1Ω+330pF) is mounted.

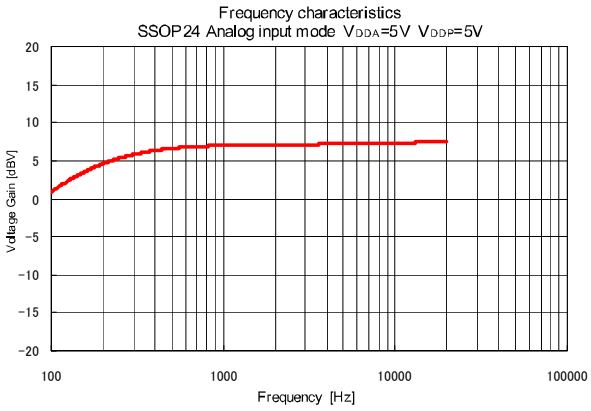
●Typical characteristics examples (V_{DDP}= V_{DDA} =5.0V, Ta=25ºC, R_L=8Ω+30 μ H, unless otherwise specified)

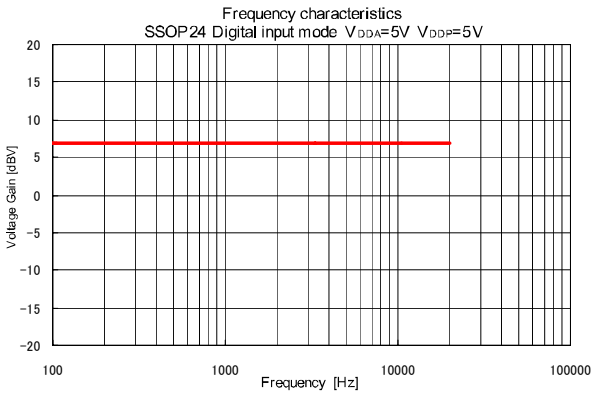


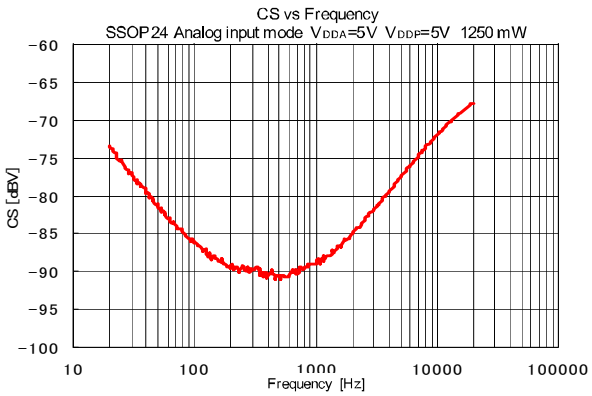


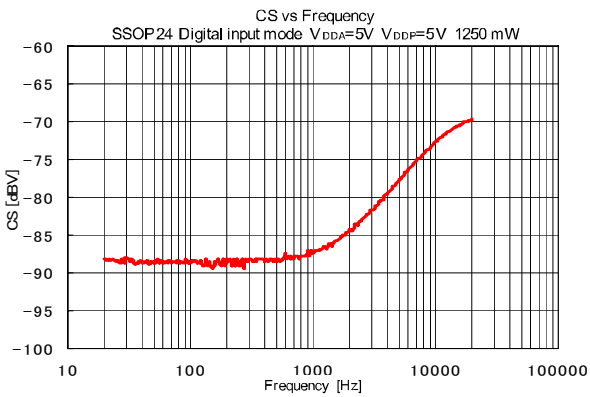


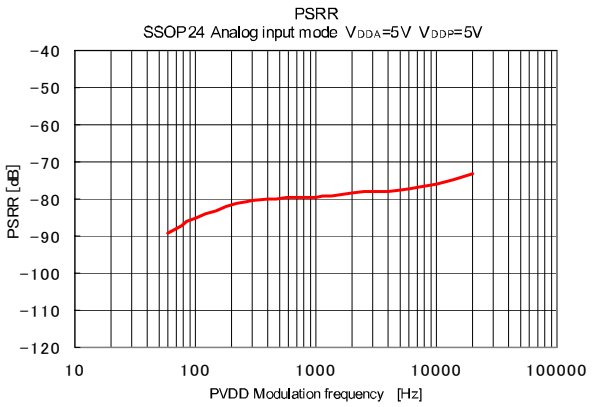


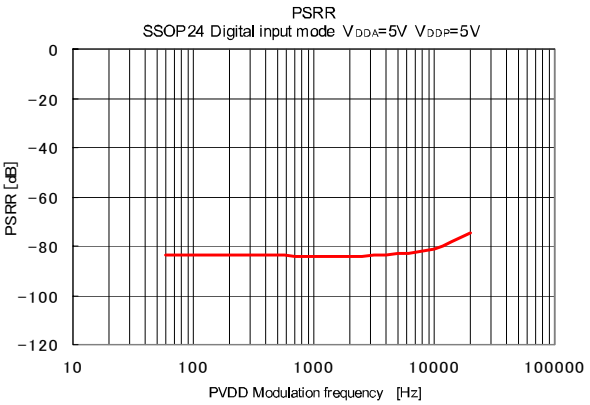




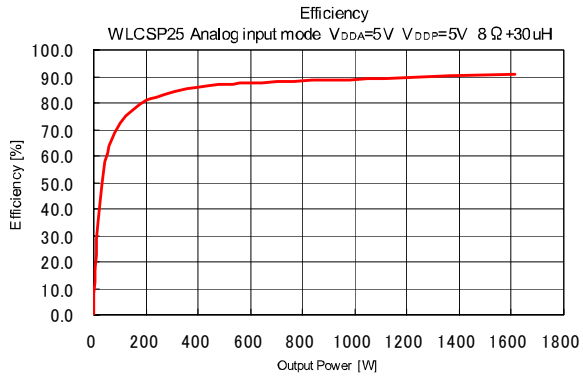


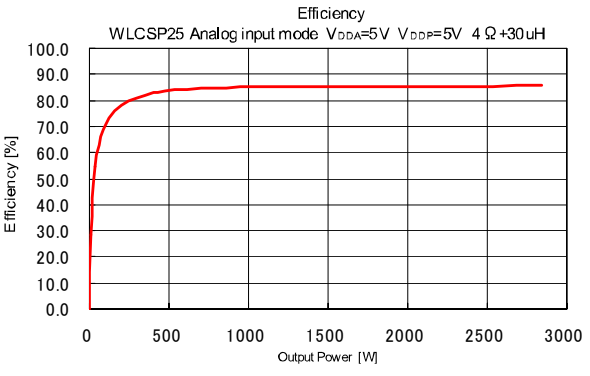


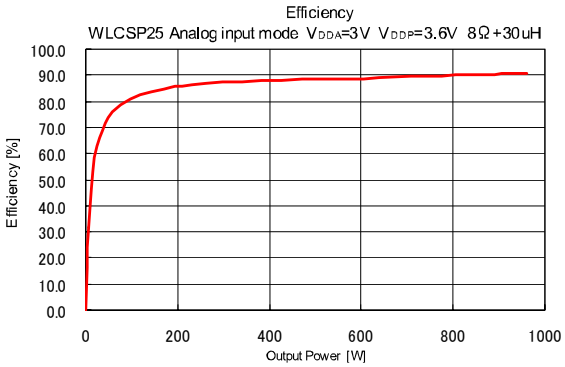


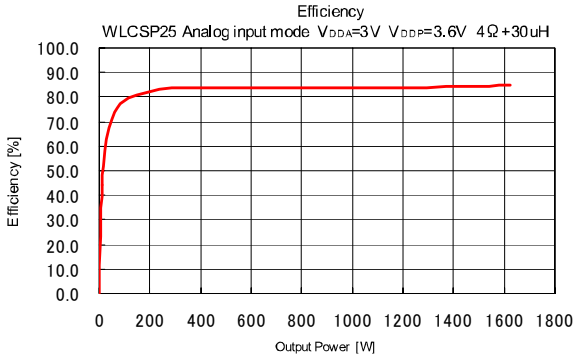


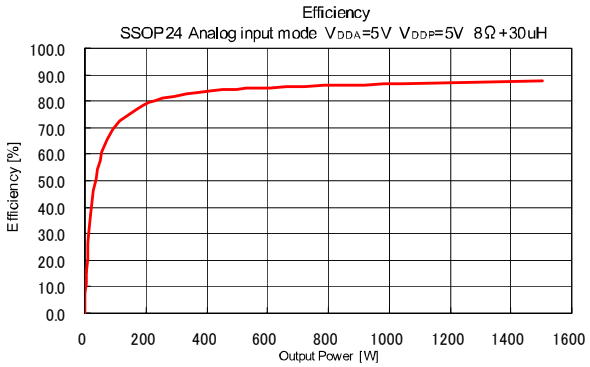
Note) The frequency characteristics, channel separation (CS), and power supply rejection ratio (PSRR) are almost equal characteristics regardless of the package.

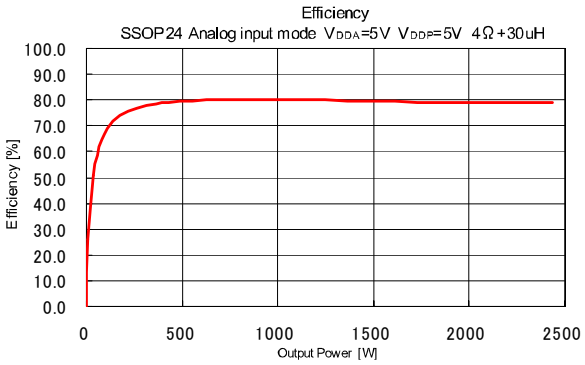


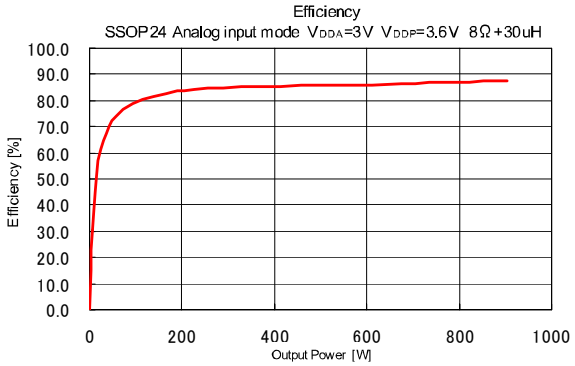


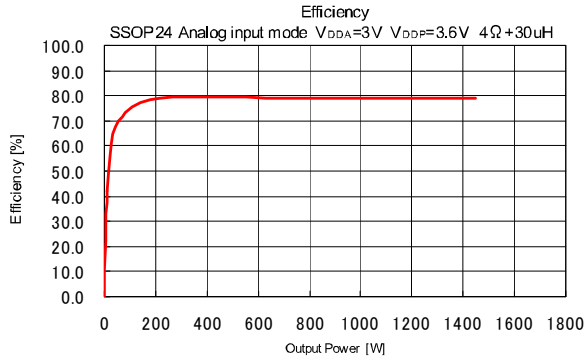








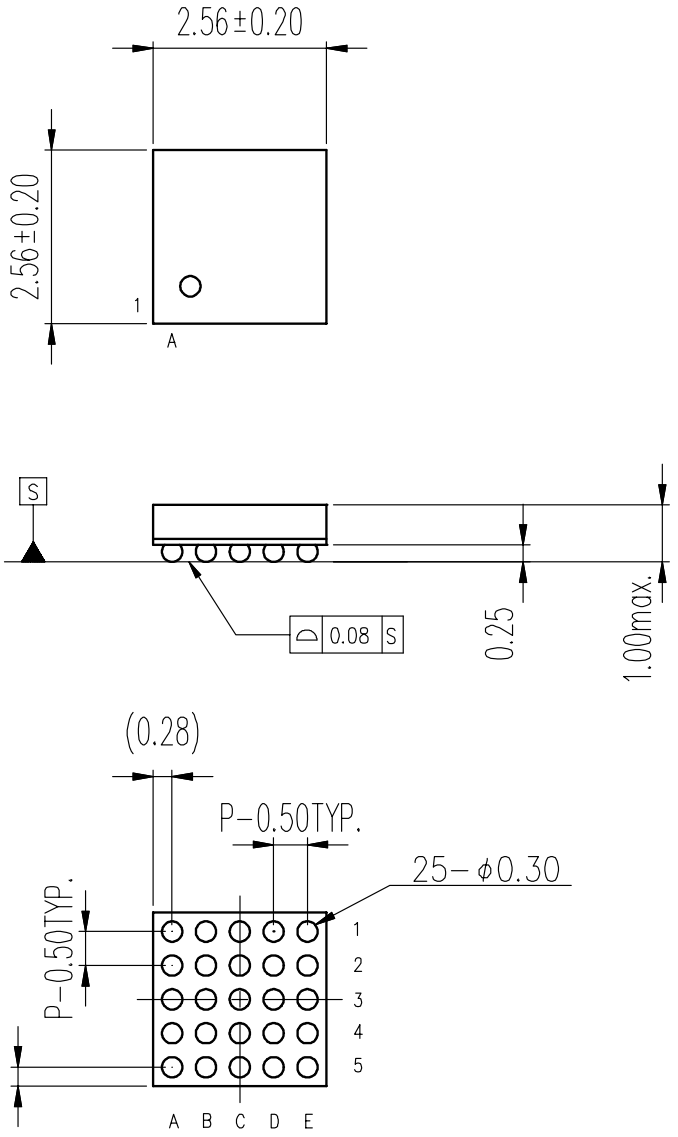




Note) Measurements in V_{DDP}=5V is the value in which snubber circuit (1Ω+330pF) is mounted.

■Package Outline

C-PK25WP-2



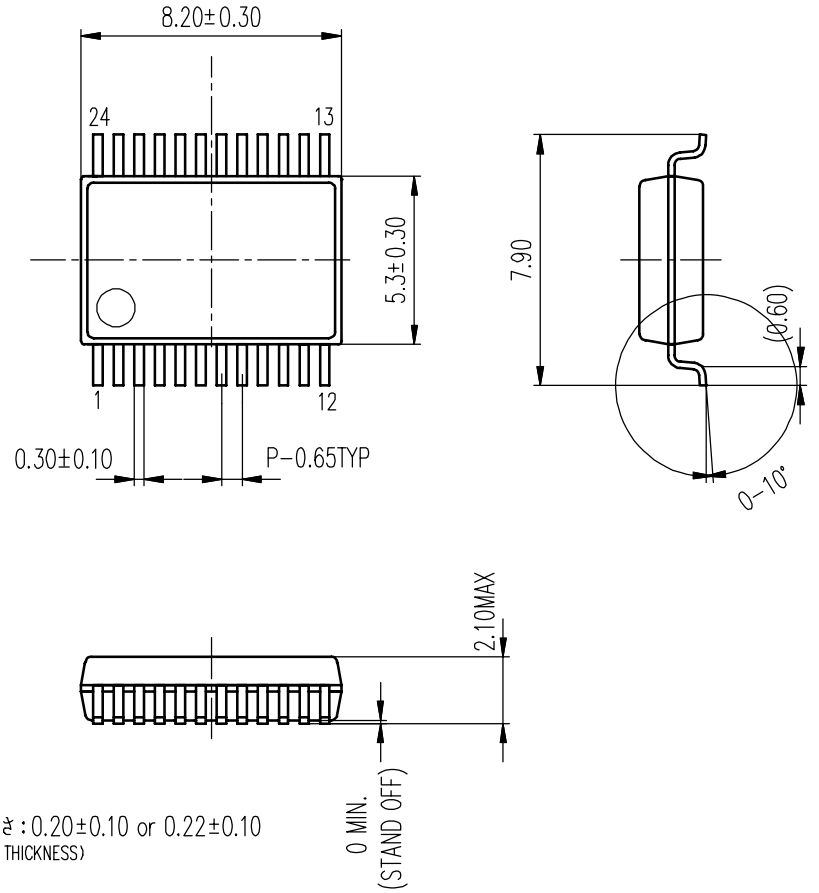
モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みます。
単位： mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.

C-PK24EP-1



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
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