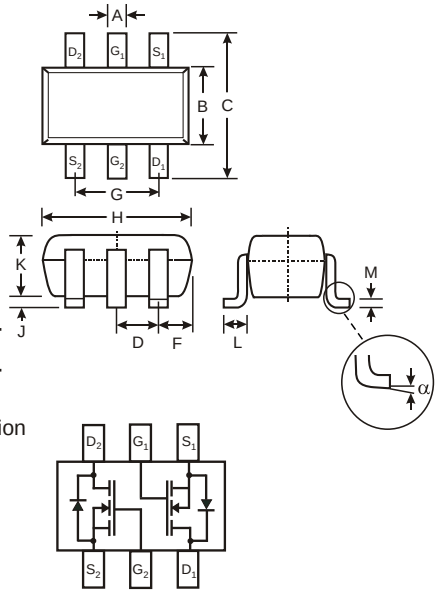
2N7002DW

DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

Features

- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- **Lead Free/RoHS Compliant (Note 2)**
- **Qualified to AEC-Q101 Standards for High Reliability**



SOT-363		
Dim	**Min**	**Max**
A	0.10	0.30
B	1.15	1.35
C	2.00	2.20
D	0.65 Nominal	
F	0.30	0.40
H	1.80	2.20
J	¾	0.10
K	0.90	1.00
L	0.25	0.40
M	0.10	0.25
α	0°	8°
All Dimensions in mm		

Mechanical Data

- Case: SOT-363
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminals: Solderable per MIL-STD-202, Method 208
- Lead Free Plating (Matte Tin Finish annealed over Alloy 42 leadframe).
- Terminal Connections: See Diagram
- Marking (See Page 2): K72
- Ordering & Date Code Information: See Page 2
- Weight: 0.006 grams (approx.)

Maximum Ratings @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	2N7002DW	Units
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage $R_{GS} \le 1.0M\Omega$	V_{DGR}	60	V
Gate-Source Voltage (Note 1) Continuous Pulsed	V_{GSS}	±20 ±40	V
Drain Current (Note 1) Continuous Continuous @ 100°C Pulsed	I_D	115 73 800	mA
Total Power Dissipation Derating above T_A = 25°C (Note 1)	P_d	200 1.60	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	625	°C/W
Operating and Storage Temperature Range	T_j, T_{STG}	-55 to +150	°C

Notes:
1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.
2. No purposefully added lead.

Electrical Characteristics @ T_A = 25°C unless otherwise specified

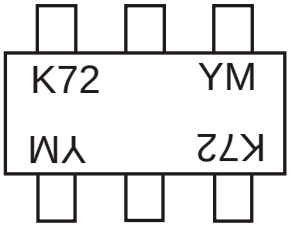
Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 3)							
Drain-Source Breakdown Voltage		BV_{DSS}	60	70	¾	V	V_{GS} = 0V, I_D = 10µA
Zero Gate Voltage Drain Current	@ T_C = 25°C @ T_C = 125°C	I_{DSS}	¾	¾	1.0 500	µA	V_{DS} = 60V, V_{GS} = 0V
Gate-Body Leakage		I_{GSS}	¾	¾	±10	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage		$V_{GS(th)}$	1.0	¾	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	@ T_j = 25°C @ T_j = 125°C	$R_{DS\ (ON)}$	¾	3.2 4.4	7.5 13.5	Ω	V_{GS} = 5.0V, I_D = 0.05A V_{GS} = 10V, I_D = 0.5A
On-State Drain Current		$I_{D(ON)}$	0.5	1.0	¾	A	V_{GS} = 10V, V_{DS} = 7.5V
Forward Transconductance		g_{FS}	80	¾	¾	mS	V_{DS} =10V, I_D = 0.2A
DYNAMIC CHARACTERISTICS							
Input Capacitance		C_{iss}	¾	22	50	pF	V_{DS} = 25V, V_{GS} = 0V f = 1.0MHz
Output Capacitance		C_{oss}	¾	11	25	pF	
Reverse Transfer Capacitance		C_{rss}	¾	2.0	5.0	pF	
SWITCHING CHARACTERISTICS							
Turn-On Delay Time		$t_{D(ON)}$	¾	7.0	20	ns	V_{DD} = 30V, I_D = 0.2A, R_L = 150Ω, V_{GEN} = 10V, R_{GEN} = 25Ω
Turn-Off Delay Time		$t_{D(OFF)}$	¾	11	20	ns	

Ordering Information (Note 4)

Device	Packaging	Shipping
2N7002DW-7-F	SOT-363	3000/Tape & Reel

Notes: 3. Short duration test pulse used to minimize self-heating effect.
4. For Packaging Details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information



K72= Product Type Marking Code
YM = Date Code Marking
Y = Year ex: N = 2002
M = Month ex: 9 = September

Date Code Key

Year	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009
Code	J	K	L	M	N	P	R	S	T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

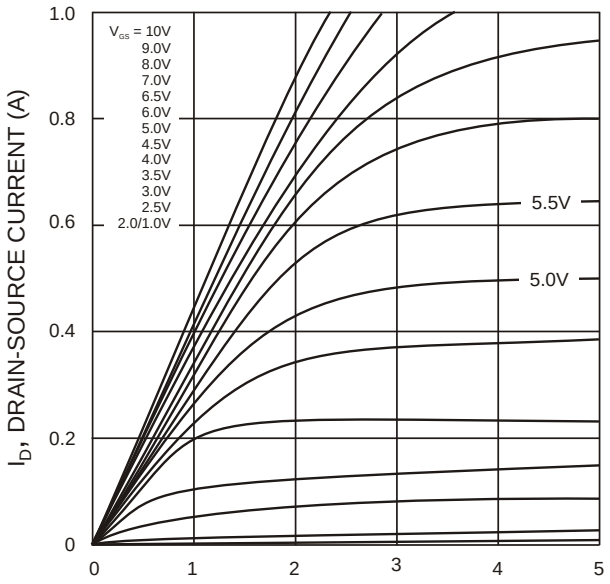


Fig. 1 On-Region Characteristics

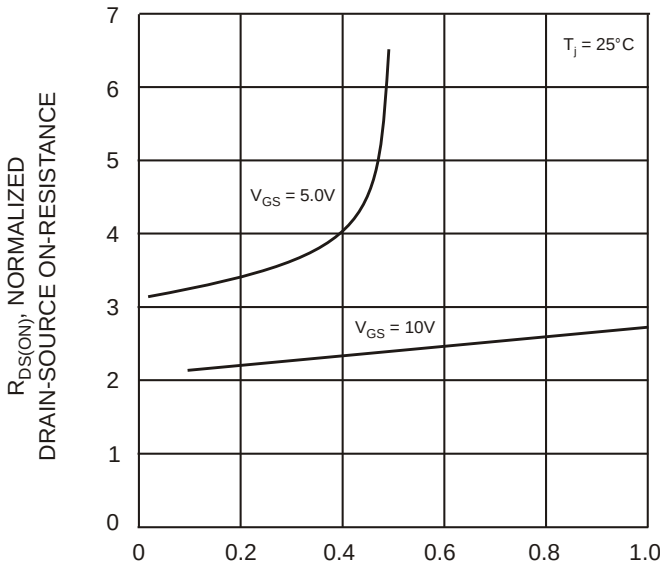


Fig. 2 On-Resistance vs Drain Current

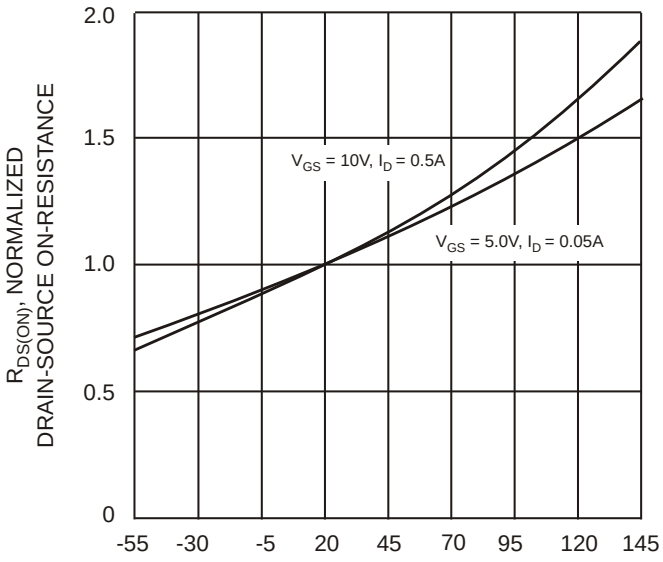


Fig. 3 On-Resistance vs Junction Temperature

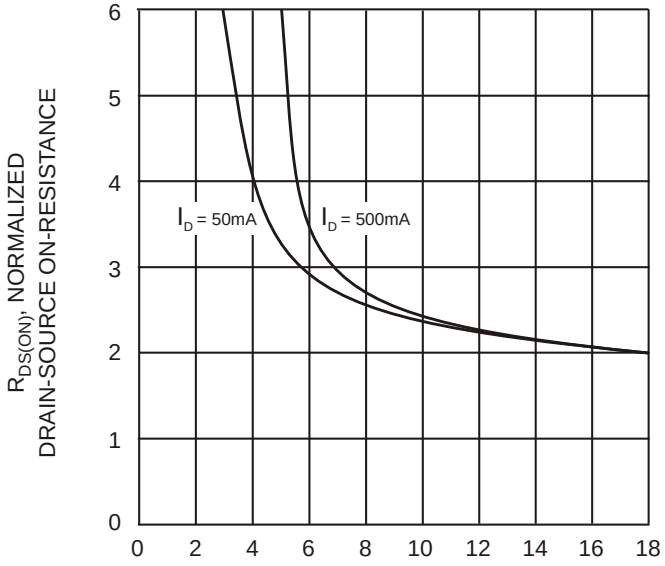


Fig. 4 On-Resistance vs. Gate-Source Voltage