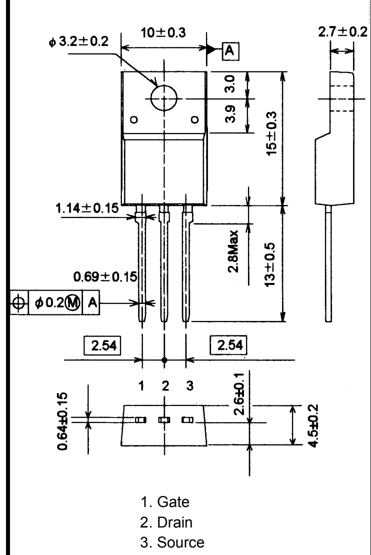
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (π-MOSIV)

2SK3799

Switching Regulator Applications

- Low drain-source ON resistance : $R_{DS\ (ON)}$ = 1.0 Ω (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 6.0 S (typ.)
- Low leakage current : I_{DSS} = 100 μA (max) (V_{DS} = 720 V)
- Enhancement model : V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	―
JEITA	SC-67
TOSHIBA	2-10U1B

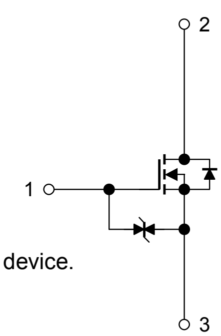
Weight: 1.7 g (typ.)

Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	900	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	900	V
Gate-source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	8	A
	Pulse (Note 1)	I_{DP}	24	A
Drain power dissipation		P_D	50	W
Single pulse avalanche energy (Note 2)		E_{AS}	1080	mJ
Avalanche current		I_{AR}	8	A
Repetitive avalanche energy (Note 3)		E_{AR}	5	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	2.5	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	62.5	°C / W



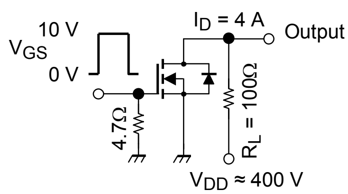
Note 1: Ensure that the channel temperature does not exceed 150°C during use of the device.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 30.9 mH, R_G = 25Ω, I_{AR} = 8 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature.

This transistor is an electrostatic-sensitive device. Handle with care.

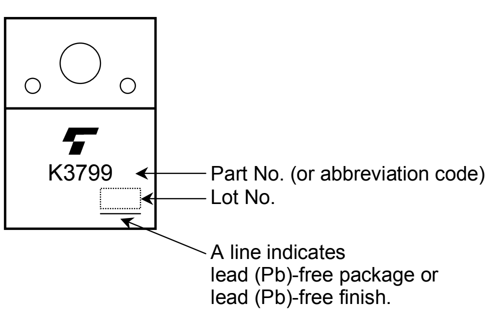
Electrical Characteristics (Ta = 25°C)

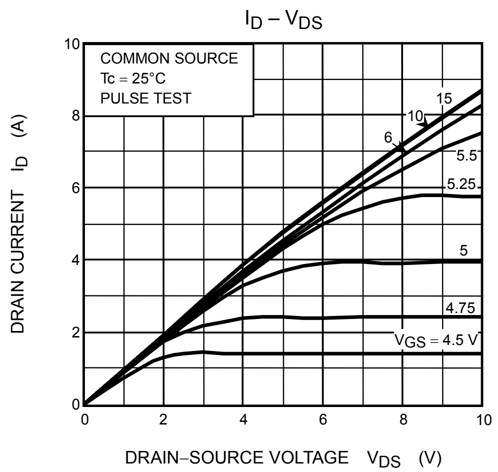
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	—	—	±10	μA
Drain-source breakdown voltage		$V_{(BR)\ GSS}$	I_G = ±10 μA, V_{GS} = 0 V	±30	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 720 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	450	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 4 A	—	1.0	1.3	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 15 V, I_D = 4 A	3.5	6.0	—	S
Input capacitance		C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	—	2200	—	pF
Reverse transfer capacitance		C_{rss}		—	45	—	
Output capacitance		C_{oss}		—	190	—	
Switching time	Rise time	t_r	 Duty ≤ 1%, t_w = 10 μs	—	25	—	ns
	Turn-on time	t_{on}		—	65	—	
	Fall time	t_f		—	20	—	
	Turn-off time	t_{off}		—	120	—	
Total gate charge (Gate-source plus gate-drain)		Q_g	V_{DD} ≈ 400 V, V_{GS} = 10 V, I_D = 8 A	—	60	—	nC
Gate-source charge		Q_{gs}		—	34	—	
Gate-drain ("miller") charge		Q_{gd}		—	26	—	

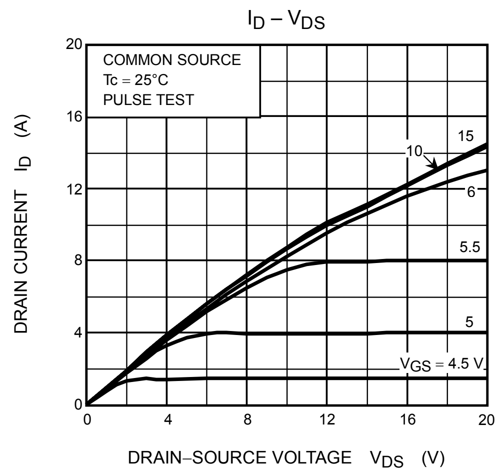
Source-Drain Ratings and Characteristics (Ta = 25°C)

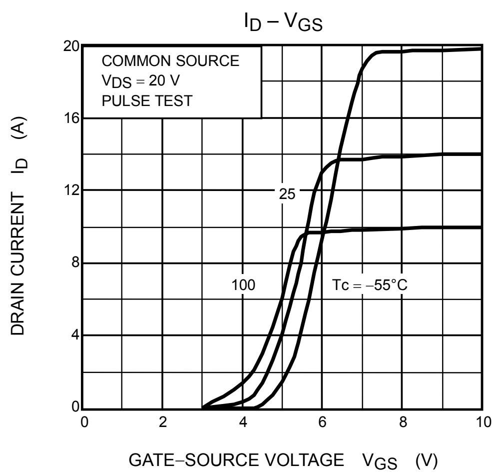
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	8	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	24	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 8 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 8 A, V_{GS} = 0 V dI_{DR} / dt = 100 A / μS	—	1700	—	ns
Reverse recovery charge	Qrr		—	23	—	μC

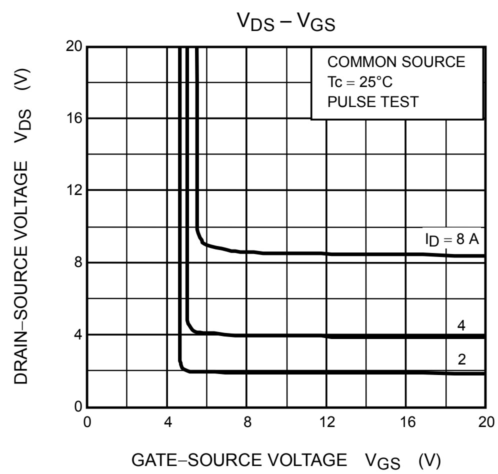
Marking

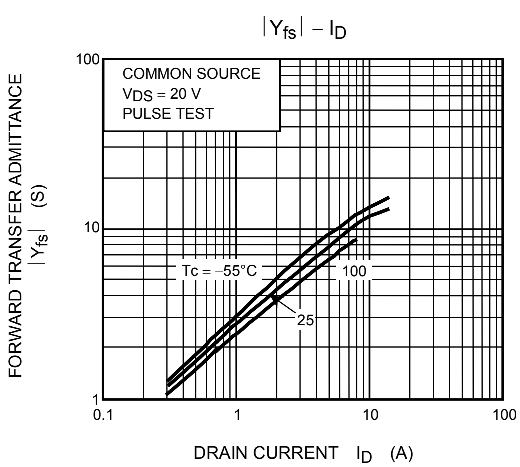


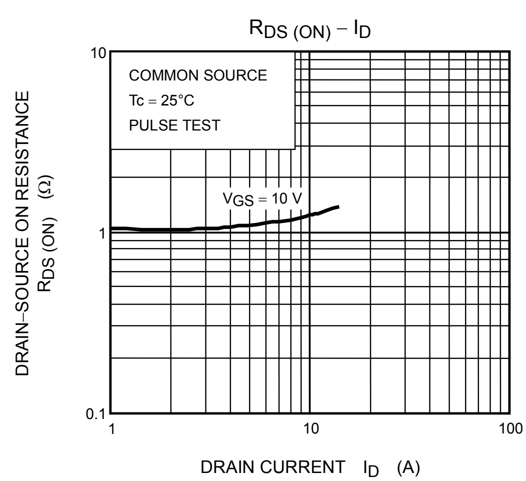

I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
15
10
6
5.5
5.25
5
4.75
V_{GS} = 4.5 V
DRAIN CURRENT I_D (A)
DRAIN−SOURCE VOLTAGE V_{DS} (V)
0 2 4 6 8 10

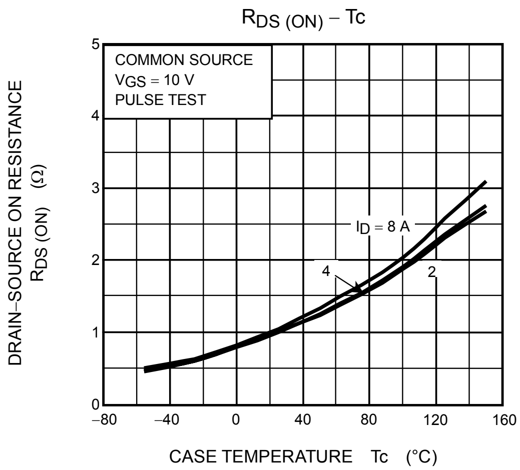

I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
15
10
6
5.5
5
V_{GS} = 4.5 V
DRAIN CURRENT I_D (A)
DRAIN−SOURCE VOLTAGE V_{DS} (V)
0 4 8 12 16 20

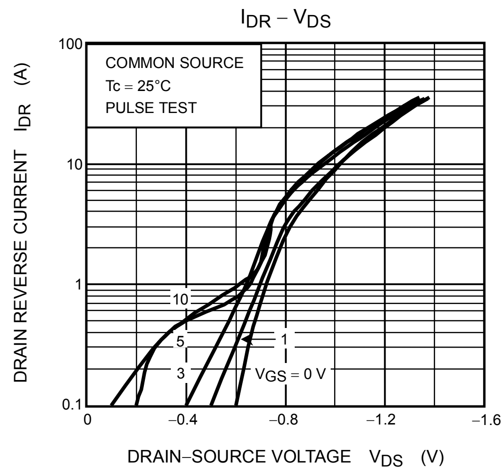

I_D – V_{GS}
COMMON SOURCE
V_{DS} = 20 V
PULSE TEST
25
100
Tc = −55°C
DRAIN CURRENT I_D (A)
GATE−SOURCE VOLTAGE V_{GS} (V)
0 2 4 6 8 10

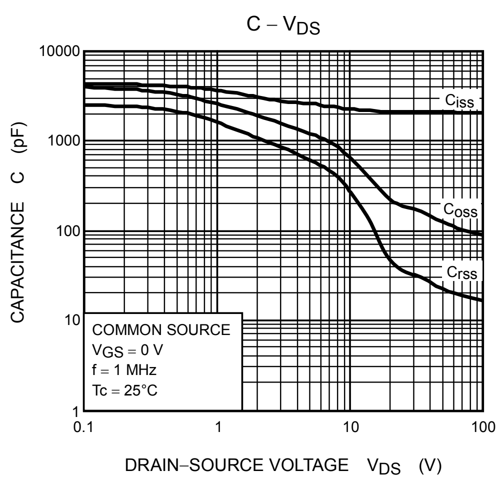

V_{DS} – V_{GS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
I_D = 8 A
4
2
DRAIN−SOURCE VOLTAGE V_{DS} (V)
GATE−SOURCE VOLTAGE V_{GS} (V)
0 4 8 12 16 20

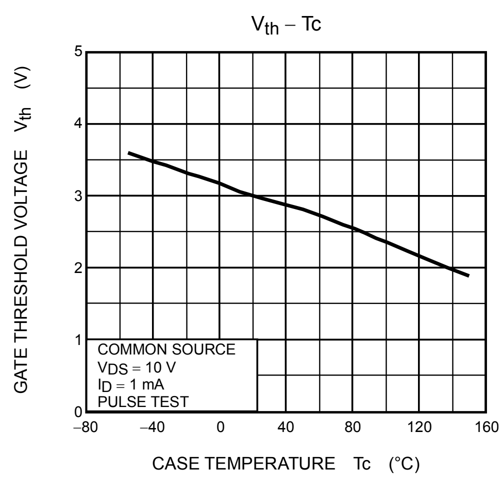

$|Y_{fs}|$ – I_D
COMMON SOURCE
V_{DS} = 20 V
PULSE TEST
Tc = −55°C
100
25
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)
0.1 1 10 100

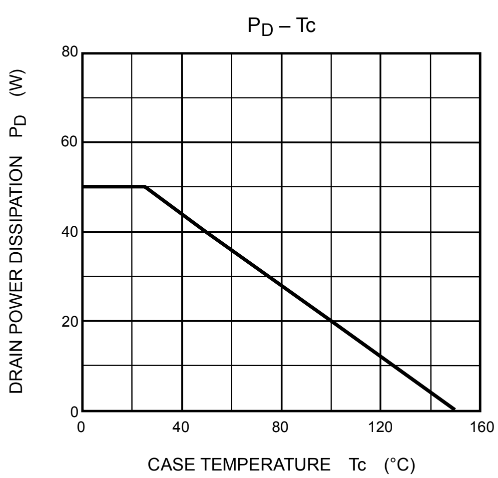

$R_{DS (ON)}$ – I_D
COMMON SOURCE
Tc = 25°C
PULSE TEST
V_{GS} = 10 V
DRAIN−SOURCE ON RESISTANCE $R_{DS (ON)}$ (Ω)
DRAIN CURRENT I_D (A)
1 10 100

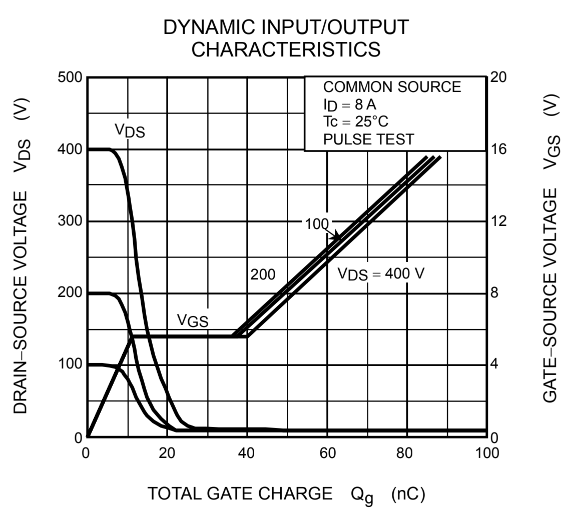

RDS (ON) – Tc
COMMON SOURCE
VGS = 10 V
PULSE TEST
ID = 8 A
4
2
DRAIN−SOURCE ON RESISTANCE RDS (ON) (Ω)
CASE TEMPERATURE Tc (°C)


IDR – VDS
COMMON SOURCE
Tc = 25°C
PULSE TEST
10
5
3
1
VGS = 0 V
DRAIN REVERSE CURRENT IDR (A)
DRAIN−SOURCE VOLTAGE VDS (V)

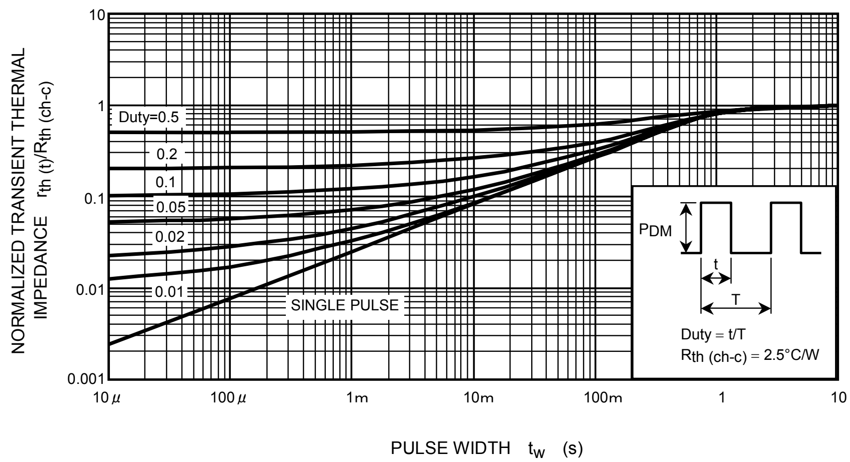

C – VDS
Ciss
Coss
Crss
COMMON SOURCE
VGS = 0 V
f = 1 MHz
Tc = 25°C
CAPACITANCE C (pF)
DRAIN−SOURCE VOLTAGE VDS (V)


Vth – Tc
COMMON SOURCE
VDS = 10 V
ID = 1 mA
PULSE TEST
GATE THRESHOLD VOLTAGE Vth (V)
CASE TEMPERATURE Tc (°C)

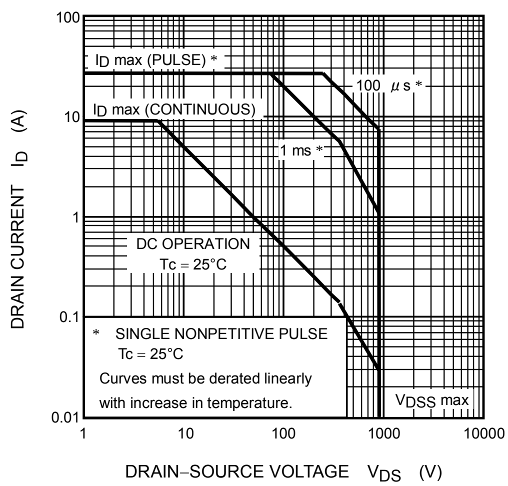

PD – Tc
DRAIN POWER DISSIPATION PD (W)
CASE TEMPERATURE Tc (°C)


DYNAMIC INPUT/OUTPUT CHARACTERISTICS
COMMON SOURCE
ID = 8 A
Tc = 25°C
PULSE TEST
VDS
VGS
100
200
VDS = 400 V
DRAIN−SOURCE VOLTAGE VDS (V)
GATE−SOURCE VOLTAGE VGS (V)
TOTAL GATE CHARGE Qg (nC)

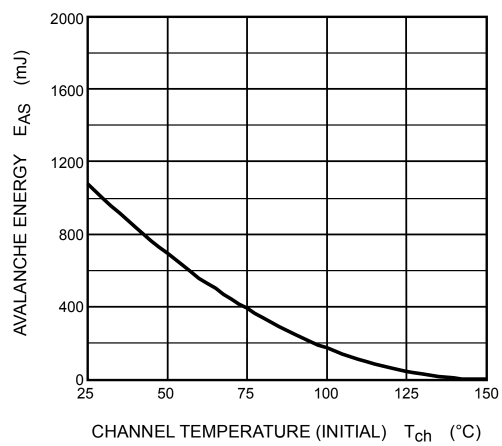
$r_{th} – t_w$

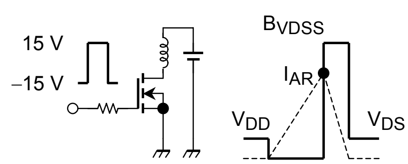


SAFE OPERATING AREA



$E_{AS} – T_{ch}$





TEST CIRCUIT WAVE FORM

$R_G = 25\ \Omega$
$V_{DD} = 90\ V,\ L = 30.9\ mH$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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