### HEADPHONE AMPLIFIER FOR **CD-ROMS**

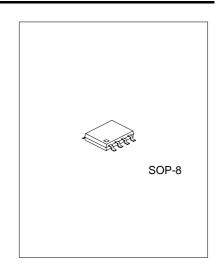
#### **DESCRIPTION**

The UTC 3544 is digital-source dual headphone amplifier. The UTC 3544 has a fixed gain of 6dB so that external gain setting is unnecessary. The UTC 3544 has internal mute function so that prevention of the popping sound when power is turned on and off is greatly simplified. Also, The UTC 3544 is equipped with thermal shutdown circuits to prevent damage from short circuits.

#### **FEATURES**

\*Internal mute function to prevent popping sounds when the power is turned on and off.

\*Built-in thermal shutdown circuit (150 ) to prevent damage to the IC if a short circuit occurs.



\*Pb-free plating product number: 3544L

#### **APPLICATIONS**

Devices that use the headphone output from CD-ROMs, CDs, MDs, personal computers, notebook computers, camcorders, etc.

#### ABSOLUTE MAXIMUM RATINGS(Ta=25)

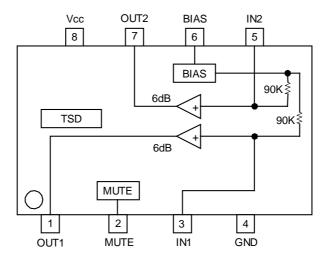
PARAMETER	SYMBOL	RATINGS	UNIT
Applied voltage	Vmax	7.0	V
Power dissipation	$P_{D}$	450 *	mW
Operating temperature	Topr	-25 ~ <b>+</b> 75	
Storage temperature	Tstg	-55 ~ <b>+</b> 125	

<sup>\*</sup>Reduced by 4.5mW for each increase in Ta of 1 over 25

#### RECOMMENDED OPERATING CONDITIONS (Ta=25)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power supply voltage	Vcc	2.8		6.5	V

#### **BLOCK DIAGRAM**



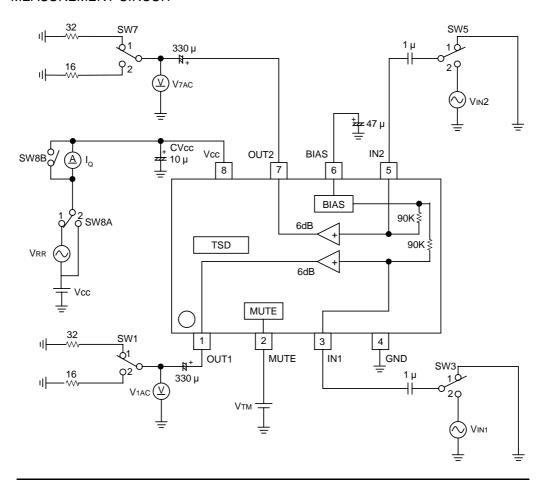
	SCRIPTION			•	
PIN NO.	PIN NAME	I/O	PIN VOLTAGE	INTERNAL EQUIVALENT CIRCUIT	FUNCTION
1	OUT1	0	2.1V	1 7 \$10k	Output pin
7	OUT2	0	2.1V (Vcc=5V)		
2	MUTE	ı	0.1V (When open)	2   VCC   VC	Mute control pin (set to low for prevention of popping noise when power is turned on and off). Operating: High Muting: Low(open)
				Vcc	Input pin
3	IN1 IN2	ı	2.1V 2.1V (Vcc=5V)	3 5 \$180k BIAS	
6	BIAS	I/O	2.1V (Vcc=5V)	Vcc	Bias pin(the external 47 µ F capacitor also serves as the anti-pop time constant, therefore make the proper considerations be changing it).
4	GND	ı	-		
5	Vcc	ı	-		

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ELECTRICAL CHARACTERISTICS (Ta=25 ,Vcc=5.0V,RL=32 ,V<sub>IN</sub>= -6dBV, f=1kHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Quiescent current	ΙQ	V <sub>IN</sub> =0Vrms	4	7	10	mA
Mute pin control voltage	$V_{TM}$		0.3	0.7	1.6	V
Voltage gain	Gvc		4	6	8	dB
Voltage gain difference between channels	Gvc		-0.5	0	0.5	dB
Total harmonic distortion	THD	BW=20 ~ 20kHz		0.02	0.1	%
Rated output 1	Po1	RL=32 ,THD<0.1%	25	31		mW
Rated output 2	Po2	RL=16 ,THD<0.1%	50	62		mW
Output noise voltage	Vno	BW=20 ~ 20kHz,Rg=0		-93	-85	dBV
Channel separation	CS	Rg=0	82	90		dB
Mute attenuation	ATT	Rg=0	70	80		dB
Ripple rejection	RR	frr=100Hz,Vrr= -20dBV	50	57		dB

#### MEASUREMENT CIRCUIT

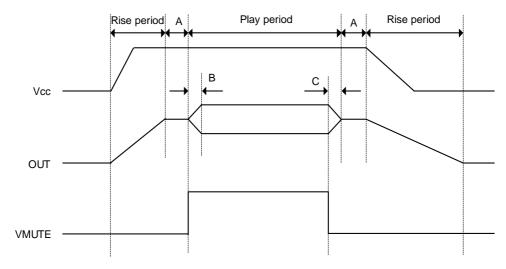


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MEAGONEMENT CONDITIONS								
SIGNAL	SW TABLE				MONITOR	CONDITIONS		
SIGNAL	SW1	SW3	SW5	SW7	SW8A	SW8B	MONTOR	CONDITIONS
ΙQ	1	1	1	1	2	OFF	Ιq	
Vтм								
Gvc	1	2	2	1	2	ON	V1AC,V2AC	f=1kHz,Vin1/2=-6dBV, VTM=1.6V
Gvc								GVC1 – GVC2
THD	1	2	2	1	2	ON	V1AC,V2AC	fin=1kHz,VIN1/2= -6dBV, VTM=1.6V
Po1	1	2	2	1	2	ON	V1AC,V2AC	fin=1kHz,VIN1/2= -6dBV, VTM=1.6V
Po <sub>2</sub>	2	2	2	2	2	ON	V1AC,V2AC	fin=1kHz,VIN1/2= -6dBV, VTM=1.6V
Vno	1	1	1	1	2	ON	V1AC,V2AC	
								fin=1kHz,VIN2= -6dBV,
cs	1	1	2	1	2	ON	V1AC,V2AC	VTM=1.6V
CS	1	2	1	1	2	ON	V1AC,V2AC	fin=1kHz,Vın1= -6dBV,
								VTM=1.6V
ATT	1	2	2	1	2	ON	V1AC,V2AC	fin=1kHz,VIN1/2= -6dBV, VTM=0.3VB
RR	1	1	1	1	1	ON	V1AC,V2AC	VRR= -20dBV, fRR=100Hz

#### **CIRCUIT OPERATION**

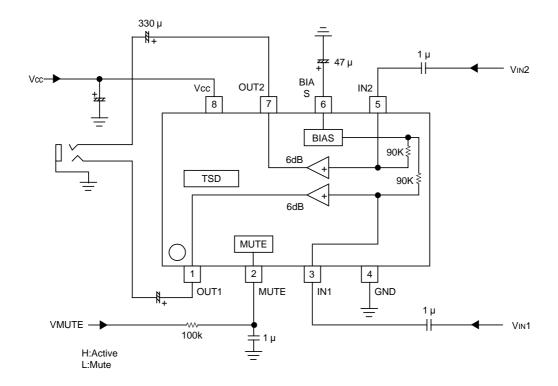
Rising edge timing



- A: MUTE period(use with MUTE=Low to prevent the popping noise when the power is turned on and off).
- B: MUTE release time(used to prevent the popping noise at the release of MUTE with the external C2 and R2 and therefore possesses a time constant, so be careful of the timing).
- C: MUTE start time(also possesses a time constant like the MUTE release time).

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#### APPLICATION EXAMPLE



#### **EXPLANATION OF EXTERNAL XOMPONENTS**

#### (1)Input coupling capacitor(C3 and C5)

Determined by the low-band cut-off frequency. Since the input impedance for this IC is 180k ,it can be determined by the formula below, but take into consideration the fluctuations, ambent temperature, etc. (a multi-layered ceramic capacitor is recommended).

$$C3(C5)=1/(2 \times 180k \times f)$$

#### (2)BIAS capacitor(C6)

47 μ F when Vcc=5V, and 33 μ F when Vcc=3V. If the capacitance is lowered too much, the electrical characteristics will be adversely affected and popping noise may occur. Therefore, take th sufficient considerations before changing these values.

#### (3)MUTE pin for anti-pop measures(R2 and C2)

Possesses an impedance of 190k with respect to GND,so if R2 is increased too much,the MUTE mode may become unable to be released.

#### (4)Output coupling capacitor(C1 and C7)

Determined by the low-band cutoff frequency. As the output load resistance value RL (assuming that for output protection or current limiting, a resistor Rx will be inserted), it can be determined by the formula below.

$$C1(C7)=1/(2 \times (RL+Rx) \times f)$$

#### (5)Input gain adjustment resistor(R3 and R4)

Input gain adjustment can by performed by external resistors R3 and R4,The desired gain can be set by the formula givev below.

Gvc=6+20log(90k /(90k +R3))[ dB ]

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### **ELECTRICAL CHARACTERISTIC CURVES**

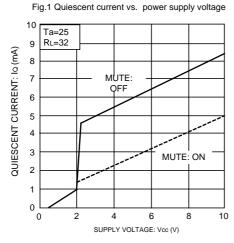
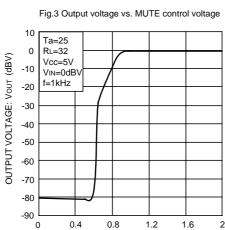
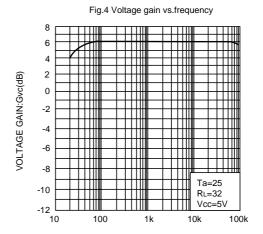


Fig.2 Pin DC current vs. power supply voltage Ta=25 RL=32 OUTPUT DC VOLTAGE: Vo (V) BIAS DC VOLTAGE: VBIAS (V) 3 2 0 6 10 SUPPLY VOLTAGE:Vcc(V)







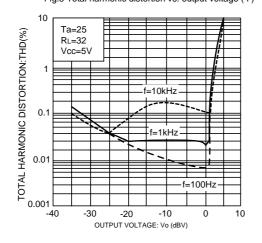


Fig.6 Total harmonic distortion vs. output voltage (II)

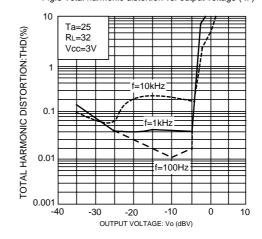


Fig.7 Total harmonic distortion vs. output voltage (III)

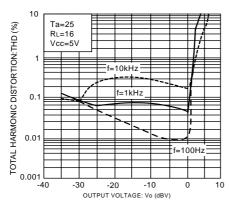


Fig.8 Total harmonic distortion vs. output voltage( IV )

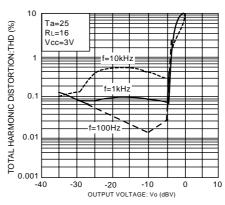


Fig.9 Channel separation vs.frequency

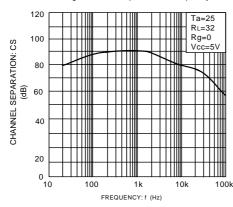
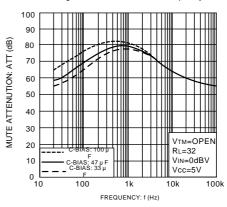
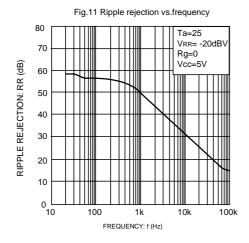


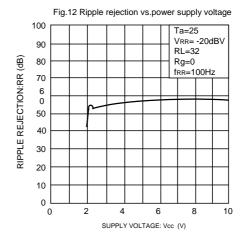
Fig.10 MUTE attenuation vs.frequency



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