

8-BIT ADDRESSABLE LATCH

FEATURES

- Serial data input
- Active parallel output
- Storage register capability
- Master clear
- Can function as demultiplexer

APPLICATIONS

- Multi-line decoders
- A/D converters

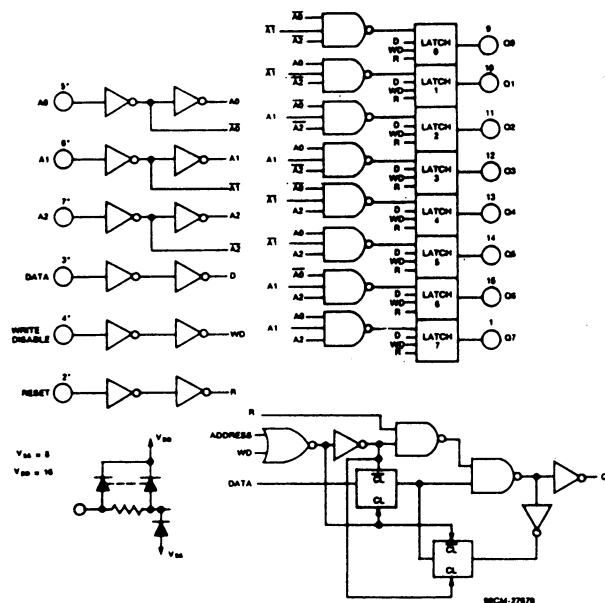
DESCRIPTION

The 4099B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

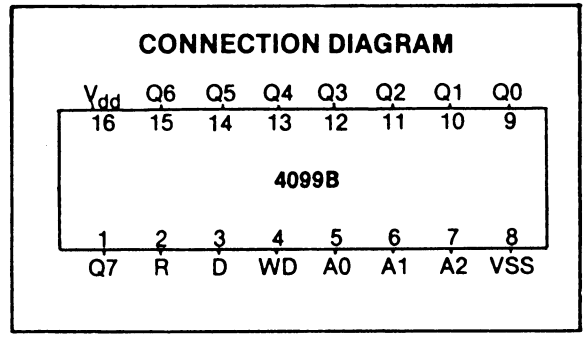
Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

LOGIC DIAGRAM



*ALL INPUTS ARE PROTECTED BY COSMIC PROTECTION NETWORK



TRUTH TABLE

WD	R	Addressed Latch	Unaddressed Latch
0	0	D	Holds previous data
0	1	D	0
1	0	Holds previous data	
1	1	0	0

TIMING DIAGRAMS

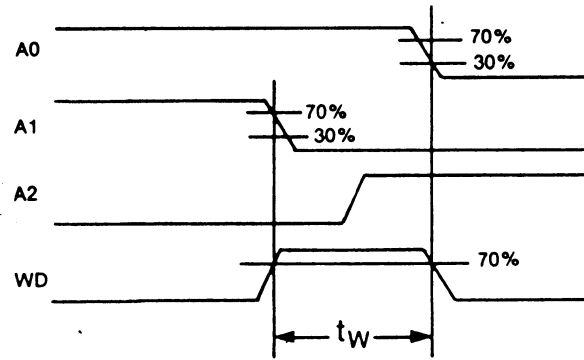


Fig. 1 — Definition of WRITE DISABLE ON time.

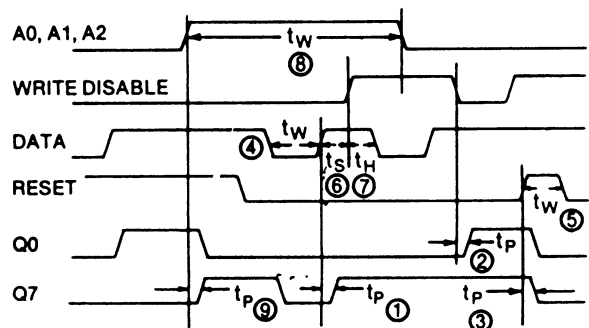


Fig. 2 — Master timing diagram.

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 2}

PARAMETER	V _{DD}	I _{LOW2}		+ 25°C			T _{HIGH}		Units
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE I _{DD} CURRENT	5	—	5	—	0.02	5	—	150	μA
	10	—	10	—	0.02	10	—	300	
	15	—	20	—	0.02	20	—	600	

DYNAMIC CHARACTERISTICS

T_A = 25° C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 K

CHARACTERISTIC	SEE FIG 2*	V _{DD} (V)	LIMITS		UNITS
			ALL PACKAGE TYP.	TYPES MAX.	
Propagation Delay: t _{PLH} , t _{PHL}	①	5	200	400	
Data to Output		10	75	150	
WRITE DISABLE to Output.		15	50	100	
t _{PLH} , t _{PHL}	②	5	200	400	ns
Reset to Output,		10	80	160	
t _{PHL}		15	60	120	
Reset to Output,	③	5	175	350	
t _{PHL}		10	80	160	
Address to Output,		15	65	130	
t _{PLH} , t _{PHL}	⑨	5	225	450	
Transition Time, T _{THL} , (Any Output) t _{TLH}		10	100	200	
		15	50	100	
Minimum Pulse Width, t _w Data	④	5	100	200	ns
Address		10	50	100	
Reset		15	40	80	
Minimum Setup Time, t _s Data to WRITE DISABLE	⑥	5	200	400	ns
Minimum Hold Time, t _H Data to WRITE DISABLE		10	100	200	
Average Input Capacitance C ₁		15	65	125	
Minimum Setup Time, t _s Data to WRITE DISABLE	⑤	5	75	150	ns
Minimum Hold Time, t _H Data to WRITE DISABLE		10	40	75	
Average Input Capacitance C ₁		15	25	50	
Minimum Setup Time, t _s Data to WRITE DISABLE	⑦	5	50	100	ns
Minimum Hold Time, t _H Data to WRITE DISABLE		10	25	50	
Average Input Capacitance C ₁		15	20	35	
Minimum Setup Time, t _s Data to WRITE DISABLE	⑧	5	75	150	ns
Minimum Hold Time, t _H Data to WRITE DISABLE		10	40	75	
Average Input Capacitance C ₁		15	25	50	
Average Input Capacitance C ₁	Any Input		5	—	pF

*Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A0, A1, and A2 are settling to a stable level, to prevent a wrong cell from being addressed (see Fig. 1).