CMOS 12-BIT PARITY TREE

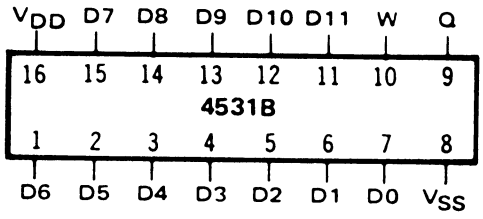
FEATURES

- Variable Word Length
- Buffered Output
- Parity Selection Input

DESCRIPTION

The 4531B 12-Bit Parity Tree is constructed with MOS P-channel and N-channel enhancement-mode devices in a single monolithic structure. The circuit consists of 12 Data-bit inputs (D0 thru D11), an even or odd Parity Selection input (W), and an output (Q). The Parity Selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even number of 1's. Words of greater than 12 bits can be accommodated by cascading other 4531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple-input summer without carries.

CONNECTION DIAGRAM
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

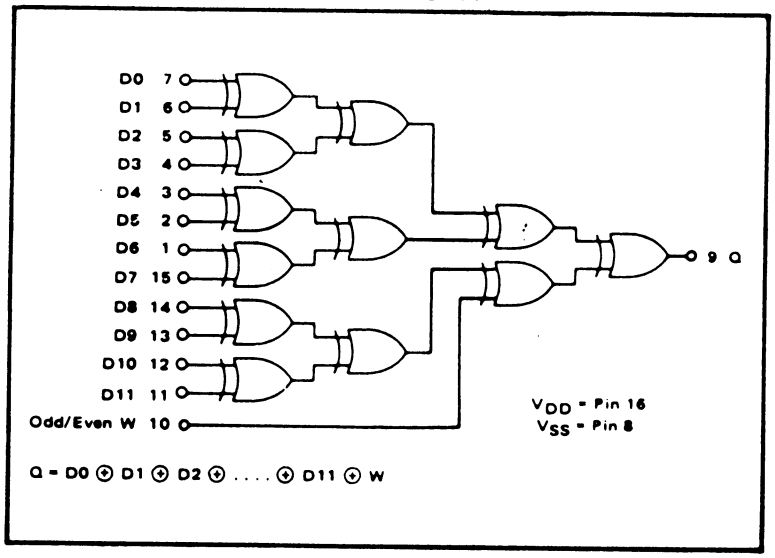
TRUTH TABLE

INPUTS								OUTPUT
W	D11	D10	···	D2	D1	D0	DECIMAL (OCTAL) EQUIVALENT	Q*
0	0	0	···	0	0	0	0 (0)	0
0	0	0	···	0	0	1	1 (1)	1
0	0	0	···	0	1	0	2 (2)	1
0	0	0	···	0	1	1	3 (3)	0
0	0	0	···	1	0	0	4 (4)	1
0	0	0	···	1	0	1	5 (5)	0
0	0	0	···	1	1	0	6 (6)	0
0	0	0	···	1	1	1	7 (7)	1
:	:	:	···	:	:	:	:	:
1	1	1	···	0	0	0	8184 (17770)	0
1	1	1	···	0	0	1	8185 (17771)	1
1	1	1	···	0	1	0	8186 (17772)	1
1	1	1	···	0	1	1	8187 (17773)	0
1	1	1	···	1	0	0	8188 (17774)	1
1	1	1	···	1	0	1	8189 (17775)	0
1	1	1	···	1	1	0	8190 (17776)	0
1	1	1	···	1	1	1	8191 (17777)	1

*0 = Even Parity
1 = Odd Parity

Note: May redefine to suit application by manipulating W and/or other available D's

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

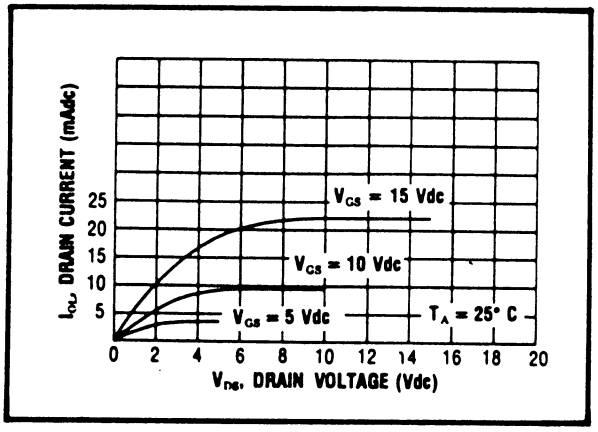
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From D Inputs	t_{PLH}, t_{PHL}	5	–	420	840	ns
		10	–	175	350	
		15	–	120	240	
From W Input	t_{PLH}, t_{PHL}	5	–	250	500	ns
		10	–	100	200	
		15	–	70	140	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	130	260	ns
		10	–	65	130	
		15	–	50	100	



Typical N-Channel
Sink Current Characteristics