CMOS 8-BIT PRIORITY ENCODER

FEATURES

- **Converts from 1 of 8 binary**
- **Provides cascading features to handle any number of inputs**
- **group select indicates one or more priority inputs**
- **Standardized, symmetrical output characteristics**
- **Noise margin (full package-temperature range):**
  - **1V at V_{DD} = 5V**
  - **2V at V_{DD} = 10V**
  - **2.5V at V_{DD} = 15V**
- **5V, 10V, and 15V parametric ratings**

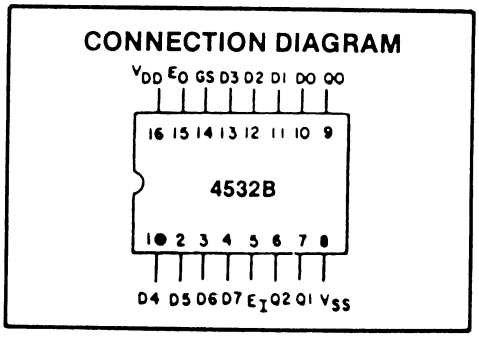
APPLICATIONS

- **Priority encoder**
- **Binary or BCD encoder (keyboard encoding)**
- **Floating point arithmetic**

DESCRIPTION

The 4532B consists of combinational logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority; D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input E_1 is low. Then E_1 is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out (E_0) is high when no priority inputs are present. If any one input is high, E_0 is low and all cascaded lower-order stages are disabled.

CONNECTION DIAGRAM

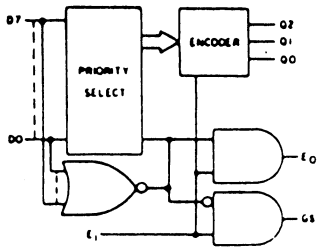


RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply Voltage Range (for T_A= Full Package Temp. Range)	3	15	V

FUNCTIONAL DIAGRAM



TRUTH TABLE

Input									Output				
E_I	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_O
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1 ≡ High Logic 0 ≡ Low

ELECTRICAL CHARACTERISTICS

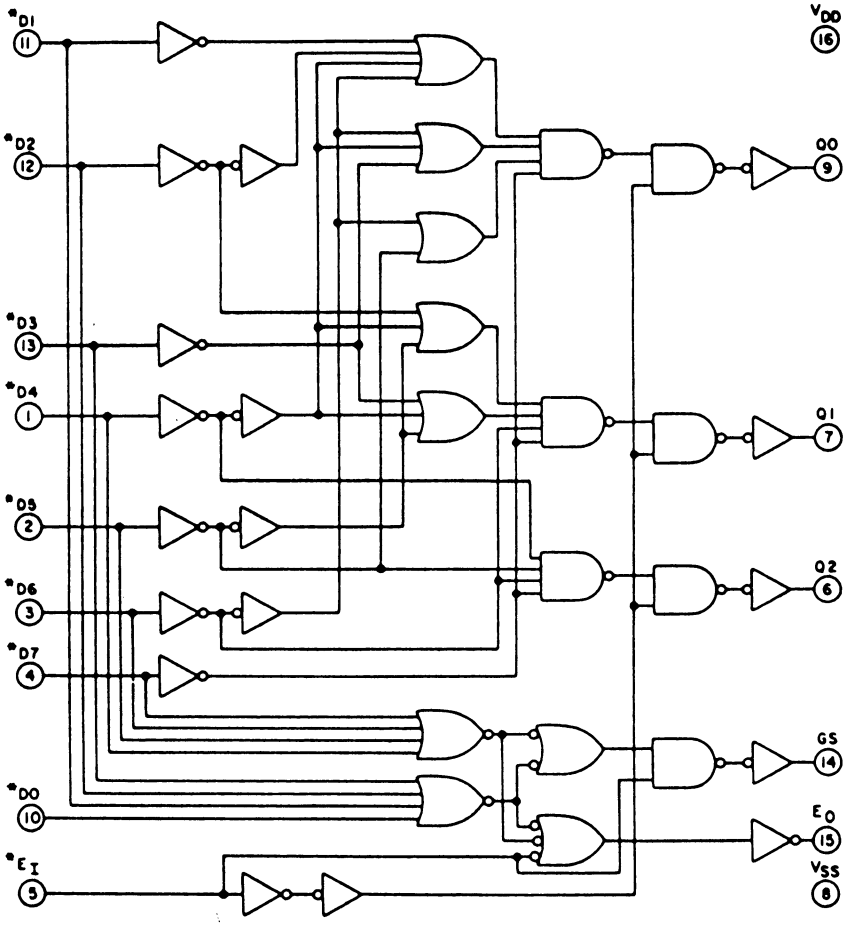
STATIC CHARACTERISTICS[1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	—	5	—	0.05	5	—	150	μAdc
		10	All Valid input	—	10	—	0.1	10	—	300	
		15	combinations	—	20	—	0.2	20	—	600	

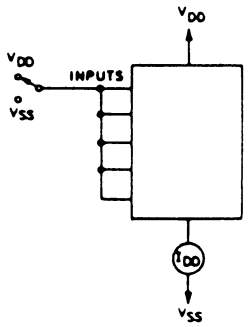
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications"
[2] T_{LOW} = −55°C for C
= −40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; C_L = 50 pF.

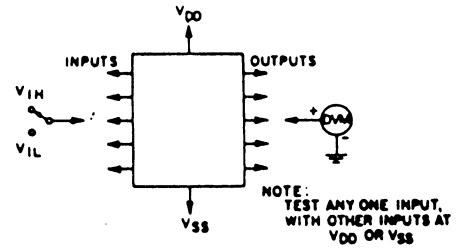
CHARACTERISTIC	TEST CONDITONS V_{DD} VOLTS	LIMITS ALL TYPES		UNITS
		TYP.	MAX.	
PROPAGATION DELAY TIME t_{PHL}, t_{PLH} E_I to E_O, E_I to GS	5	110	220	ns
	10	55	110	
	15	45	85	
E_I to Qm, Dn to Gs	5	170	340	
	10	85	170	
	15	65	125	
Dn to QM	5	220	440	
	10	110	220	
	15	85	160	
TRANSITION TIME t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
INPUT CAPACITANCE C_{IN}	Any Input	5	75	pF



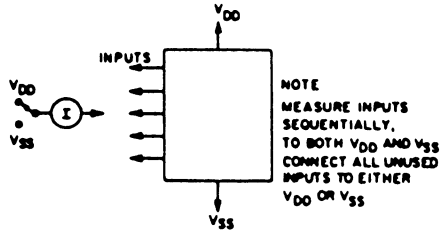
4532 logic diagram.



Quiescent device current test circuit.



Input voltage test circuit.



Input current test circuit.

AC TEST WAVEFORMS

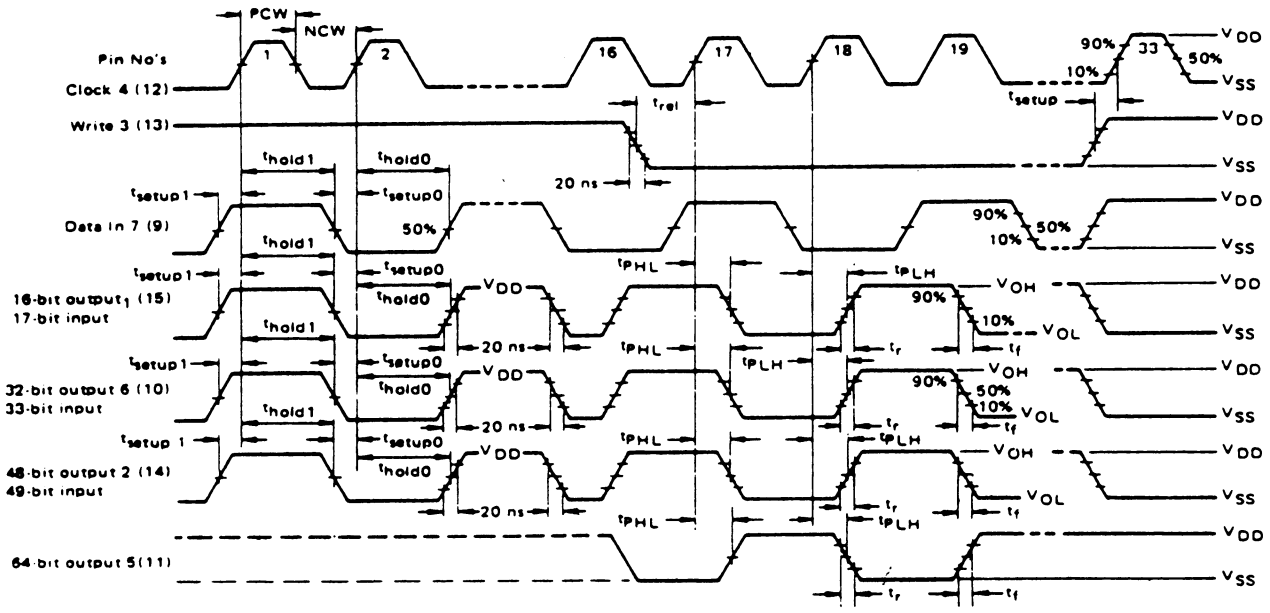
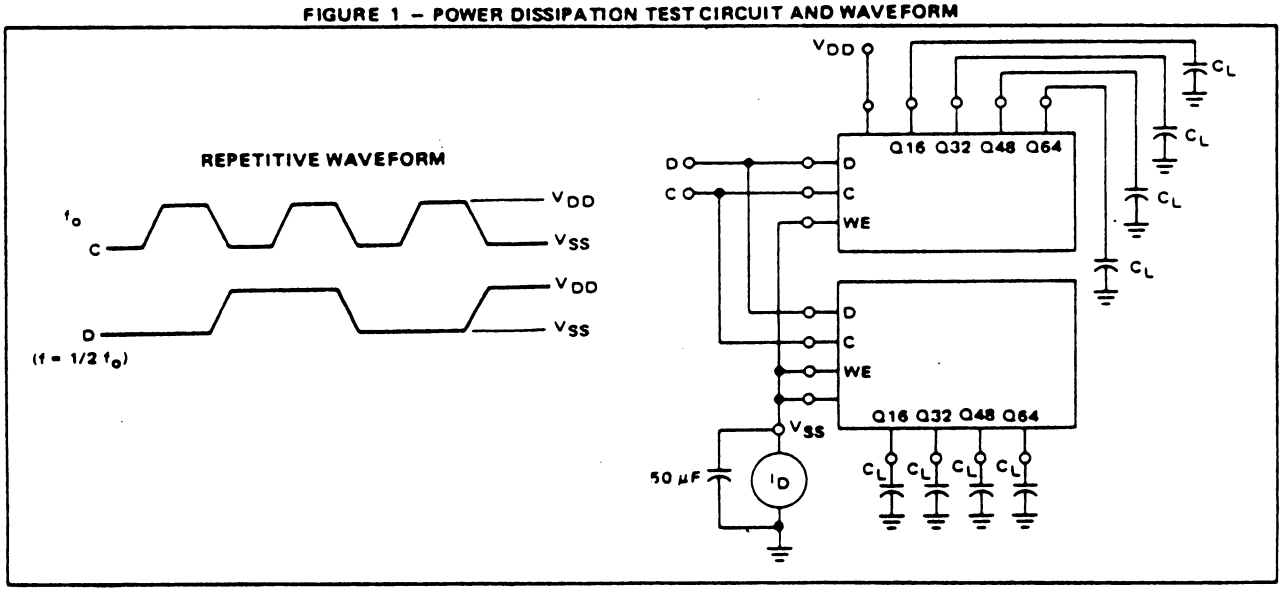


FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



EXPANDED BLOCK DIAGRAM
(1/2 OF DEVICE SHOWN)