

FEATURES:

- Monolithic CMOS A/D converters
 - Inherent sampling architecture
 - 2-channel input multiplexer
 - Flexible serial output port
- Conversion time
 - 5102A: 40 μ s
- Linearity error: $\pm 0.001\%$ FS
 - Guaranteed no missing codes
- Self-calibration maintains accuracy
 - Over time and temperature
- Fully latchup protected

DESCRIPTION:

Maxwell Technologies' 5102ALPRP is a 16-bit monolithic CMOS analog-to-digital converter capable of 20 kHz throughput. On-chip self-calibration achieves nonlinearity of $\pm 0.001\%$ of FS and guarantees 16-bit no missing codes over the entire specified temperature range. Offset and full-scale errors are minimized during the calibration cycle, eliminating the need for external trimming.

The 5102ALP each consist of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, clock generator, comparator, and serial communications port. The inherent sampling architecture of the device eliminates the need for an external track and hold amplifier.

Maxwell Technologies' patented RAD-PAK[®] packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while improving the TID performance in most space environments. This product is available with screening up to Maxwell Technologies self-defined Class K.

TABLE 1. 5102ALP ABSOLUTE MAXIMUM RATINGS
(AGND, DGND = 0V, ALL VOLTAGES WITH RESPECT TO GROUND)

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC Power Supplies: ¹				V
Positive Digital	VD+	-0.3	6.0	
Negative Digital	VD-	0.3	-6.0	
Positive Analog	VA+	-0.3	6.0	
Negative Analog	VA-	0.3	-6.0	
Input Current, Any Pin Except Supplies ²	I _{IN}	--	±10	mA
Analog Input Voltage (AIN and V _{REF} pins)	V _{INA}	(VA-) -0.3	(VA+) 0.3	V
Digital Input Voltage	V _{IND}	-0.3	(VA+) 0.3	V
Ambient Operating Temperature	T _A	-15	55	°C
Storage Temperature	T _{STG}	-65	150	°C

1. In addition, VD+ must not be greater than (VA+) 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latchup.

TABLE 2. 5102ALP RECOMMENDED OPERATING CONDITIONS
(AGND, DGND = 0V, ALL VOLTAGES WITH RESPECT TO GROUND)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DC Power Supplies:					V
Positive Digital	VD+	4.5	5.0	VA+	
Negative Digital	VD-	-4.5	-5.0	-5.5	
Positive Analog	VA+	4.5	5.0	5.5	
Negative Analog	VA-	-4.5	-5.0	-5.5	
Analog Reference Voltage	VREF	2.5	4.5	(VA+) -0.5	V
Analog Input Voltage ¹	V _{AIN}				V
Unipolar		AGND	--	V _{REF}	
Bipolar		-V _{REF}	--	V _{REF}	

1. The 5102ALPRP can accept input voltage up to the analog supplies (VA+ and VA-). They will produce an output of all 1s for inputs above V_{REF} and all 0s for inputs below AGND in unipolar mode and -V_{REF} in bipolar mode, with binary coding (CODE = low).

TABLE 3. ANALOG CHARACTERISTICS

($T_A = T_{MIN}$ TO T_{MAX} ; V_{A+} , $V_{D+} = 5V$; V_{A-} , $V_{D-} = -5V$; $V_{REF} = 4.5V$; FULL-SCALE INPUT SINEWAVE, 200 Hz; $CLKIN = 1.6$ MHz; $f_S = 20$ kHz; BIPOLAR MODE;

FRN MODE; A_{IN1} AND A_{IN2} TIED TOGETHER, EACH CHANNEL TESTED SEPARATELY; ANALOG SOURCE IMPEDANCE = 50 Ω WITH 1000 pF TO AGND UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Accuracy					
Resolution ¹	RES	16	--	--	Bits
Full Scale Error ²	FSE	--	± 1	± 5	LSB
Drift ³		--	± 2	--	DLSB
Unipolar Offset ²	VOFF	--	± 1	± 5	LSB
Drift ³		--	± 2	--	DLSB
Bipolar Offset ²	BOFF	--	± 2	± 5	LSB
Drift ³		--	± 2	--	DLSB
Bipolar Negative Full Scale Error ²	BNFSE	--	± 2	± 5	LSB
Drift ²		--	± 2	--	DLSB
Integral Nonlinearity	INL	--	--	± 3	LSB
Differential Nonlinearity	DNL	--	± 1	--	LSB
Dynamic Performance (Bipolar Mode)					
Peak Harmonic or Spurious Noise ^{2, 4}		94	100	--	dB
Total Harmonic Distortion ⁴		--	0.002	--	%
Signal-to-Noise Ratio ^{2, 4}					dB
0 dB Input		87	90	--	
-60 dB Input		--	30	--	
Noise ⁵					μ Vrms
Unipolar Mode		--	35	--	
Bipolar Mode		--	70	--	
Analog Input					
Aperture Time		--	30	--	ns
Aperture Jitter		--	100	--	ps
Input Capacitance ^{6, 4}					pF
Unipolar Mode		--	335	--	
Bipolar Mode		--	215	--	
Conversion and Throughput					
Conversion Time ⁷	t_c	--	40.625	--	μ s
Acquisition Time ⁸	t_a	--	9.375	--	μ s
Throughput ^{9, 10}	f_{TP}	--	20	--	kHz
Power Supplies					

TABLE 3. ANALOG CHARACTERISTICS

($T_A = T_{MIN}$ TO T_{MAX} ; V_{A+} , $V_{D+} = 5V$; V_{A-} , $V_{D-} = -5V$; $V_{REF} = 4.5V$; FULL-SCALE INPUT SINEWAVE, 200 Hz; $CLKIN = 1.6$ MHz; $f_S = 20$ kHz; BIPOLAR MODE; FRN MODE; A_{IN1} AND A_{IN2} TIED TOGETHER, EACH CHANNEL TESTED SEPARATELY; ANALOG SOURCE IMPEDANCE = 50 Ω WITH 1000 pF TO AGND UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Current ¹¹					mA
Positive Analog	I_{A+}	--	8.5	12	
Negative Analog	I_{A-}	--	-7.7	-11	
(SLEEP High) Positive Digital	I_{D+}	--	0.5	1.5	
Negative Digital	I_{D-}	--	-0.5	-1.5	
Power Consumption ^{11, 12}					mW
(SLEEP High)	P_{do}	--	85	130	
(SLEEP Low)	P_{ds}	--	45	--	
Power Supply Rejection ¹³					dB
Positive Supplies	PSR	--	84	--	
Negative Supplies	PSR	--	84	--	

1. Minimum resolution for which no missing codes are guaranteed over the specified temperature range.
2. Applies after calibration at any temperature within the specified temperature range.
3. Total drift over specified temperature range after calibration at power-up at 25°C.
4. Guaranteed by characterization (5102A die).
5. Wideband noise aliased into the baseband. Referred to the input.
6. Applied only in the track mode. When converting or calibrating, input capacitance will not exceed 30 pF.
7. Conversion time scales directly to the master clock speed. The times shown are for synchronous, internal loopback (FRN mode). In PDT, RBT, and SSC modes, asynchronous delay between the falling edge of HOLD and the start of conversion may add to the apparent conversion time. This delay will not exceed 1 master clock cycle + 140 ns.
8. The 5102ALPRP requires 6 clock cycles of coarse charge, followed by a minimum of 5.625 μ s of fine charge. FRN mode allows 9 clock cycles for fine charge which provides for the minimum 5.625 μ s with a 1.6 MHz clock; however, in PDT, RBT, or SSC modes, at clock frequencies less than 1.6 MHz, fine charge may be less than 9 clock cycles.
9. Throughput is the sum of the acquisition and conversion times. It will vary in accordance with conditions affecting acquisition and conversion times described above.
10. Typical value (measured).
11. All outputs unloaded. All inputs at V_{D+} or DGND.
12. Power consumption in the sleep mode applies with no master clock applied ($CLKIN$ held high or low).
13. With 300 mV p-p, 1 kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB.

TABLE 4. 5102ALP SWITCHING CHARACTERISTICS

($T_A = T_{MIN}$ TO T_{MAX} ; V_{A+} , $V_{D+} = 5V \pm 10\%$; V_{A-} , $V_{D-} = -5V \pm 10\%$; INPUTS: LOGIC 0 = 0V, LOGIC 1 = V_{D+} ; $C_L = 50$ pF)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CLKIN Period ^{1, 2}	t_{clk}	0.5	--	10	μ s
CLKIN Low Time	t_{ckl}	200	--	--	ns
CLKIN High Time	t_{clkh}	200	--	--	ns

TABLE 4. 5102ALP SWITCHING CHARACTERISTICS

(T_A = T_{MIN} TO T_{MAX}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; INPUTS: LOGIC 0 = 0V, LOGIC 1 = VD+; C_L = 50 pF)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Crystal Frequency ^{1,2}	f _{xtal}	--	1.6	--	MHz
SLEEP Rising to Oscillator Stable ³		--	20	--	ms
RST Pulse Width ⁴	t _{rst}	150	--	--	ns
RST to STBY Falling	t _{drst}	--	100	--	ns
RST Rising to STBY Rising	t _{cal}	--	2,882,040	--	t _{clk}
CH1/2 Edge to TRK1, TRK2 Rising ⁵	t _{drsh1}	--	80	--	ns
CH1/2 Edge to TRK1, TRK2 Falling ⁵	t _{dfsh4}	--	--	68t _{clk} + 260	ns
HOLD to SSH Falling ⁶	t _{dfsh2}	--	60	--	ns
HOLD to TRK1, TRK2, Falling ⁶	t _{dfsh1}	66t _{clk}	--	68t _{clk} + 260	ns
HOLD to TRK1, TRK2, SSH Rising ⁶	t _{drsh}	--	120	--	ns
HOLD Pulse Width ⁷	t _{hold}	1t _{clk} + 20	--	63t _{clk}	ns
HOLD to CH1/2 Edge ⁶	t _{dhlri}	300	--	64t _{clk}	ns
HOLD Falling to CLKIN Falling ⁷	t _{hcf}	275	--	1t _{clk} + 10	ns
PDT and RBT Modes					
SCLK Input Pulse Period	t _{sclk}	1000	--	--	ns
SCLK Input Pulse Width Low	t _{sckll}	500	--	--	ns
SCLK Input Pulse Width High	t _{scklh}	500	--	--	ns
SCLK Input Falling to SDATA Valid	t _{dss}	--	100	150	ns
HOLD Falling to SDATA Valid - PDT Mode	t _{dhs}	--	140	230	ns
TRK1, TRK2 Falling to SDATA Valid ⁸	t _{dtst}	--	65	125	ns
FRN and SSC Modes					
SCLK Output Pulse Width Low	t _{slkl}	--	2t _{clk}	--	t _{clk}
SCLK Output Pulse Width High	t _{slkh}	--	2t _{clk}	--	t _{clk}
SDATA Valid Before Rising SCLK	t _{ss}	2t _{clk} - 100	--	--	ns
SDATA Valid After Rising SCLK	t _{sh}	2t _{clk} - 100	--	--	ns
SDL Falling to 1st Rising SCLK	t _{rscld}	--	2t _{clk}	--	ns
Last Rising SCLK to SDL Rising	t _{rsdl}	--	2t _{clk}	2t _{clk} + 200	ns
HOLD Falling to 1st Falling SCLK	t _{hfs}	6t _{clk}	--	8t _{clk} + 200	ns
CH1/2 Edge to 1st Falling SCLK	t _{chfs}	--	7t _{clk}	--	t _{clk}

1. Minimum CLKIN period is 0.625 μs in FRN mode (20 kHz sample rate).
2. External loading capacitors are required to allow the crystal to oscillate. Maximum crystal frequency is 1.6 MHz in FRN mode (20 kHz sample rate).
3. With a 2.0 MHz crystal, two 33 pF loading capacitors and a 10 MW parallel resistor.
4. Guaranteed by initial characterization (5102A die).
5. These times are for FRN mode.
6. These times are for PDT and RBT modes.

- When $\overline{\text{HOLD}}$ goes low, the analog sample is captured immediately. To start conversion, $\overline{\text{HOLD}}$ must be latched by a falling edge of CLKIN. Conversion will begin on the next rising edge of CLKIN after $\overline{\text{HOLD}}$ is latched.
- Only valid for $\overline{\text{TRK1}}$, $\overline{\text{TRK2}}$ falling when SCLK is low. If SCLK is high when $\overline{\text{TRK1}}$, $\overline{\text{TRK2}}$ falls, then SDATA is valid t_{dss} time after the next falling SCLK.

TABLE 5. 5102ALP DIGITAL CHARACTERISTICS
($T_A = T_{\text{MIN}}$ TO T_{MAX} ; V_{A+} , $V_{D+} = 5V \pm 10\%$; V_{A-} , $V_{D-} = -5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Calibration Memory Retention Power Supply Voltage V_{A+} & V_{D+} ¹	V_{MR}	2.0	--	--	V
High-Level Input Voltage	V_{IH}	2.0	--	--	V
Low-Level Input Voltage	V_{IL}	--	--	0.8	V
High-Level Output Voltage ²	V_{OH}	(V_{D+}) -1.0	--	--	V
Low-Level Output Voltage - $I_{\text{OUT}} = 1.6 \text{ mA}$	V_{OL}	--	--	0.4	V
Input Leakage Current	I_{IN}	--	--	10	μA
Digital Output Pin Capacitance	C_{OUT}	--	9	--	pF

- V_{A-} and V_{D-} can be any value from zero to -5V for memory retention. Neither V_{A-} or V_{D-} should be allowed to go positive. A_{IN1} , A_{IN2} or V_{REF} must not be greater than V_{A+} or V_{D+} . This parameter is guaranteed by characterization.
- $I_{\text{OUT}} = -100 \mu\text{A}$. This specification guarantees TTL compatibility ($V_{\text{OH}} = 2.4\text{V}$ @ $I_{\text{OUT}} = -40 \mu\text{A}$).

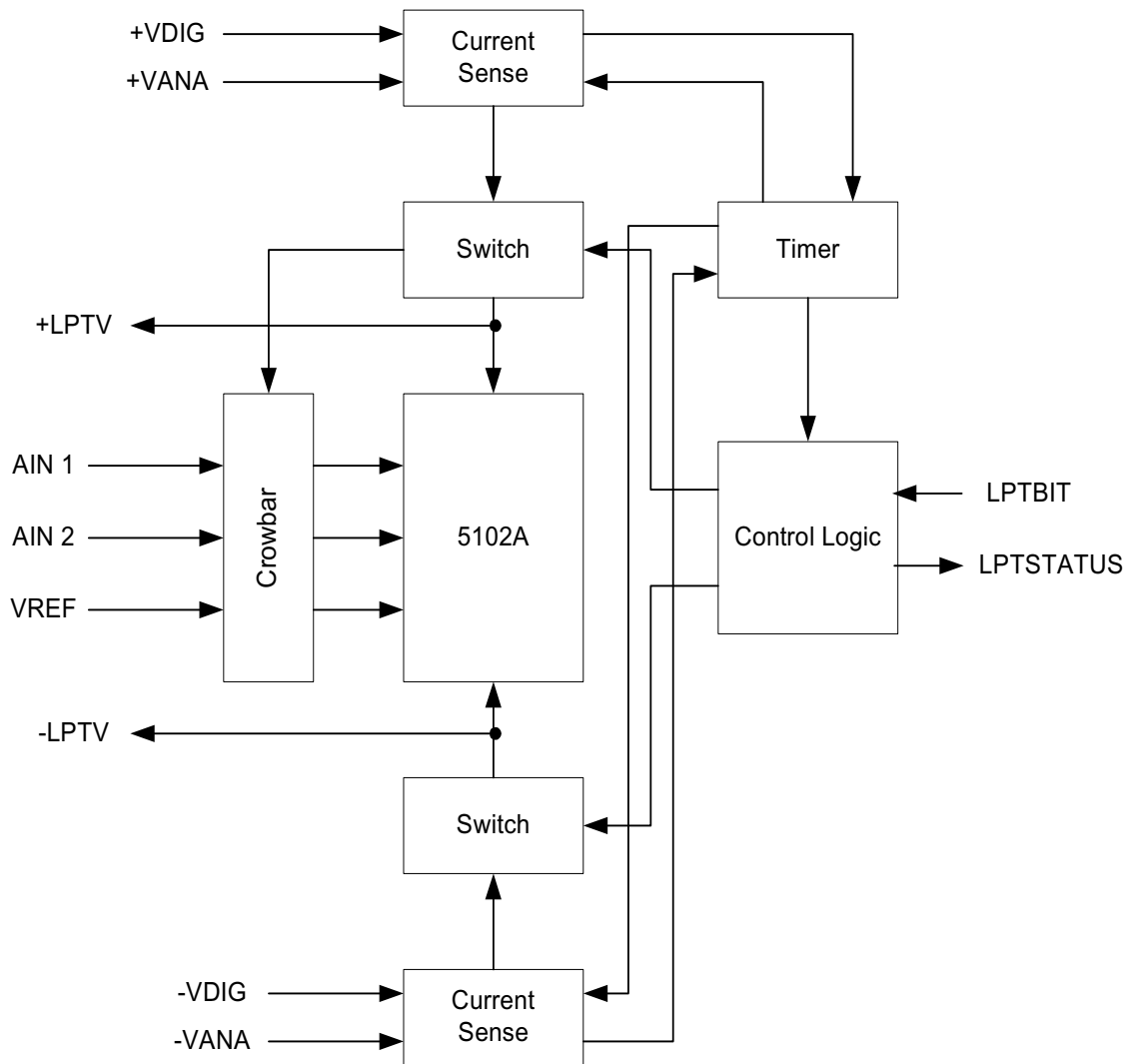
LPT™ OPERATION

Latchup Protection Technology (LPT™) automatically detects an increase in the supply current of the 5102ALP converter due to a single event effect and internally cycle the power to the converter off, then on, which restores the steady state operation of the device.

If data outputs are connected to a bus with other bus driver circuits, all external data bus drivers must be tri-stated and individual pull up resistors to the supply voltage (if used on the data bus) must no be less than 10 K ohm typical to assure proper single event effect recovery.

STATUS can also be used to generate an input to the system data processor indicating that an LPT™ cycle has occurred, and the protected device output accuracy may not be met until after the respective recovery time to the event. The STATUS signal is generated from an advanced CMOS logic gate output. This output may not exhibit a monotonic fall time and may even oscillate briefly while power is being restored to the protected device and the decoupling capacitance is charged. Loading on the STATUS output should be minimized because this signal is used internally by the 5102ALP. It is recommended that load current not exceed 2 mA and load capacitance be kept will below 1000 pF.

5102ALP LPT™ BLOCK DIAGRAM



LATCH-UP PROTECTION CIRCUIT (LPT) PIN DESCRIPTION

PIN	PIN NAME	FUNCTION
18	LPTBIT	The LPT circuit will crowbar the power supplies to the SEI5102ALPRP for as long as a logical high is applied. Used to verify operation of the LPT. Normally a logical low or ground is applied to this input.
26	-LPTV	Negative power supply. VA- and VD- are connected and can be measured on this pin. Normally -5V.
27	+LPTV	Positive power supply. VA+ and VD+ are connected and can be measured on this pin. Normally +5V.

LATCH-UP PROTECTION CIRCUIT (LPT) PIN DESCRIPTION

PIN	PIN NAME	FUNCTION
39	LPT-STATUS	A 0 to 5V square-wave will output during a latch condition. Normally low.

FIGURE 1. RESET AND CALIBRATION TIMING

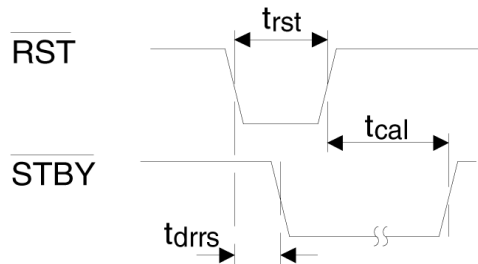


FIGURE 2. CONTROL OUTPUT TIMING

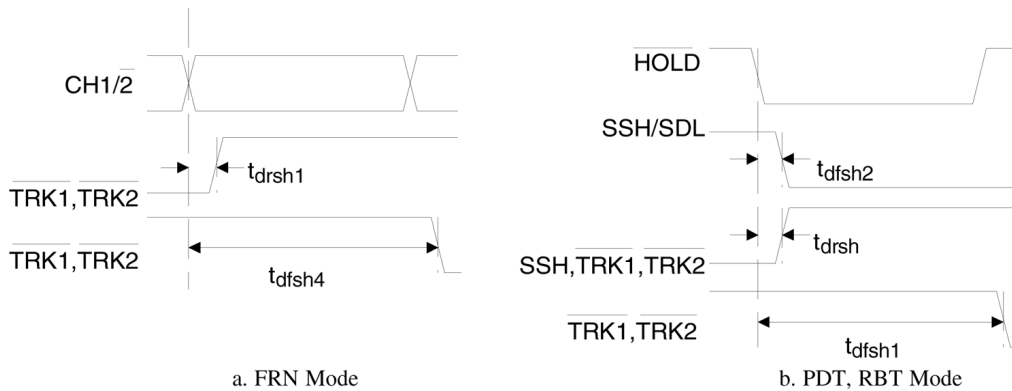


FIGURE 3. CHANNEL SELECTION TIMING

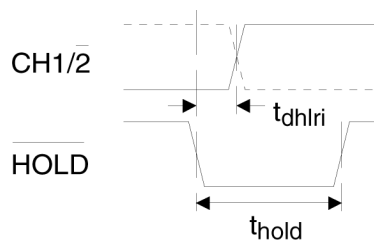


FIGURE 4. START CONVERSION TIMING

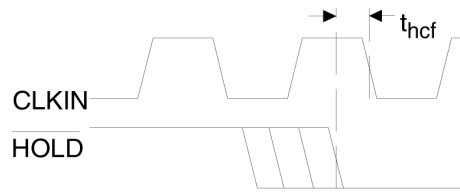


FIGURE 5. SERIAL DATA TIMING

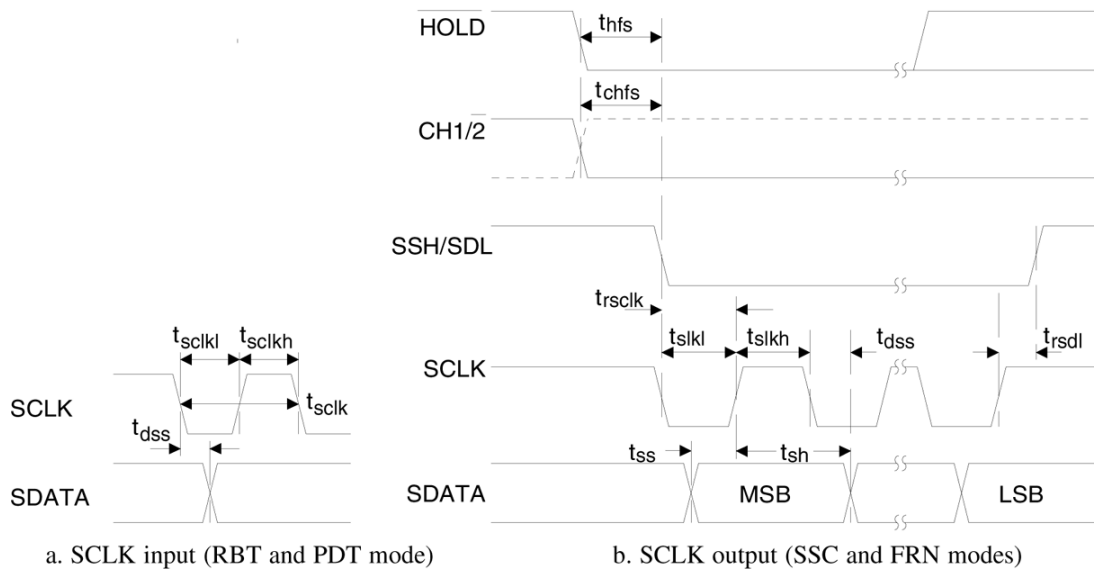


FIGURE 6. DATA TRANSMISSION TIMING

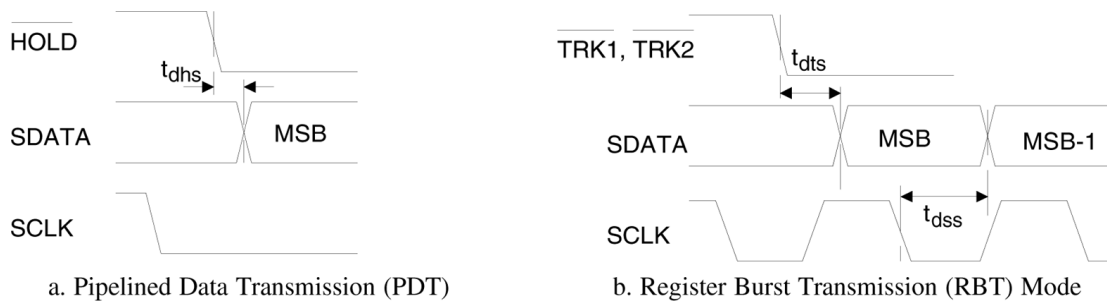
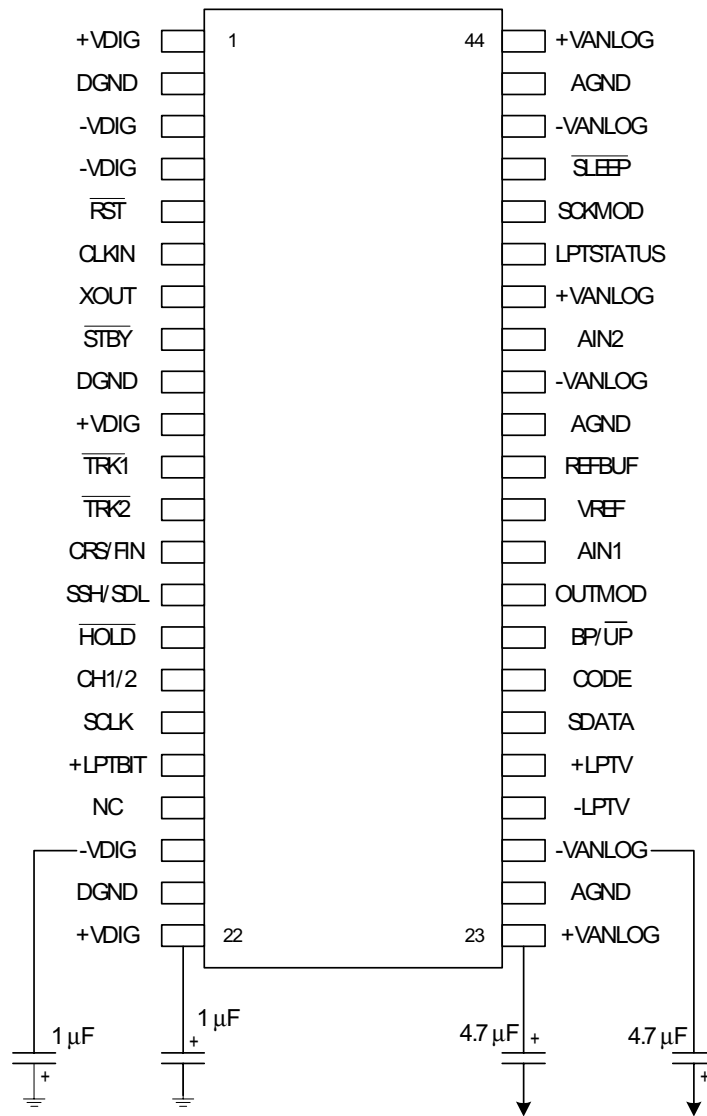


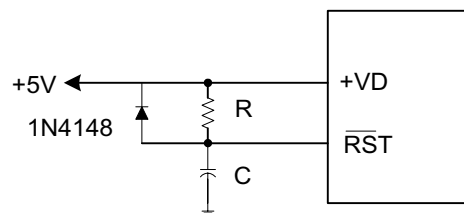
FIGURE 7. BYPASS CIRCUIT

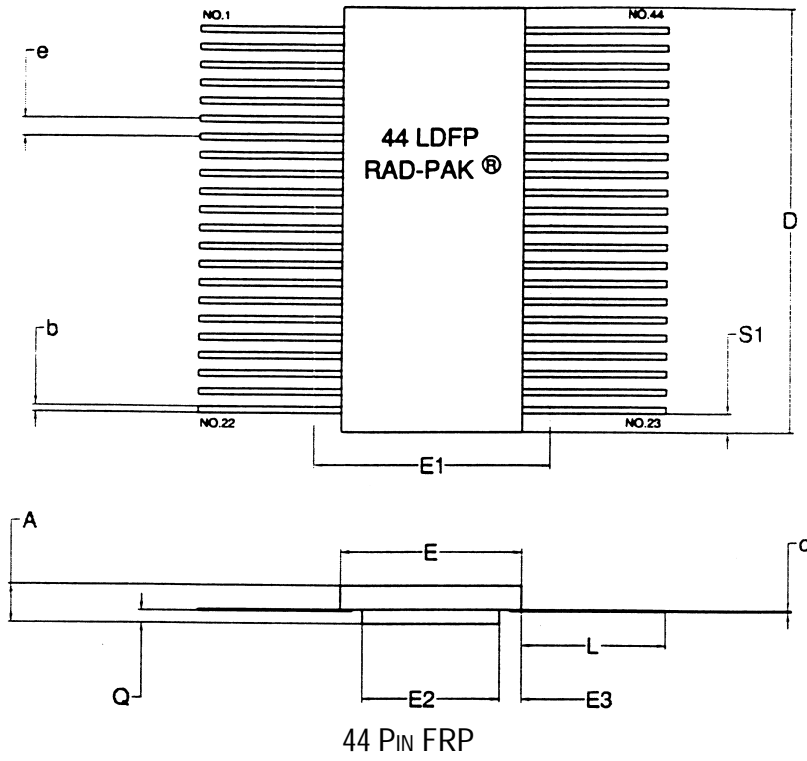


Note:

1. Cap must be connected to the device for proper operation. 4.7 μ F analog side. 1 μ F digital side.
2. Unused logic inputs should be tied to +VD or DGND.

FIGURE 8. POWER-UP RESET CIRCUIT





SYMBOL	DIMENSION		
	Min	Nom	Max
A	0.256	0.282	0.308
b	0.014	0.017	0.020
c	0.009	0.010	0.012
D	1.089	1.100	1.111
E	0.564	0.570	0.576
E1	--	--	0.600
E2	0.410	0.430	0.450
E3	0.044	0.070	--
e	0.050 BSC		
L	0.455	0.465	0.475
Q	0.022	0.027	0.032
S1	0.005	--	--
N	44		

F44

Note: All dimensions in inches

Important Notice:

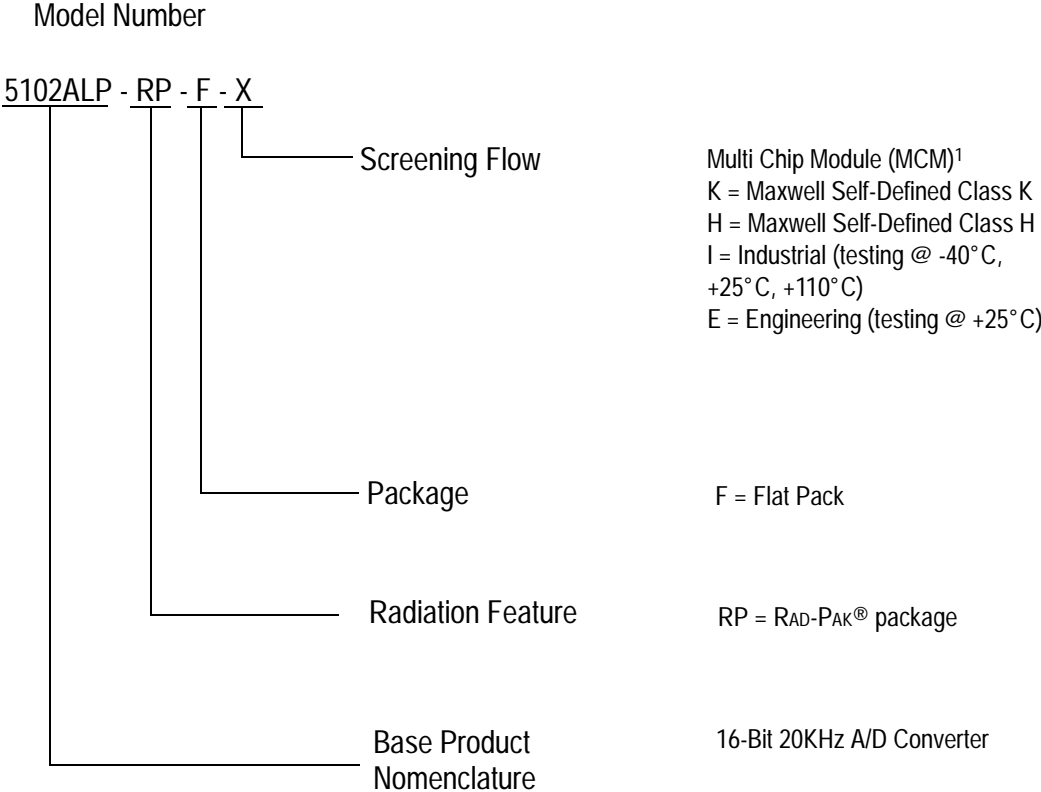
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Product Ordering Options



1) Products are manufactured and screened to Maxwell Technologies self-defined Class H and Class K flows.