

# 74F823

## 9-Bit D-Type Flip-Flop

### General Description

The 74F823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems.

### Features

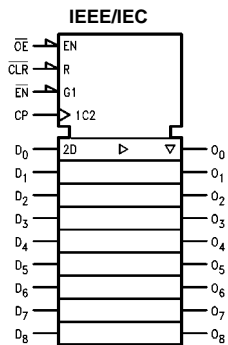
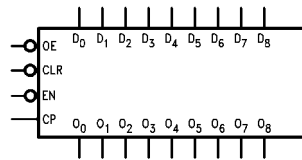
- 3-STATE outputs
- Clock Enable and Clear

### Ordering Code:

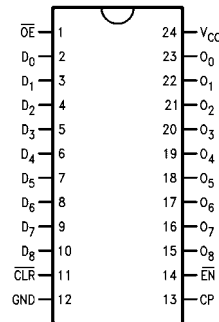
Order Number	Package Number	Package Description
74F823SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F823SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



### Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> -D <sub>8</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{OE}$	Output Enable Input	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{CLR}$	Clear	1.0/1.0	20 $\mu$ A/-0.6 mA
CP	Clock Input	1.0/2.0	20 $\mu$ A/-1.2 mA
$\overline{EN}$	Clock Enable	1.0/1.0	20 $\mu$ A/-0.6 mA
O <sub>0</sub> -O <sub>8</sub>	3-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

### Functional Description

The 74F823 device consists of nine D-type edge-triggered flip-flops. It has 3-STATE true outputs and is organized in broadside pinning. The buffered Clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the  $\overline{OE}$  LOW the contents of the flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, the 74F823 has Clear ( $\overline{CLR}$ ) and Clock Enable ( $\overline{EN}$ ) pins.

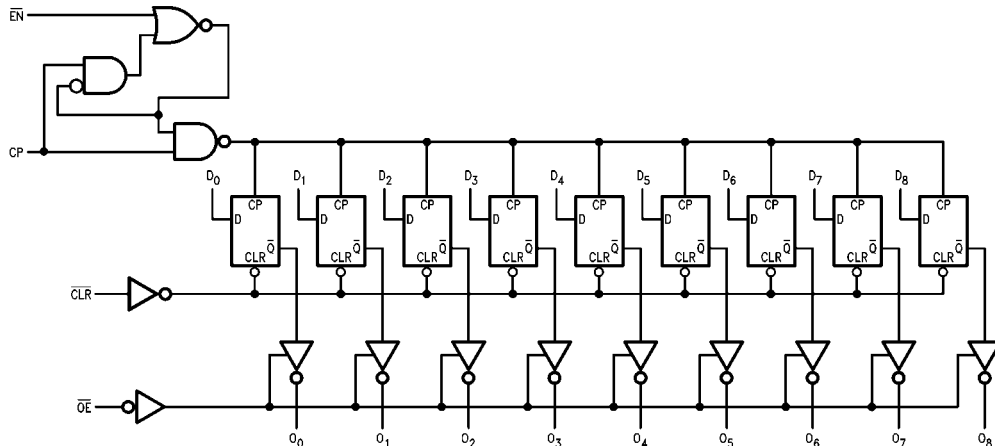
When the  $\overline{CLR}$  is LOW and the  $\overline{OE}$  is LOW, the outputs are LOW. When  $\overline{CLR}$  is HIGH, data can be entered into the flip-flops. When  $\overline{EN}$  is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the  $\overline{EN}$  is HIGH, the outputs do not change state regardless of the data or clock inputs transitions. This device is ideal for parity bus interfacing in high performance systems.

### Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	$\overline{Q}$	O	
H	H	L	H	X	NC	Z	Hold
H	H	L	L	X	NC	Z	Hold
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	Clear
H	H	L	$\nearrow$	H	H	Z	Load
H	H	L	$\nearrow$	H	L	Z	Load
L	H	L	$\nearrow$	L	H	L	Data Available
L	H	L	$\nearrow$	H	L	H	Data Available
L	H	L	H	X	NC	NC	No Change in Data
L	H	L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Immaterial  
Z = High Impedance  
 $\nearrow$  = LOW-to-HIGH Transition  
NC = No Change

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 10% V <sub>CC</sub> 5% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.2	mA mA	Max Max	V <sub>IN</sub> = 0.5V (OE, CLR, EN) V <sub>IN</sub> = 0.5V (CP)
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Buss Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		75	100	mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics

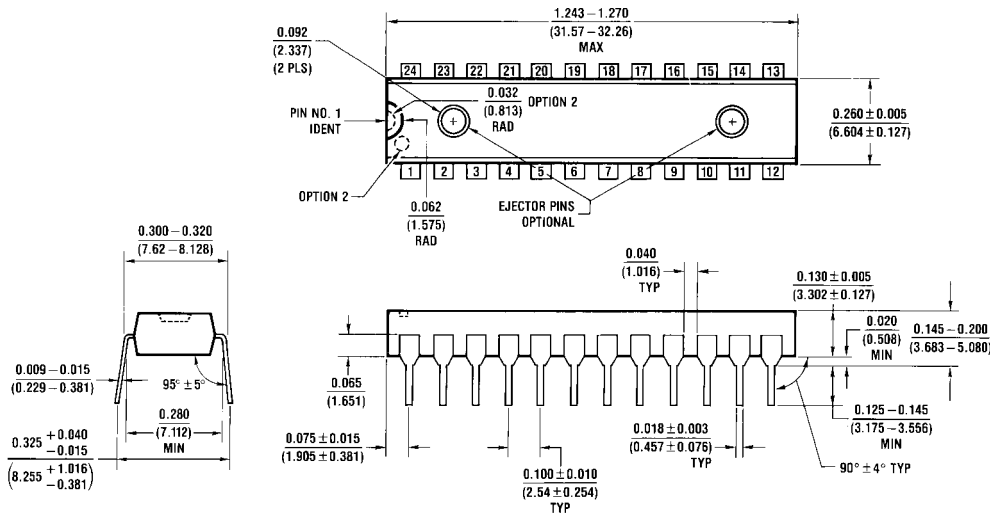
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	100	160		60		70		MHz
t <sub>PLH</sub>	Propagation Delay	2.0	5.6	9.5	2.0	10.5	2.0	10.5	ns
t <sub>PHL</sub>	CP to O <sub>n</sub>	2.0	5.2	9.5	2.0	10.5	2.0	10.5	
t <sub>PHL</sub>	Propagation Delay CLR to O <sub>n</sub>	4.0	7.1	12.0	4.0	13.0	4.0	13.0	ns
t <sub>PZH</sub>	Output Enable Time	2.0	5.8	10.5	2.0	13.0	2.0	11.5	ns
t <sub>PZL</sub>	$\overline{\text{OE}}$ to O <sub>n</sub>	2.0	5.5	10.5	2.0	13.0	2.0	11.5	
t <sub>PHZ</sub>	Output Disable Time	1.5	2.9	7.0	1.0	7.5	1.5	7.5	
t <sub>PLZ</sub>	$\overline{\text{OE}}$ to O <sub>n</sub>	1.5	2.7	7.0	1.0	7.5	1.5	7.5	

## AC Operating Requirements

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V		Units
		Min	Max	Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns
t <sub>S</sub> (L)	D <sub>n</sub> to CP	2.5		4.0		3.0		
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	2.5		2.5		2.5		ns
t <sub>H</sub> (L)	D <sub>n</sub> to CP	2.5		2.5		2.5		
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	4.5		5.0		5.0		ns
t <sub>S</sub> (L)	$\overline{\text{EN}}$ to CP	2.5		3.0		3.0		
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	2.0		3.0		2.0		
t <sub>H</sub> (L)	$\overline{\text{EN}}$ to CP	0		1.0		0		
t <sub>W</sub> (H)	CP Pulse Width	5.0		6.0		6.0		ns
t <sub>W</sub> (L)	HIGH or LOW	5.0		6.0		6.0		ns
t <sub>W</sub> (L)	CLR Pulse Width, LOW	5.0		5.0		5.0		ns
t <sub>REC</sub>	CLR Recovery Time	5.0		5.0		5.0		ns



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



N24C (REV F)

**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N24C**

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