Document Title

256K X 16 / 512K X 8 BIT CMOS MASK ROM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	July 28, 2004	Preliminary

Preliminary

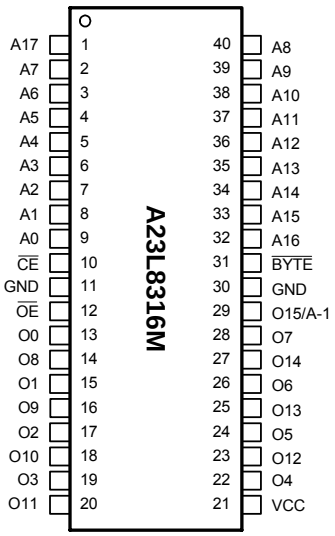
512K X 16 / 1M X 8 BIT CMOS MASK ROM

Features

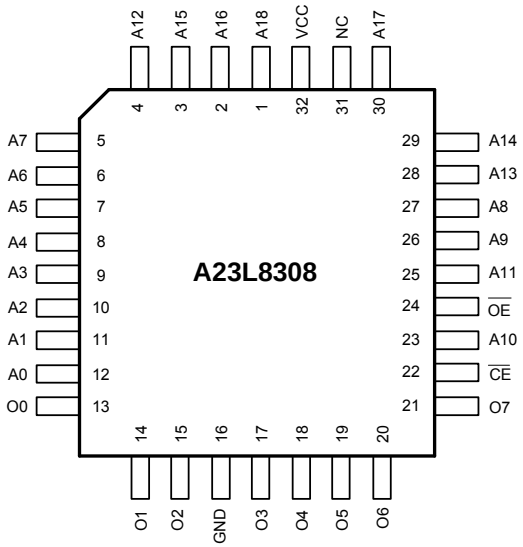
- 256K x 16 bit or 512K x 8 bit organization
- Supply voltage range: 2.7V~3.6V
- Access time: 70ns (max.)/3.0V~3.6V
  100ns (max.)/2.7V~3.6V
- Current: Operating: 20mA (typ.)/3.3V
  Standby: 10μA (typ.)/3.3V
- Three-state outputs for wired-OR expansion
- Full static operation
- All inputs and outputs are directly TTL-compatible
- Flash memory pinout compatible with AMD (A23L83161)
- Available in 40-pin SOP, 32-pin PLCC 48-pin TSOP (forward, reverse type and flash memory's pinouts compatible) packages

Pin Configurations

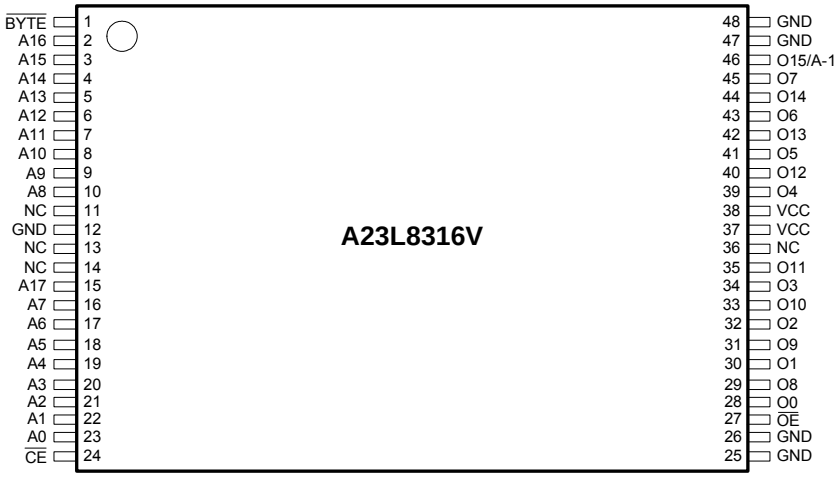
■ SOP



■ PLCC



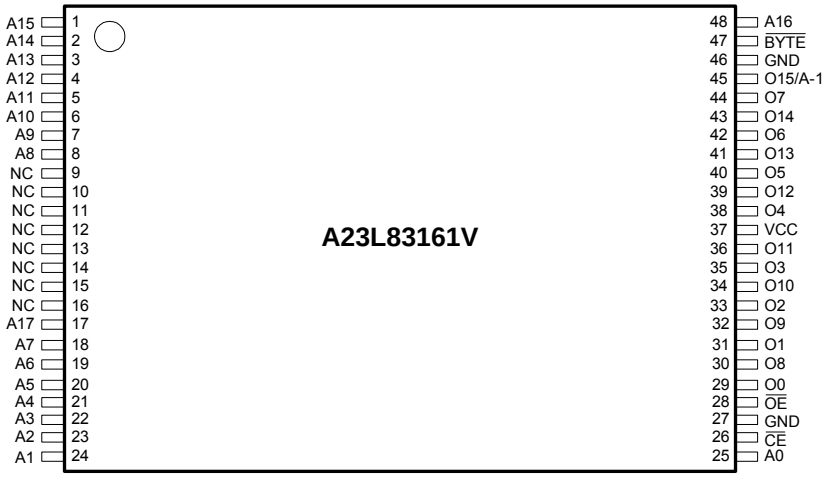
■ TSOP (forward type)



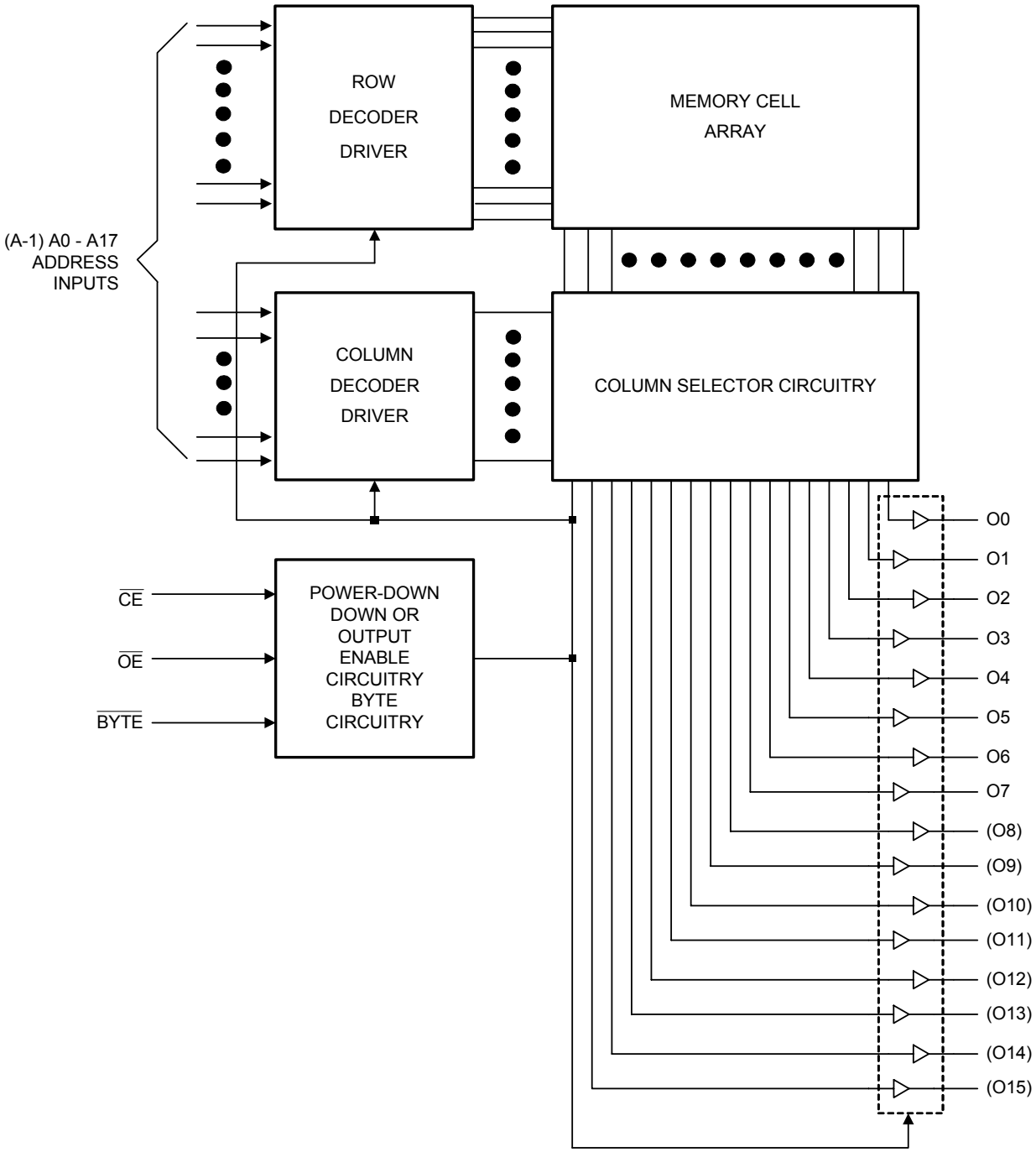
Pin Configurations (continued)

■ **TSOP (reverse type)**

■ **TSOP (forward type)**



Block Diagram



Pin Descriptions

Pin No.				Symbol	Description
32L PLCC (A23L8316)	40L SOP (A23L8316)	48L TSOP (A23L8316)	48L TSOP (A23L83161)		
1-12, 23, 25-30	1-9, 32-40	2-10, 15-23	1-8, 17-25, 48	A0-A17	Address Inputs
13-15, 17-21	13-20, 22-28	28-35, 39-45	29-36, 38-44	O0-O14	Data Outputs
-	29	46	45	O15/A-1	Output 15(WORD mode) /LSB Address (BYTE mode)
22	10	24	26	$\overline{CE}$	Chip Enable Input
24	12	27	28	$\overline{OE}$	Output Enable Input
-	31	1	47	$\overline{BYTE}$	BYTE or WORD mode Selection
32	21	37-38	37	VCC	Power Supply
16	11, 30	12, 25-26, 47-48	27, 46	GND	Ground
31	-	11, 13-14, 36	9-16	NC	No Connection

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply Voltage	2.7	3.6	V
GND	Ground	0	0	V
V_{IH}	Input High Voltage	2.2	VCC+0.3	V
V_{IL}	Input Low Voltage	- 0.3	0.6	V

Absolute Maximum Ratings*

Ambient Operating Temperature . . . . . 0°C to + 70°C
Storage Temperature . . . . . -65°C to + 125°C
Output Voltage . . . . . -0.5V to VCC + 0.5V
Input Voltage . . . . . -0.5V to VCC + 0.5V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0°C to + 70°C, VCC = 2.7V~3.6V, GND = 0V for -100, VCC = 3.0V~3.6V, GND = 0 for -70)

Symbol	Parameter	Min.	Max.	Unit	Conditions	Note
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -0.4mA (3V)	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 1.6mA (3V)	
V_{IH}	Input High Voltage	2.2	VCC + 0.3	V		
V_{IL}	Input Low Voltage	-0.3	0.6	V		
$\lvert I_{LI} \rvert$	Input Leakage Current		+10	μA	VCC = max. V_{IN} = VCC to GND	
$\lvert I_{LO} \rvert$	Output Leakage Current		+10	μA	VCC = max. V_{OUT} = VCC to GND	1
I_{CC}	Operating Supply Current		30	mA	t_{CYC} = min.	2
I_{SB}	Standby Supply Current (TTL)		1.5	mA	$\overline{CE}$ = V_{IH}	
I_{SB1}	Standby Supply Current (CMOS)		10	μA	$\overline{CE}$ ≥ VCC - 0.2V	

Capacitance

Symbol	Parameter	Min.	Max.	Unit	Test Conditions	Note
C_I	Input Capacitance		10	pF	T_A = 25°C f = 1.0MHz	3
C_O	Output Capacitance		10	pF		

AC Characteristics

(T_A = 0°C to +70°C, VCC = 2.7V~3.6V for -100, VCC = 3.0V~3.6V for -70, GND = 0V)

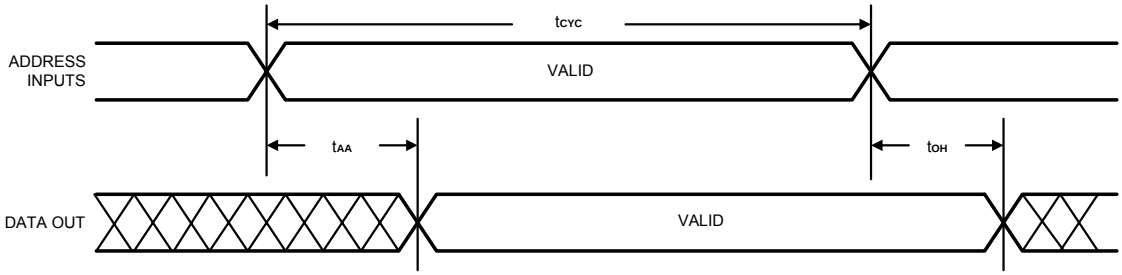
Symbol	Parameter	A23L8316/A23L83161 -70		A23L8316/A23L83161 -100		Unit	Note
		Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	70		100		ns	
t_{AA}	Address Access Time		70		100	ns	
t_{ACE}	Chip Enable Access Time		70		100	ns	
t_{AOE}	Output Enable Access Time		35		50	ns	
t_{OH}	Output Hold after Address Change	10		10		ns	
t_{LZ}	Output Low Z Delay	10		10		ns	4, 6
t_{HZ}	Output High Z Delay*		20		20	ns	5, 6

* t_{HZ} is specified from either $\overline{OE}$ or $\overline{CE}$ going disabled, whichever occurs first.

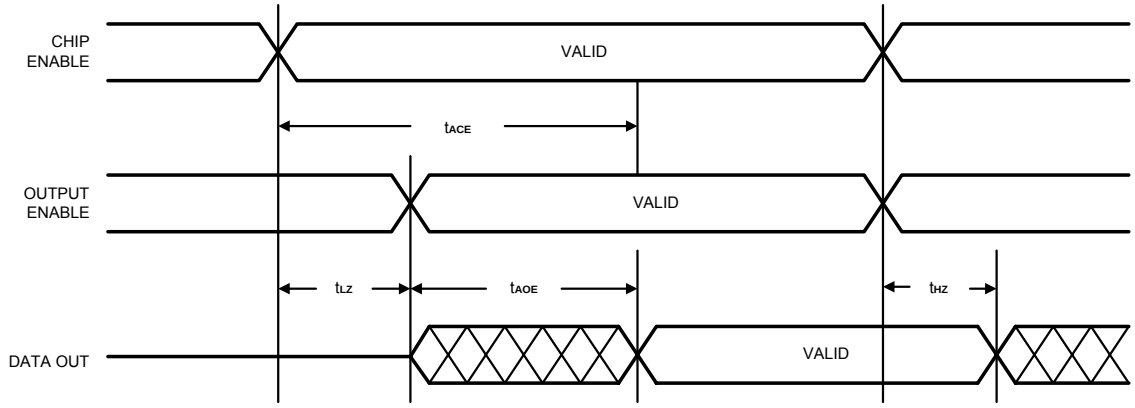
Notes:
1. $\overline{OE}$ / $\overline{CE}$ = V_{IH} (Output is unloaded)
2. V_{IN} = V_{IH}/V_{IL}, $\overline{OE}$ / $\overline{CE}$ = V_{IL} (Output is unloaded)
3. This parameter is periodically sampled and is not 100% tested. All pins, except pins under test, are tied to AC ground.
4. Output LOW impedance delay (t_{LZ}) is measured from $\overline{CE}$ or $\overline{OE}$ going active.
5. Output HIGH impedance delay (t_{HZ}) is measured from $\overline{CE}$ or $\overline{OE}$ going inactive.
6. This parameter is sampled and not 100% tested.

Timing Waveforms

Propagation Delay from Address ($\overline{CE}$ = Active, $\overline{OE}$ = Active)



Propagation Delay from Chip Enable or Output Enable (Address Valid)



AC Test Conditions

Part No.	A23L8316/A23L83161 -70	A23L8316/A23L83161 -100
Applied Voltage	3.0V~3.6V	2.7V~3.6V
Input Pulse Levels	0.4V to 2.4V	0.4V to 2.4V
Input Rise and Fall Time	10 ns	10 ns
Timing Measurement Reference Level	V_{IN} = 1.4V, V_{OUT} = 1.4V	V_{IN} = 1.4V, V_{OUT} = 1.4V
Output Load	1 TTL gate and C_L = 100pF	1 TTL gate and C_L = 100pF

Function Table

$\overline{CE}$	$\overline{OE}$/NC	$\overline{BYTE}$	O15/A-1	O0 - O7	O8 - O15	Mode
L	L	H	Data Pin O15	Data Out	Data out	Word
L	L	L	LSB Address A-1	Data Out	Hi - Z	Byte
H	X	X	X	Hi - Z	Hi - Z	Power-down
L	H	X	X	Hi - Z	Hi - Z	Output Disable

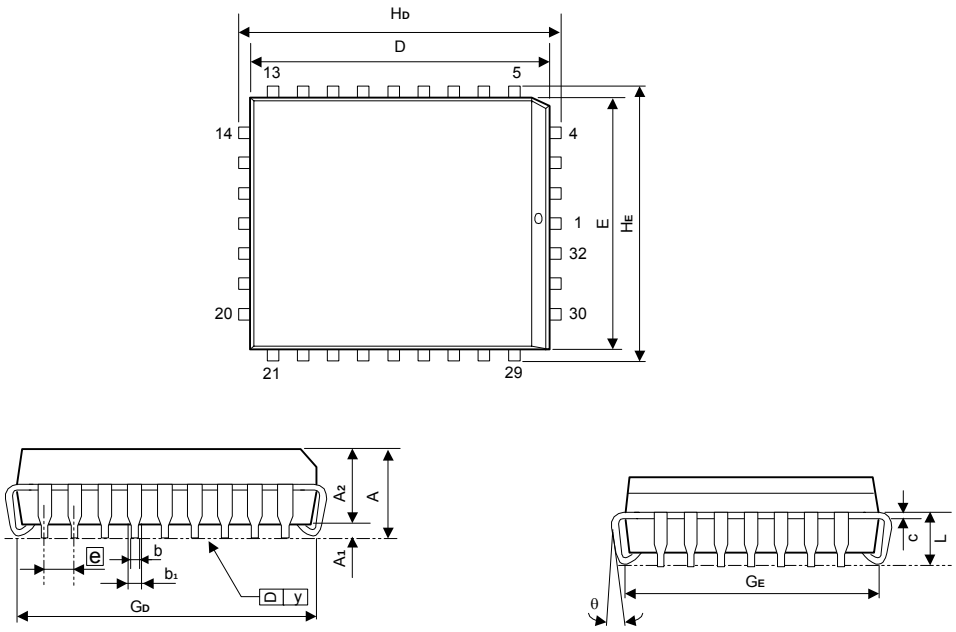
Ordering Information

Part No.	Access Time (ns)	Package
A23L8316M-70	70	40L SOP
A23L8316M-100	100	40L SOP
A23L8316V-70	70	48L TSOP (Forward)
A23L8316V-100	100	48L TSOP (Forward)
A23L8316R-70	70	48L TSOP (Reverse)
A23L8316R-100	100	48L TSOP (Reverse)
A23L83161V-70	70	48L TSOP AMD (Flash Compatible)
A23L83161V-100	100	48L TSOP AMD (Flash Compatible)

Package Information

PLCC 32L Outline Dimension

unit: inches/mm

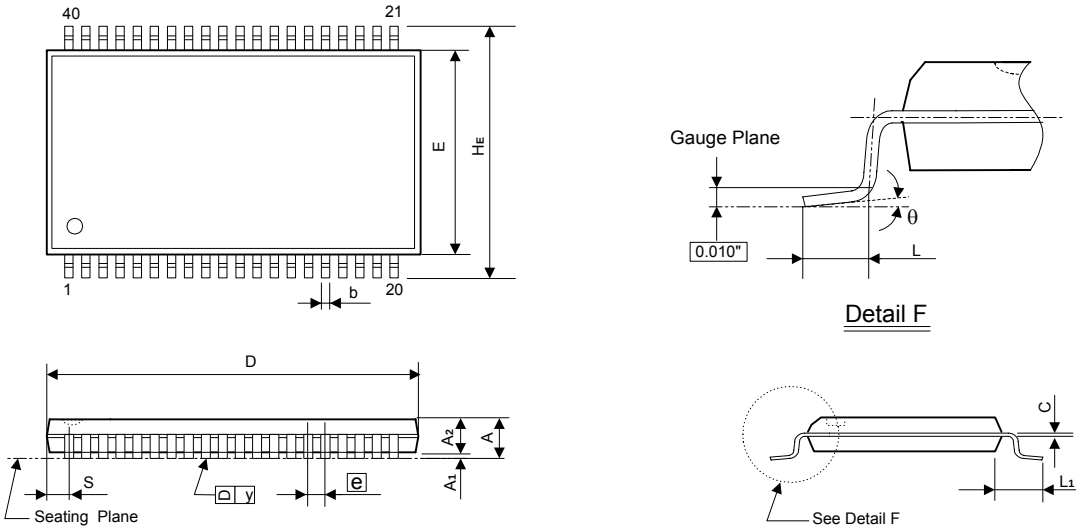


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.134	-	-	3.40
A_1	0.0185	-	-	0.47	-	-
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.021	0.41	0.46	0.54
C	0.008	0.010	0.014	0.20	0.254	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	-	-	0.003	-	-	0.075
θ	0°	-	10°	0°	-	10°

Notes:
1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

Package Information

SOP 40L Outline Dimensions unit: inches/mm

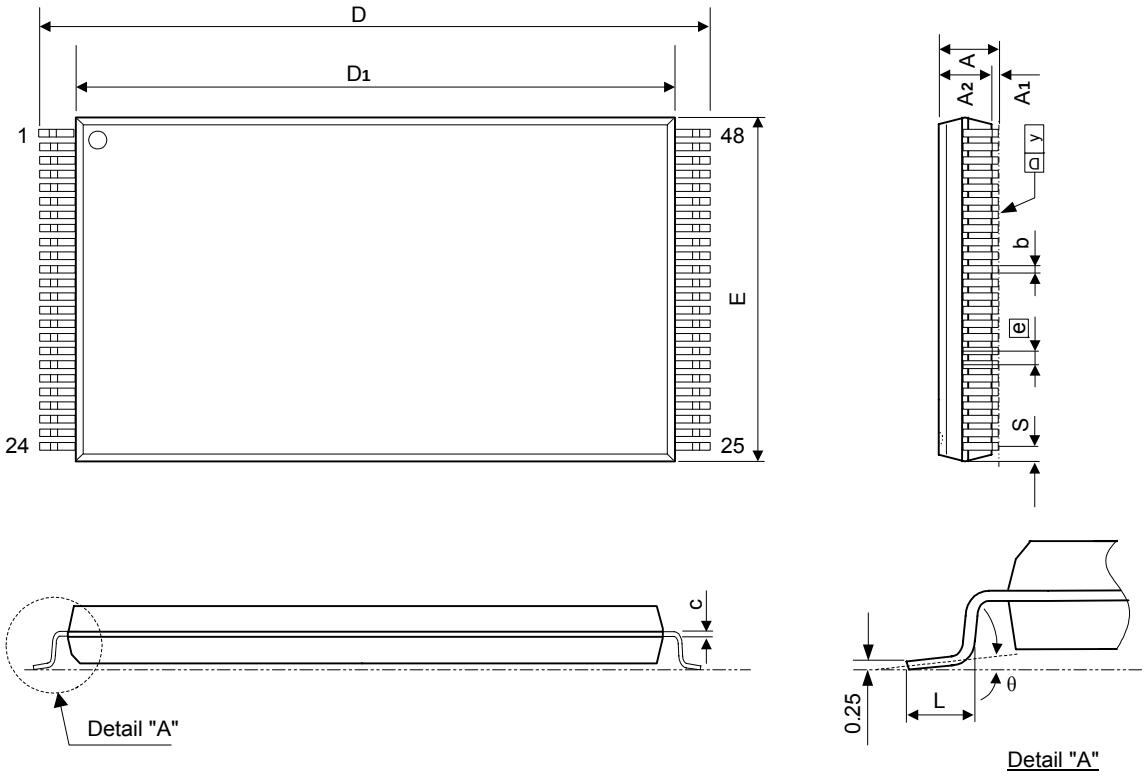


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.118	-	-	3.00
A_1	0.004	-	-	0.10	-	-
A_2	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
C	0.006	0.008	0.012	0.15	0.20	0.31
D	1.021	1.026	1.031	25.93	26.06	26.19
E	0.440	0.445	0.450	11.18	11.30	11.43
e	-	0.050	-	-	1.27	-
H_E	0.546	0.556	0.566	13.87	14.12	14.38
L	0.024	0.032	0.040	0.61	0.80	1.02
L_1	0.047	0.055	0.063	1.19	1.40	1.60
S	-	0.038	0.046	-	0.97	1.17
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information

TSOP 48L (Type I) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.042	0.94	1.00	1.06
b	0.007	0.009	0.011	0.18	0.22	0.27
c	0.004	-	0.008	0.12	-	0.20
D	0.779	0.787	0.795	19.80	20.00	20.20
D_1	0.720	0.724	0.728	18.30	18.40	18.50
E	-	0.472	0.476	-	12.00	12.10
e	0.020 BASIC			0.50 BASIC		
L	0.016	0.020	0.024	0.40	0.50	0.60
S	0.011 Typ.			0.28 Typ.		
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.