



**Document Title**

**16M(1M x 16bit) Normal mode & Page mode with Deep Power Down Static  
Random Access Memory**

**Revision history**

<b><u>Rev. No.</u></b>	<b><u>History</u></b>	<b><u>Issue Date</u></b>	<b><u>Remark</u></b>
0.0	Initial issue	May 24, 2005	Preliminary

# MEMORY

## 16M(1M x 16bit) Normal mode & Page mode with Deep Power Down Static Random Access Memory

### DESCRIPTION

The A64S06162A is a 16Mb high speed, low power Static Random Access Memory(SRAM) organized as 1,048,576 words by 16 bits and supports Deep Power Down and Page Mode. The A64S06162A is a Pseudo SRAM based on successfully proven DRAM CELL SRAM which was specifically developed for cost sensitive, low power computing and communication applications such as mobile cellular phone handsets, personal digital assistants and other battery-operated consumer products.

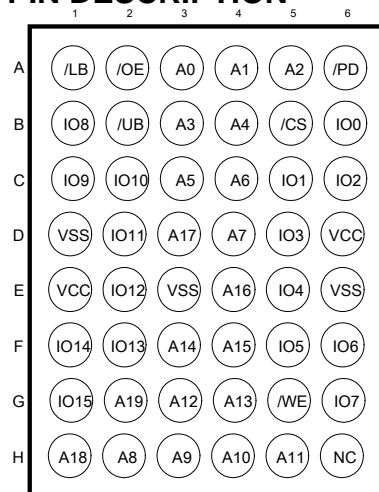
### FEATURES

- Standard Asynchronous SRAM Interface with Deep Power Down and Page Mode
- Organization : 1M x 16Bit
- Power Supply Voltage : 2.7 ~ 3.3 V
- Page Size : 4 words
- Page Mode Access (tPAA) : 35ns
- Data Retention Voltage : 2.4V
- Deep Power Down : 5uA
- Tri-state Output and TTL Compatible

### PRODUCT FAMILY

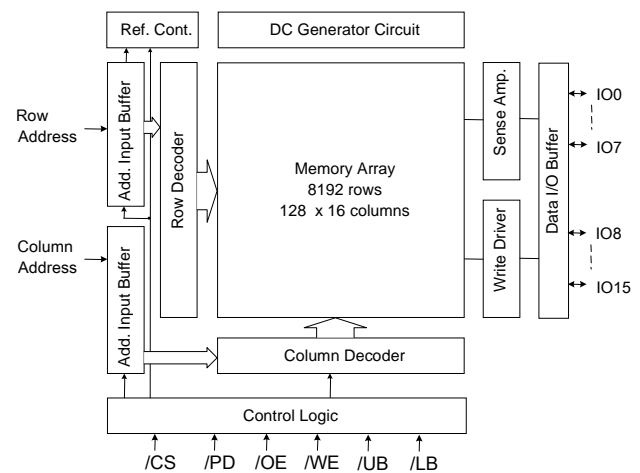
Product Family	Operating Temperature	Voltage	Speed	ISB1 (Max)	IccDR (Max)	ICC1 (Max)	Mode
A64S06162A	-40 ~ 85 °C	2.7 ~ 3.3 V	70	100uA	100uA	2.0mA	Page

### PIN DESCRIPTION



Note : E3 pin ( VSS ) can be remain as a NC

### FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
/CS	Chip Select Input	VCC	Power
/OE	Output Enable Input	VSS	Ground
/WE	Write Enable Input	/UB	Upper Byte (IO8~15)
A0~A19	Address Input	/LB	Lower Byte (IO0~7)
IO0~IO15	Data Input / Output	/PD	Deep Power Down



PRODUCT LIST

Part Name	Function
A64S06162A-70U	16M, 48-FBGA , 70 ns, 3.0V, -40°C~85°C

ABSOLUTE MAXIMUM RATING

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.2 to VCC+0.3 V	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.2 to 3.6	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage temperature	T <sub>STG</sub>	-55 to 150	°C
Operating Temperature (Extended)	T <sub>A</sub>	-40 ~ 85	°C

Note :

Stresses greater than those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS	/PD	/OE	/WE	/LB	/UB	I/O 0~7	I/O 8~15	MODE	Power
X	L	X	X	X	X	High-Z	High-Z	Deselected	Deep Power Down
H	H	X	X	X	X	High-Z	High-Z	Deselected	Standby
X	H	X	X	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	H	L	H	L	L	Data Out	Data Out	Word Read	Active
L	H	X	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	H	X	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	H	X	L	L	L	Data In	Data In	Word Write	Active

**RECOMMENDED DC OPERATING CONDITIONS <sup>1)</sup>**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage <sup>(5)</sup>	V <sub>cc</sub>	2.7	3.0	3.3	V
Ground	V <sub>ss</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	0.8*V <sub>cc</sub>	-	V <sub>cc</sub> +0.2 <sup>2)</sup>	V
Input Low Voltage	V <sub>IL</sub>	-0.2 <sup>3)</sup>	-	0.4	V

Note :

1. T<sub>A</sub> = -40°C to 85°C, otherwise specified.
2. Overshoot : V<sub>cc</sub> + 1.0V in case of pulse width ≤ 20 ns.
3. Undershoot : -1.0V in case of pulse width ≤ 20 ns.
4. Overshoot and undershoot are sampled, not 100% tested.
5. Stable power supply required 100 us before device operation.

**CAPACITANCE (T<sub>A</sub> = 25 °C, f = 1.0MHz)**

Symbol	Parameter	Condition	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IO</sub> = 0V	10	pF

Note : This parameter is sampled and not 100% tested

**DC AND OPERATING CHARACTERISTICS**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>ss</sub> to V <sub>cc</sub>	-1		1	uA
Output Leakage Current	I <sub>LO</sub>	/CS = V <sub>IH</sub> , /UB=/LB= V <sub>IH</sub> or /OE=V <sub>IH</sub> or /WE=V <sub>IL</sub> , V <sub>IO</sub> =V <sub>ss</sub> to V <sub>cc</sub>	-1		1	uA
	I <sub>cc1</sub>	Cycle Time = 1 us, 100% duty, I <sub>IO</sub> =0mA, /CS ≤ 0.2V, V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>cc</sub> -0.2V			2.0	mA
	I <sub>cc2</sub>	Cycle time=Min, I <sub>IO</sub> =0mA, 100% duty /CS = V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>			20	mA
	I <sub>ccp</sub>	/CS1 = V <sub>IL</sub> , CS2=V <sub>IH</sub> , T <sub>pwc</sub> = min Page address cycling			10	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2 mA			0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.2			V
Standby Current(TTL)	I <sub>SB</sub>	/CS=V <sub>IH</sub> , /UB=/LB= V <sub>IH</sub> , Other inputs = V <sub>IH</sub> or V <sub>IL</sub>			0.3	mA
Standby Current(CMOS)	I <sub>SB1</sub>	/CS ≥ V <sub>cc</sub> -0.2V, /UB=/LB ≥ V <sub>cc</sub> -0.2V (/UB,/LB Controlled) Other inputs = 0 or V <sub>cc</sub>			100	uA
Deep Power Down Current	I <sub>SB2</sub>	/PD ≤ V <sub>ss</sub> +0.2V			5	uA

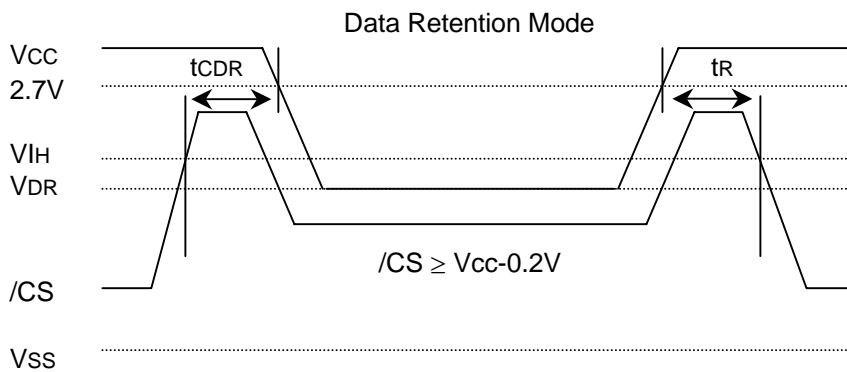
**Data Retention Electric Characteristic**

T<sub>A</sub> = -40°C to 85°C (Normal), unless otherwise specified

Item	Symbol	Test Condition	Min	Typ. (1)	Max	Unit
Voltage for Data Retention	VDR	/CS=/PD=V <sub>IH</sub> > V <sub>CC</sub> -0.2V or /UB,/LB≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤V <sub>SS</sub> + 0.2V	2.4		3.3	V
Data Retention Current	I <sub>CCDR</sub>	V <sub>CC</sub> =2.4V, /CS=/PD=V <sub>IH</sub> > V <sub>CC</sub> -0.2V or /UB,/LB≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤V <sub>SS</sub> + 0.2V			100	uA
Chip Deselect to Data Retention Time	t <sub>CDR</sub>	Refer to data retention wave form	0	-	-	ns
Operating Recovery Time	t <sub>R</sub>		t <sub>RC</sub>	-	-	ns

(1) V<sub>CC</sub> = 2.4V, T<sub>A</sub> = 25°C

**Data Retention Wave Form**

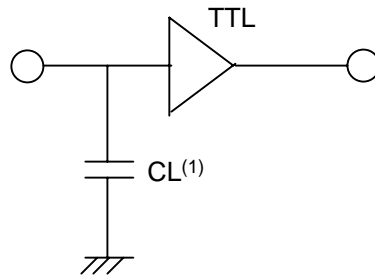


**AC TEST CONDITIONS**

T<sub>A</sub> = -40°C to 85°C (Normal), unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 30pF + 1TTL Load

**AC TEST LOADS**



Note : (1) Including jig and scope capacitance

**POWER UP TIME**

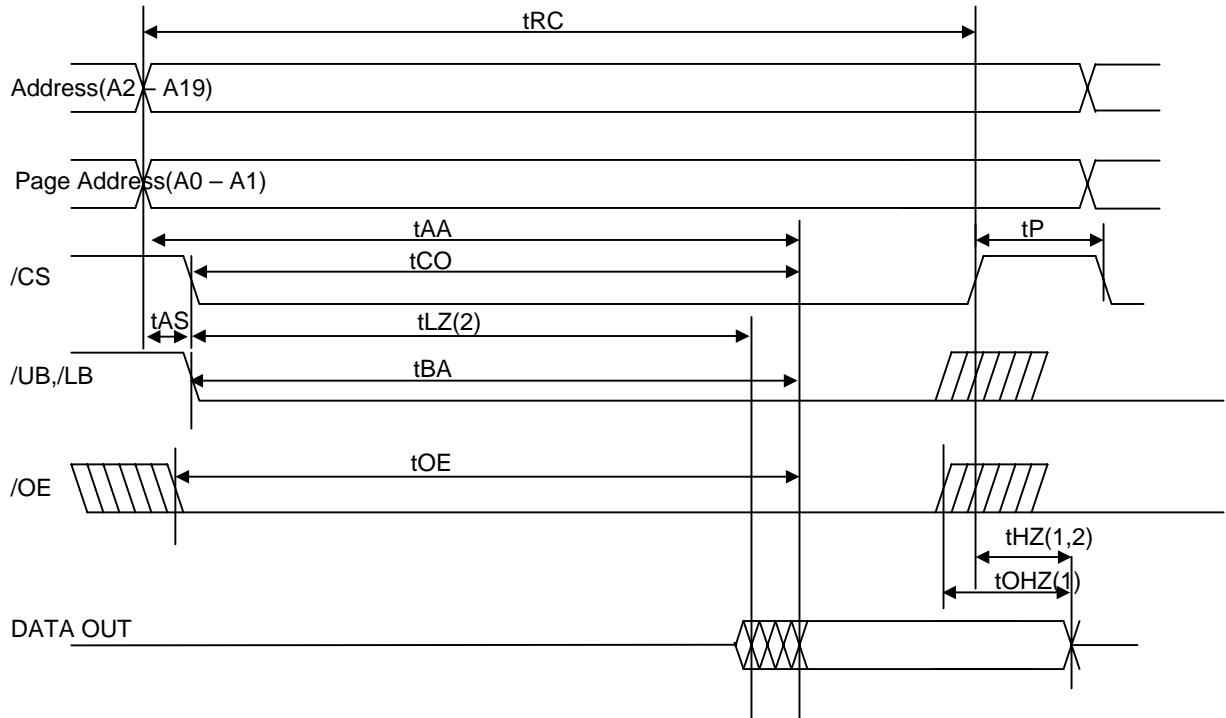
At starting, maintain stable power for a minimum 100us with /CS = /PD = high.

**AC CHARACTERISTICS** ( $V_{CC} = 2.7 \sim 3.3V$ ,  $T_A = -40$  to  $85^\circ C$ )

Parameter List		Symbol	70ns		Unit
			Min	Max	
R E A D	Read Cycle Time	tRC	70		ns
	Address Set-up Time	tAS	0		ns
	Address Access Time	tAA		70	ns
	Chip Select to Output	tCO		70	ns
	Output Enable to Valid Output	tOE		35	ns
	/UB,/LB Access Time	tBA		70	ns
	Chip select to Low-Z Output	tLZ	10		ns
	/UB, /LB Enable to Low-Z Output	tBLZ	10		ns
	Output Enable to Low-Z Output	tOLZ	5		ns
	Chip Disable to High-Z Output	tHZ	0	25	ns
	/UB, /LB Disable to High-Z Output	tBHZ	0	25	ns
	Output Disable to High-Z Output	tOHZ	0	25	ns
	Output Hold from Address Change	tOH	10		ns
	Page Read Precharge Time	tP	10		ns
	Page Read Cycle Time	tPRC	35		ns
	Page Read Address Access Time	tPAA		35	ns
W R I T E	Write Cycle Time	tWC	70		ns
	Chip Select to End of Write	tCW	60		ns
	Address Valid to End of Write	tAW	60		ns
	/UB, /LB Valid to End of Write	tBW	60		ns
	Write Pulse Width	tWP	50		ns
	Write Recovery Time	tWR	0		ns
	Write to Output High-Z	tWHZ	0	20	ns
	Data to Write Time Overlap	tDW	40		ns
	Data Hold from Write Time	tDH	0		ns
	End of Write to Output Low-Z	tOW	5		ns
	Page Write Precharge Time	tP	10		ns
	Page Write Cycle Time	tPWC	35		ns
	Page Write Data to Write Time overlap	tPDW	20		ns
	Page Write Data Hold from Write Time	tPDH	0		ns

**TIMING DIAGRAMS**

**READ CYCLE** ( $/PD = /WE = V_{IH}$ )

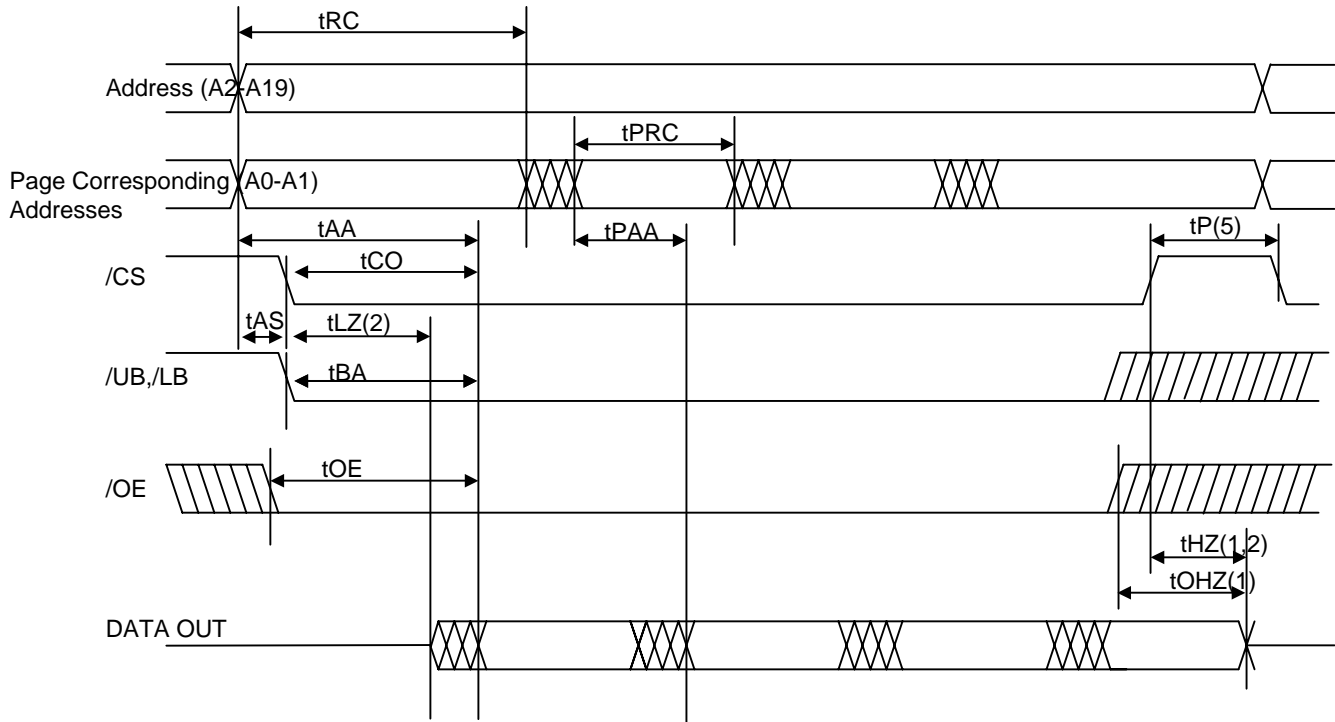


**Note (READ CYCLE) :**

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition,  $t_{HZ}(\text{max.})$  is less than  $t_{LZ}(\text{min.})$  both for a given device and from device to device.
3.  $/WE$  is high for the read cycle.
4. Do not access device with cycle timing shorter than  $t_{RC}$  for continuous periods  $> 16\mu\text{s}$ .



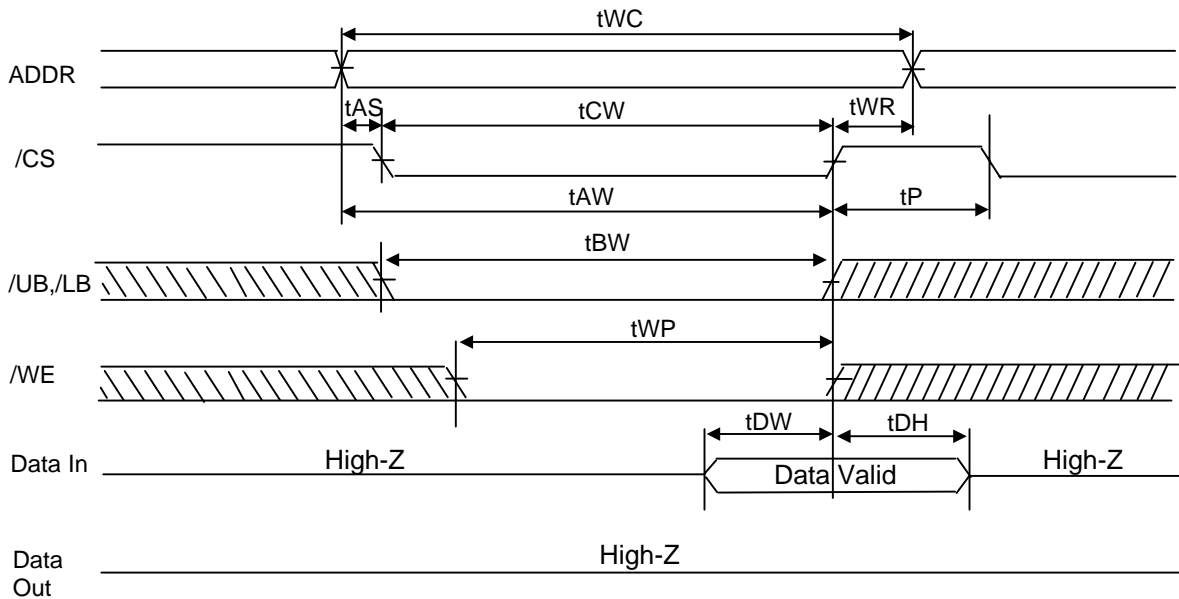
**PAGE READ CYCLE** ( $/PD = /WE = V_{IH}$ )



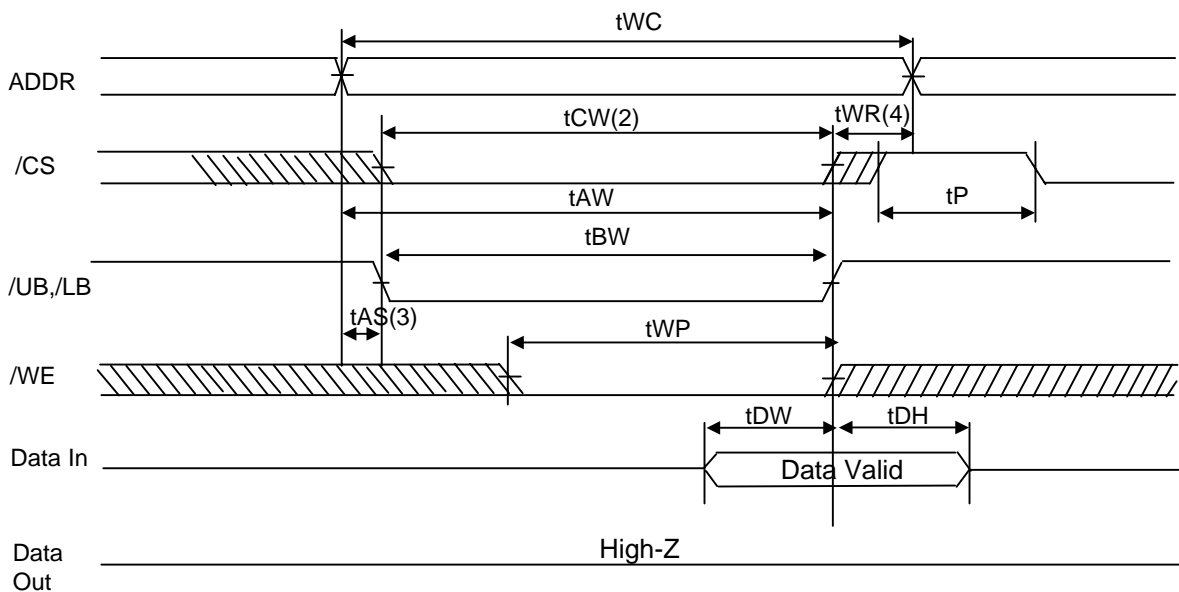
**Note (PAGE MODE READ CYCLE) :**

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition,  $t_{HZ}(\text{max.})$  is less than  $t_{LZ}(\text{min.})$  both for a given device and from device to device.
3.  $/WE$  is high for the read cycle.
4. Do not access device with cycle timing shorter than  $t_{RC}$  for continuous periods  $> 16\mu\text{s}$ .
5.  $t_P$  (precharge time) should be guaranteed for **new Address**.
6. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page

**WRITE CYCLE 1 (/CS Controlled, /PD = V<sub>IH</sub>)**



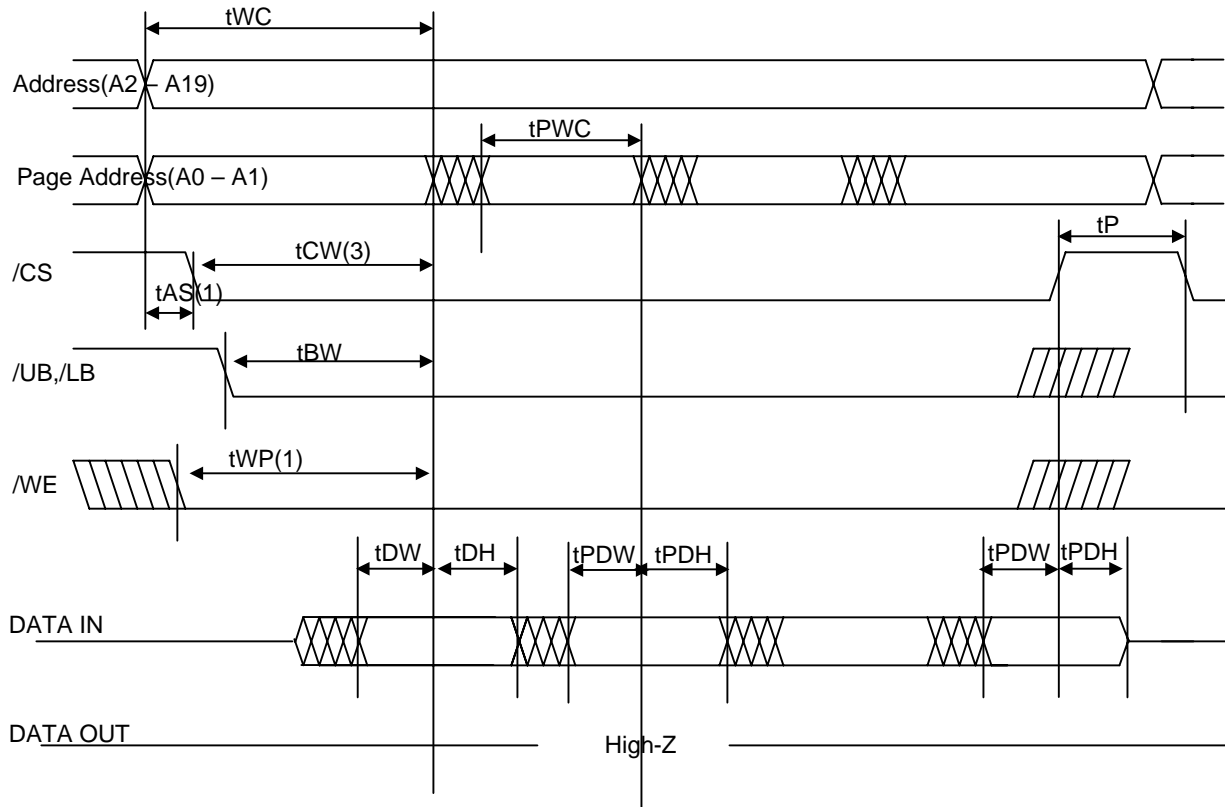
**WRITE CYCLE 2 (/UB /LB Controlled, /PD = V<sub>IH</sub>)**



**Notes (WRITE CYCLE) :**

1. A write occurs during the overlap of a low /CS and low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of /CS going low to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  is applied in case a write ends as /CS.
5. Do not access device with cycle timing shorter than  $t_{RC}$  for continuous periods > 16 $\mu$ s.

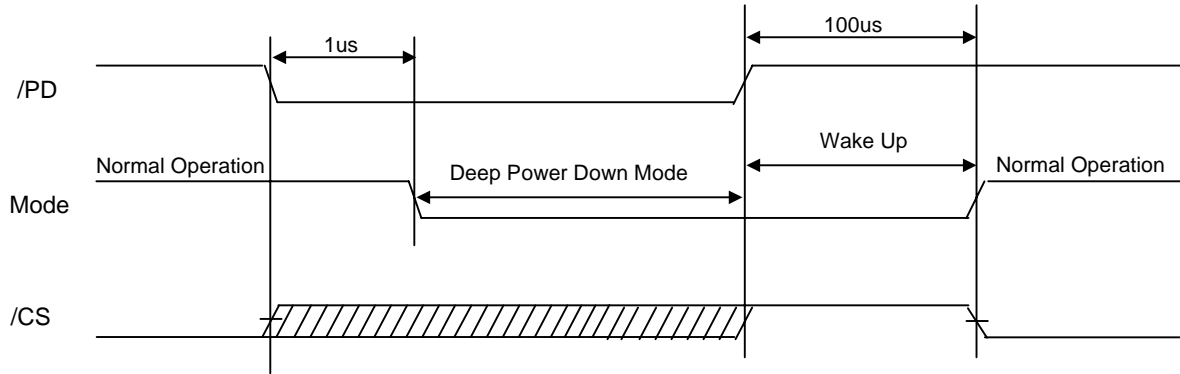
**PAGE MODE WRITE CYCLE** ( $/PD = V_{IH}$ )



**Notes (PAGE MODE WRITE CYCLE) :**

1. A write occurs during the overlap of a low  $/CS$  and low  $/WE$ .  
 A write begins at the latest transition among  $/CS$  going low in initial page mode .  
 A write end at the earliest transition among  $/CS$  going high and **Page Address transition**.  
 $tWP$  is measured from the beginning of write to the end of write in initial page access.
2.  $tPWC$  is measured from Page Address transition (After initial page access) to Page Address transition or  $/CS$  going high.
2.  $tCW$  is measured from the later of  $/CS$  going low to the end of write in initial page access.
3.  $tAS$  is measured from the address valid to the beginning of write.
4. Do not access device with cycle timing shorter than  $tRC$  for continuous periods > 16us.
5.  $tP$  (precharge time) should be guaranteed for new Page Address.
6. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page

**Deep Power Down Mode**





**Ordering Information**

<b>Part No.</b>	<b>Access Time (ns)</b>	<b>Operating Current Max. (mA)</b>	<b>Power Down Mode Standby Current Max. (μA)</b>	<b>Package</b>
A64S06162AG-70	70	20	5	48B Mini BGA
A64S06162AG-70F	70	20	5	48B Pb-Free Mini BGA
A64S06162AG-70U	70	20	5	48B Mini BGA
A64S06162AG-70UF	70	20	5	48B Pb-Free Mini BGA

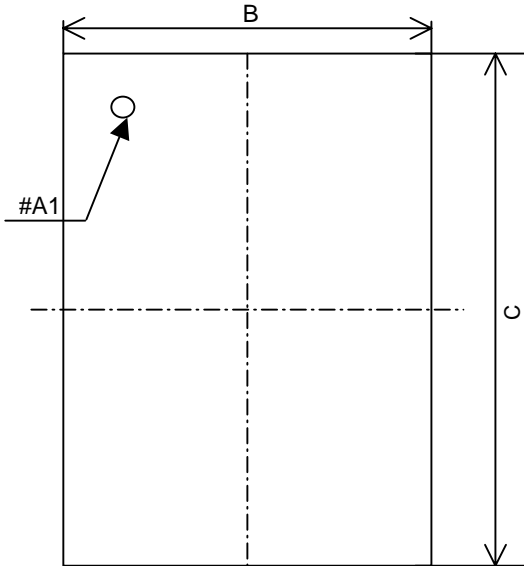
•Note : -U is for -40c ~ 85c temperature grade

**PACKAGE DIMENSION FOR BGA TYPE**

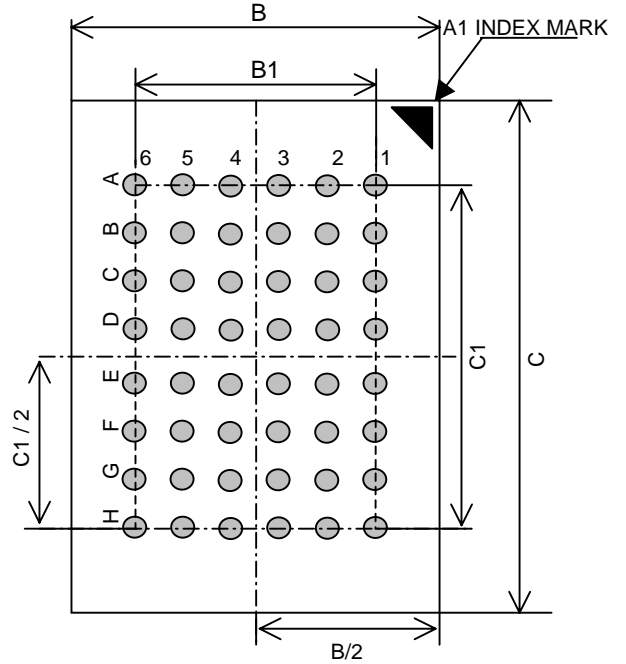
Unit: millimeters

48 BALL FINE PITCH 6mm x 8mm BGA(0.75mm ball pitch)

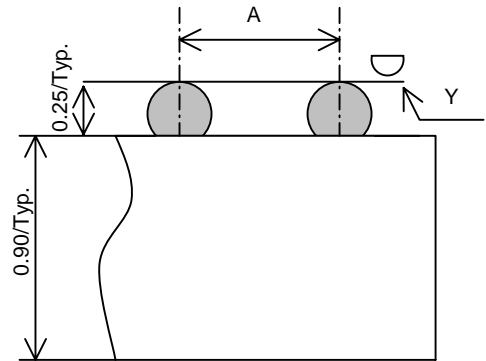
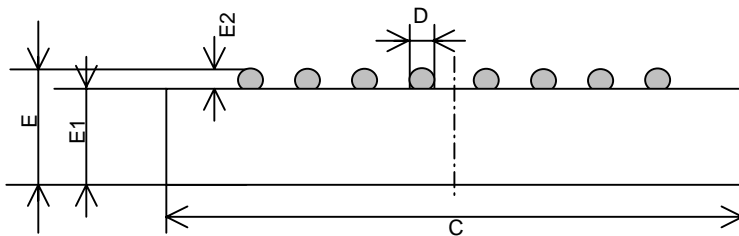
Top View



Bottom View



Side View



	Min	Typical	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	-	1.20
E1	-	-	0.90
E2	0.20	0.25	0.30
Y	-	-	0.10