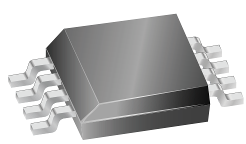
Wide Input Voltage 3.0 A Step Down Regulator

Features and Benefits

- 8 to 25 V input range
- Integrated DMOS switch
- Adjustable fixed off-time
- Highly efficient
- Adjustable 0.8 to 20 V output

Package: 8-Lead SOIC with exposed thermal pad (suffix LJ)



Approximate Scale 1:1

Description

The A8698 is a constant off-time current mode step-down regulator with a wide input voltage range. Regulation voltage is set by external resistors, to output voltages as low as 0.8 V.

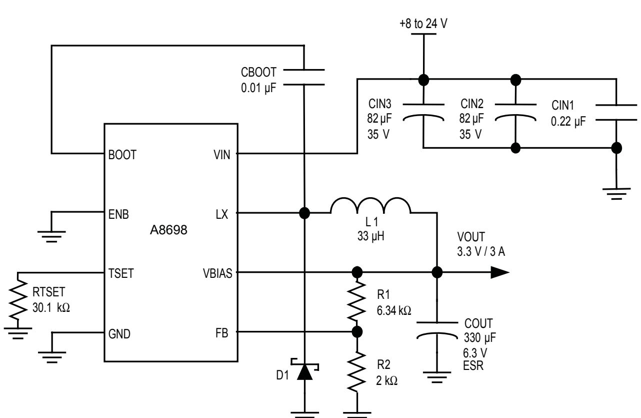
The A8698 includes an integrated power DMOS switch to reduce the total solution footprint. It also features internal compensation, allowing users to design stable regulators with minimal design efforts.

The off-time can be set with an external resistor, allowing flexibility in inductor selection. Additionally, the A8698 has a logic level enable pin which can shut the device down and put it into a low quiescent current mode for power sensitive applications.

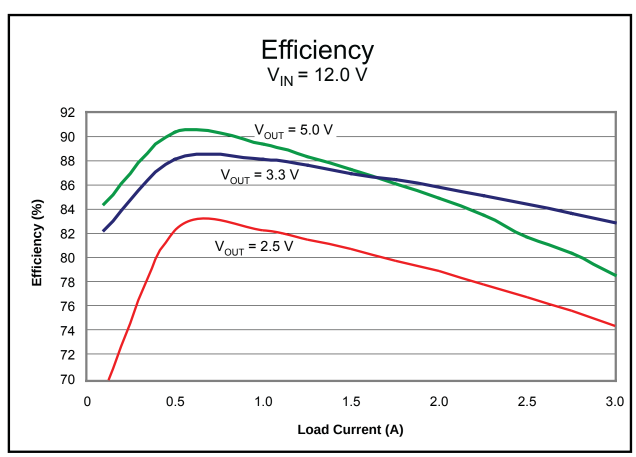
The A8698 is supplied in a low-profile 8-lead SOIC with exposed pad (package LJ). Applications include:

- Applications with 8 to 25 V input
- Consumer electronics, networking equipment
- 12 V lighter-powered applications (portable DVD, etc.)
- Point of Sale (POS) applications

Typical Application



Circuit for 12 V step down to 3.3 V at 3 A.



Efficiency curves for circuit at left.

Absolute Maximum Ratings

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Units
VIN Supply Voltage	V_{IN}		–	–	25	V
VBIAS Input Voltage	V_{BIAS}		–0.3	–	7	V
Switching Voltage	V_S		–1	–	–	V
ENB Input Voltage	V_{ENB}		–0.3	–	7	V
Operating Ambient Temperature Range	T_A	Range E	–40	–	85	°C
Junction Temperature	T_J(max)		–	–	150	°C
Storage Temperature	T_S		–55	–	150	°C

*Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current ratings, or a junction temperature, T_J, of 150°C.

Package Thermal Characteristics*

Package	$R_{\theta JA}$ (°C/W)	PCB
LJ	35	4-layer

* Additional information is available on the Allegro website.

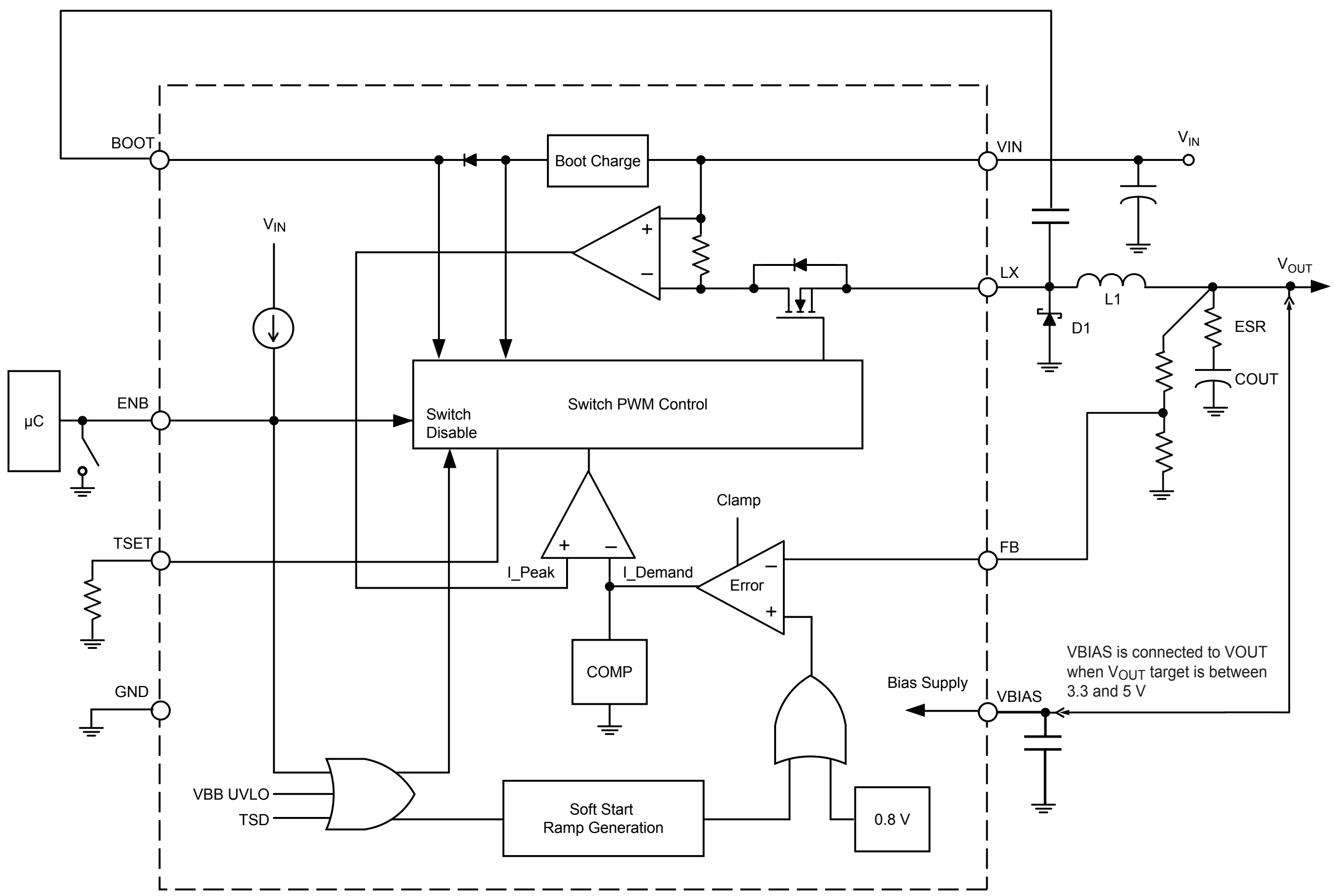
Ordering Information

Use the following complete part numbers when ordering:

Part Number[a]	Packing[b]	Description
A8698ELJTR-T	13 in. reel, 3000 pieces/reel	LJ package, SOIC surface mount with exposed thermal pad
A8698ELJ-T	98 pieces/tube	

[a]Leadframe plating 100% matte tin.
[b]Contact Allegro for additional packing options.

Functional Block Diagram



Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000
www.allegromicro.com

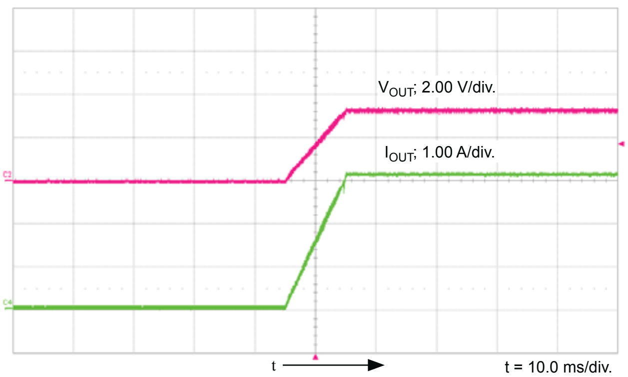
ELECTRICAL CHARACTERISTICS[1,2] at T_A = 25°C, V_{IN} = 8 to 25 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
VIN Quiescent Current	$I_{VIN(Q)}$	V_{ENB} = LOW, V_{IN} = 12 V, V_{BIAS} = 3.2 V, V_{FB} = 1.5 V (not switching)	–	1.0	–	mA
		V_{ENB} = LOW, V_{IN} = 12 V, V_{BIAS} < 3 V, V_{FB} = 1.5 V	–	4.1	–	mA
		V_{ENB} = HIGH	–	–	100	μA
VBIAS Input Current	I_{BIAS}	$V_{BIAS} = V_{OUT}$	–	3.8	5	mA
Buck Switch On Resistance	$R_{DS(on)}$	T_A = 25°C, I_{OUT} = 3 A	–	180	–	mΩ
Fixed Off-Time Proportion		Based on calculated value	–15	–	15	%
Feedback Voltage	V_{FB}		0.784	0.8	0.816	V
Output Voltage Regulation	V_{OUT}	I_{OUT} = 0 mA to 3 A	–3	–	3	%
Feedback Input Bias Current	I_{FB}		–400	–100	100	nA
Soft Start Time	t_{ss}		5	10	15	ms
Buck Switch Current Limit	I_{CL}	V_{FB} > 0.4 V	3.5	–	5	A
		V_{FB} < 0.4 V	–	1.15	–	A
ENB Open Circuit Voltage	V_{OC}	Output disabled	2.0	–	7	V
ENB Input Voltage Threshold	$V_{ENB(0)}$	LOW level input (Logic 0), output enabled	–	–	1.0	V
ENB Input Current	$I_{ENB(0)}$	V_{ENB} = 0 V	–10	–	–1	μA
VIN Undervoltage Threshold	V_{UVLO}	V_{IN} rising	6.6	6.9	7.2	V
VIN Undervoltage Hysteresis	$V_{UVLO(hys)}$	V_{IN} falling	0.7	–	1.1	V
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	$T_{JTSD(hys)}$	Recovery = $T_{JTSD} - T_{JTSD(hys)}$	–	15	–	°C

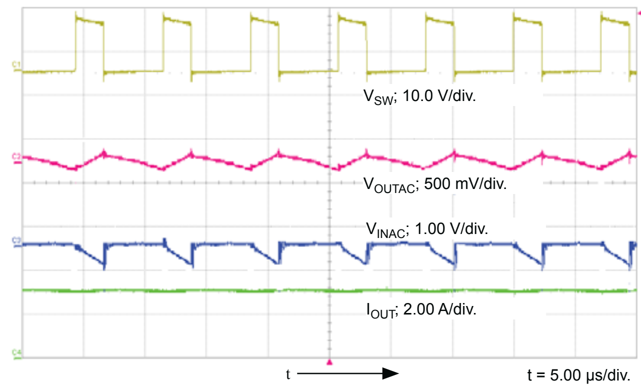
[1]Negative current is defined as coming out of (sourcing) the specified device pin.
[2]Specifications over the junction temperature range of 0ºC to 125ºC are assured by design and characterization.

Performance Characteristics

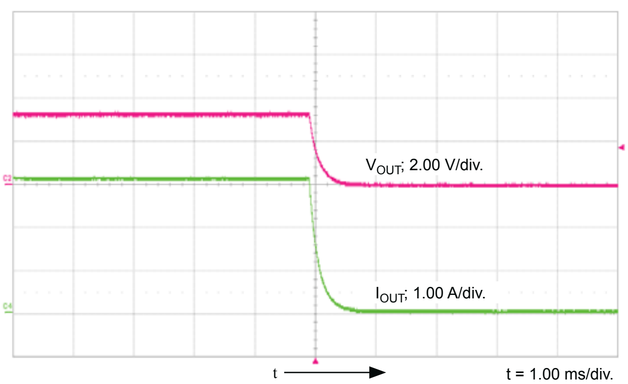
Start-up



Operation

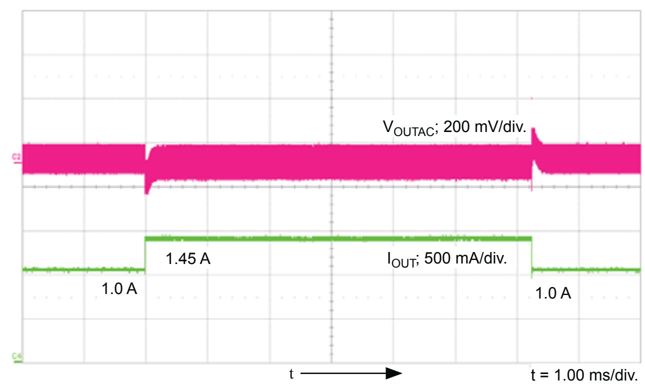


Power Off



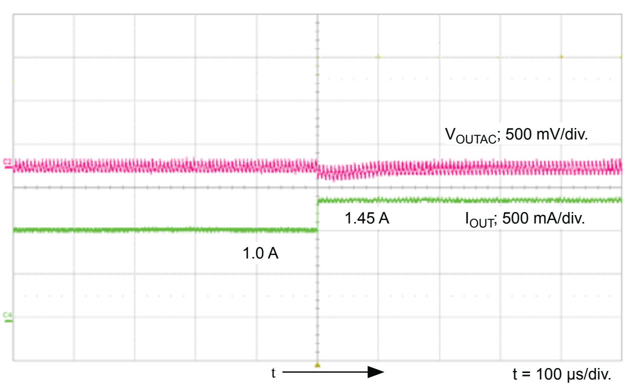
Transient Response

V_{IN} = 12 V, V_{OUT} = 3.3 V



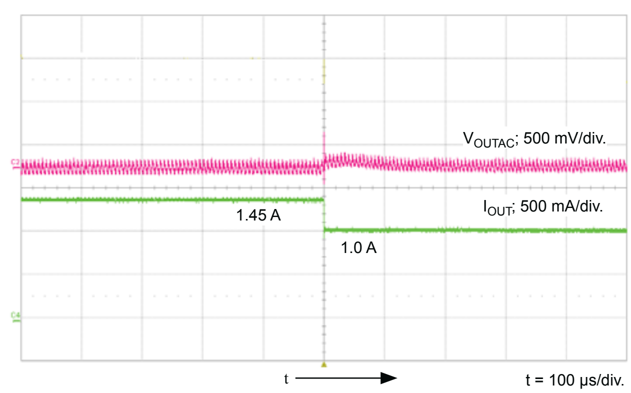
Detail: Step Up Transient Response

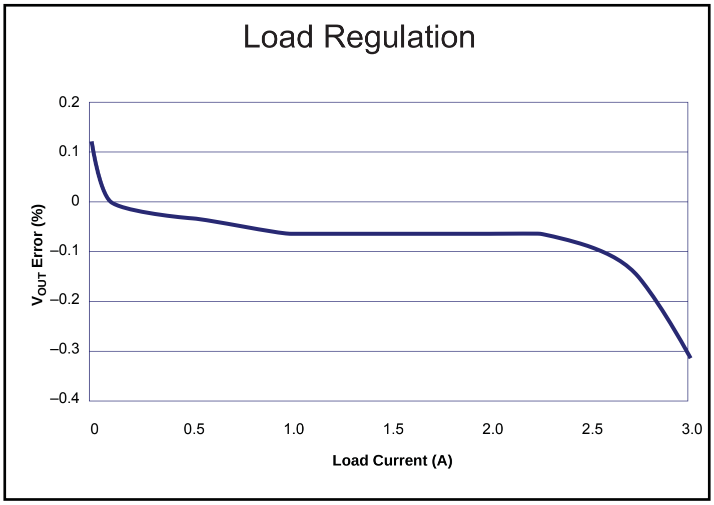
V_{IN} = 12 V, V_{OUT} = 3.3 V

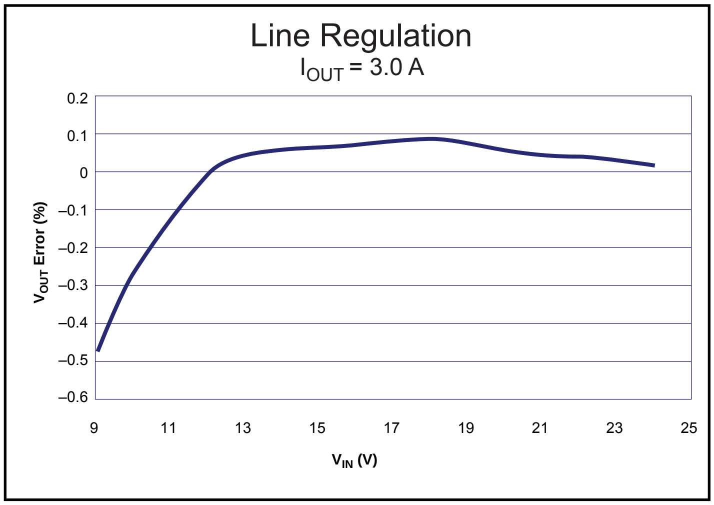


Detail: Step Down Transient Response

V_{IN} = 12 V, V_{OUT} = 3.3 V




Load Regulation
0.2
0.1
0
–0.1
–0.2
–0.3
–0.4
VOUT Error (%)
0
0.5
1.0
1.5
2.0
2.5
3.0
Load Current (A)


Line Regulation
IOUT = 3.0 A
0.2
0.1
0
–0.1
–0.2
–0.3
–0.4
–0.5
–0.6
VOUT Error (%)
9
11
13
15
17
19
21
23
25
VIN (V)

Functional Description

The A8698 is a fixed off-time, current-mode–controlled buck switching regulator. The regulator requires an external clamping diode, inductor, and filter capacitor, and operates in both continuous and discontinuous modes. An internal blanking circuit is used to filter out transients resulting from the reverse recovery of the external clamp diode. Typical blanking time is 200 ns.

The value of a resistor between the TSET pin and ground determines the fixed off-time (see graph in the t_{OFF} section).

V_{OUT}. The output voltage is adjustable from 0.8 to 20 V, based on the combination of the value of the external resistor divider and the internal 0.8 V ±2% reference. The voltage can be calculated with the following formula:

$$V_{OUT} = V_{FB} \times (1 + R1/R2) \quad (1)$$

Light Load Regulation. To maintain voltage regulation during light load conditions, the switching regulator enters a cycle-skipping mode. As the output current decreases, there remains some energy that is stored during the power switch minimum on-time. In order to prevent the output voltage from rising, the regulator skips cycles once it reaches the minimum on-time, effectively making the off-time larger.

Soft Start. An internal ramp generator and counter allow the output to slowly ramp up. This limits the maximum demand on the external power supply by controlling the inrush current required to charge the external capacitor and any dc load at startup. Internally, the ramp is set to 10 ms nominal rise time. During soft start, current limit is 3.5 A minimum.

The following conditions are required to trigger a soft start:

- $V_{IN} > 6$ V
- ENB pin input falling edge
- Reset of a TSD (thermal shut down) event

V_{BIAS}. To improve overall system efficiency, the regulator output, V_{OUT}, is connected to the VBIAS input to supply the operating bias current during normal operating conditions. During startup the circuitry is run off of the VIN supply. VBIAS should be connected to VOUT when the V_{OUT} target level is between 3.3 and 5 V. If the output voltage is less than 3.3 V, then the A8698 can operate with an internal supply and pay a penalty in efficiency, as the bias current will come from the high voltage supply, VIN. VBIAS can also be supplied with an external voltage source. No power-up sequencing is required for normal opperation.

ON/OFF Control. The ENB pin is externally pulled to ground to enable the device and begin the soft start sequence. When the ENB is open circuited, the switcher is disabled and the output decays to 0 V.

Protection. The buck switch will be disabled under one or more of the following fault conditions:

- $V_{IN} < 6$ V
- ENB pin = open circuit
- TSD fault

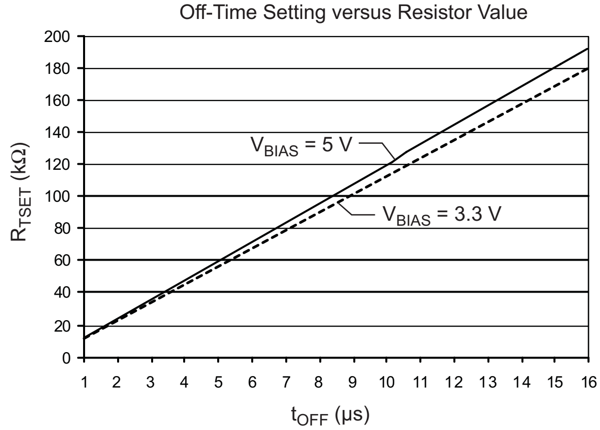
When the device comes out of a TSD fault, it will go into a soft start to limit inrush current.

t_{OFF}. The value of a resistor between the TSET pin and ground determines the fixed off-time. The formula to calculate t_{OFF} (μs) is:

$$t_{OFF} = R_{SET}\left(\frac{1–0.03\ V_{BIAS}}{10.2 \times 10^9}\right) \quad (2)$$

where R_{TSET} (kΩ) is the value of the resistor. Results with the VBIAS pin connected are shown in the following graph (when VBIAS is not connected, use $V_{BIAS} = 0$ in equation 2):

Off-Time Setting versus Resistor Value



t_{ON}. From the volt-second balance of the inductor, the turn-on time, t_{on}, can be calculated approximately by the equation:

$$t_{ON} = \frac{(V_{OUT} + V_f + I_{OUT} \times R_L) \times t_{OFF}}{V_{IN} - I_{OUT} \times R_{DS(on)} - I_{OUT} \times R_L - V_{OUT}} \quad (3)$$

where

V_f is the voltage drop across the external Schottky diode,
R_L is the winding resistance of the inductor, and

$R_{DS(on)}$ is the on-resistance of the switching MOSFET.

The switching frequency is calculated as follows:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} \quad (4)$$

Shorted Load. If the voltage on the FB pin falls below 0.4 V, the regulator will invoke a 1.5 A typical overcurrent limit to handle the shorted load condition at the regulator output. For low output voltages at power up and in the case of a shorted output, the off-time is extended to prevent loss of control of the current limit due to the minimum on-time of the switcher.

The extension of the off-time is based on the value of the TSET multiplier and the FB voltage, as shown in the following table:

V_{FB} (V)	TSET Multiplier
< 0.16	$8 \times t_{OFF}$
< 0.32	$4 \times t_{OFF}$
< 0.5	$2 \times t_{OFF}$

Component Selection

L1. The inductor must be rated to handle the total load current. The value should be chosen to keep the ripple current to a reasonable value. The ripple current, I_{RIPPLE}, can be calculated by:

$$I_{RIPPLE} = V_{L(OFF)} \times t_{OFF} / L \quad (5)$$

$$V_{L(OFF)} = V_{OUT} + V_f + I_{L(AV)} \times R_L \quad (6)$$

Example:

Given V_{OUT} = 3.3 V, V_f = 0.55 V, V_{IN} = 12 V, I_{LOAD} = 3.0 A, power inductor with L = 33 µH and R_L = 0.05 Ω Rdc at 55°C, t_{OFF} = 2.67 µs, and $R_{DS(on)}$ = 0.2 Ω.

Substituting into equation 6:

$$V_{L(OFF)} = 3.3\text{ V} + 0.55\text{ V} + 3.0\text{ A} \times 0.05\ \Omega = 4.0\text{ V}$$

Substituting into equation 5:

$$I_{RIPPLE} = 4.0\text{ V} \times 2.67\ \mu\text{s} / 33\ \mu\text{H} = 323\text{ mA}$$

The switching frequency, f_{SW}, can then be estimated by:

$$f_{SW} = 1 / (t_{ON} + t_{OFF}) \quad (7)$$

$$t_{ON} = I_{RIPPLE} \times L / V_{L(ON)} \quad (8)$$

$$V_{L(ON)} = V_{IN} - I_{L(AV)} \times R_{DS(on)} - I_{L(AV)} \times R_L - V_{OUT} \quad (9)$$

Substituting into equation 9:

$$V_{L(ON)} = 12\text{ V} - 3\text{ A} \times 0.2\ \Omega - 3\text{ A} \times 0.05\ \Omega - 3.3\text{ V} = 7.95\text{ V}$$

Substituting into equation 8:

$$t_{ON} = 323\text{ mA} \times 33\ \mu\text{H} / 7.95\text{ V} = 1.34\ \mu\text{s}$$

Substituting into equation 7:

$$f_{SW} = 1 / (2.67\ \mu\text{s} + 1.34\ \mu\text{s}) = 250\text{ kHz}$$

Higher inductor values can be chosen to lower the ripple current. This may be an option if it is required to increase the total maximum current available above that drawn from the switching regulator. The maximum total current available, $I_{LOAD(MAX)}$, is:

$$I_{LOAD(MAX)} = I_{CL}(\text{min}) - I_{RIPPLE} / 2 \quad (10)$$

where I_{CL}(min) is 3.5 A, from the Electrical Chracteristics table.

D1. The Schottky catch diode should be rated to handle 1.2 times the maximum load current. The voltage rating should be higher than the maximum input voltage expected during all operating conditions. The duty cycle for high input voltages can be very close to 100%.

COUT. The main consideration in selecting an output capacitor is voltage ripple on the output. For electrolytic output capacitors, a low-ESR type is recommended.

The peak-to-peak output voltage ripple is simply I_{RIPPLE} × ESR. Note that increasing the inductor value can decrease the ripple current. The ESR should be in the range from 50 to 500 mΩ.

If a low ESR capacitor is used, such as a POSCAP or SP, an extra R_r, C_r circuit is needed to inject ripple into the feedback pin and ensure stability. Please refer to the Application Circuit section for the connection. The R_r should be much larger than the feedback resistor to prevent any potential offset in output voltage. For example, if $R_f < 10$ kΩ, R_r should be 1 MΩ. C_r should be selected based on the following equation:

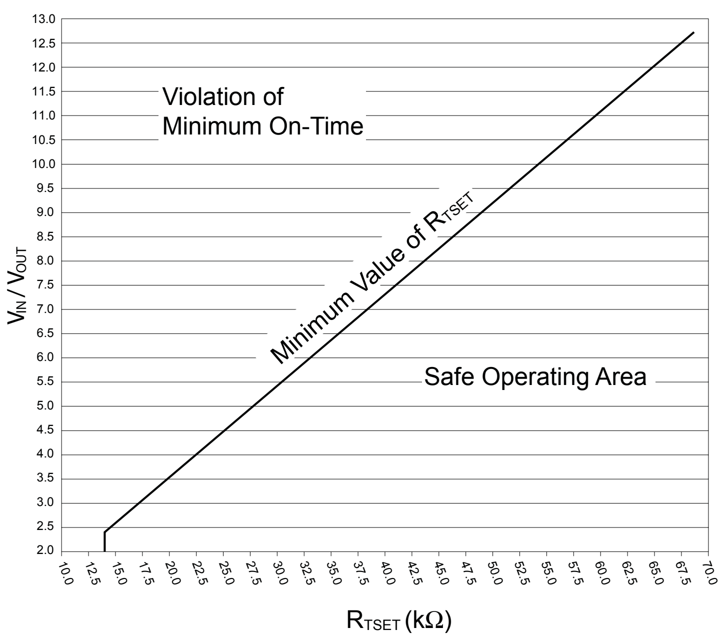
$$C_r(\max) = \frac{(V_{IN}(\min) - V_{FB}) \times t_{ON}(\min)}{0.05 \times R_r} \quad (5)$$

where Cr is in pF, $t_{ON}(\min)$ is in µs, and R_r is in MΩ.

RTSET Selection. Correct selection of RTSET values will ensure that minimum on-time of the switcher is not violated and prevent the switcher from cycle skipping. For a given V_{IN} to V_{OUT} ratio, the RTSET value must be greater than or equal to the value defined by the curve in the plot below.

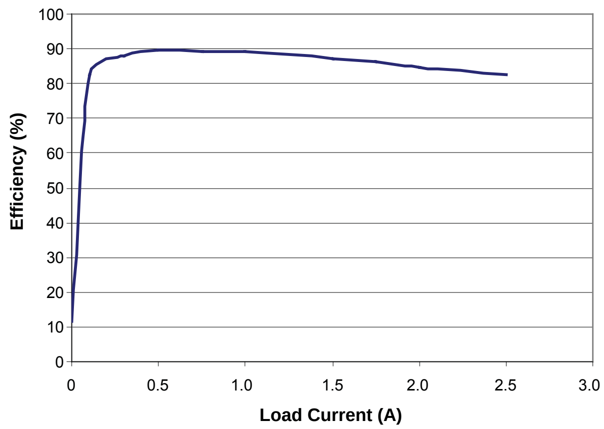
Note. The curve represents the minimum RTSET value. When calculating R_{TSET}, be sure to use $V_{IN}(\max) / V_{OUT}(\min)$. Resistor tolerance should also be considered, so that under no operating conditions the resistance on the TSET pin is allowed to go below the minimum value.

FB Resistor Selection. The impedance of the FB network should be kept low to improve noise immunity. Large value resistors can pick up noise generated by the inductor, which can affect voltage regulation of the switcher.

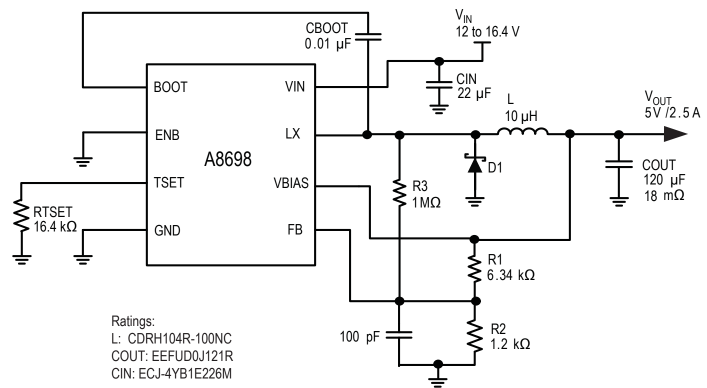


Application Circuit

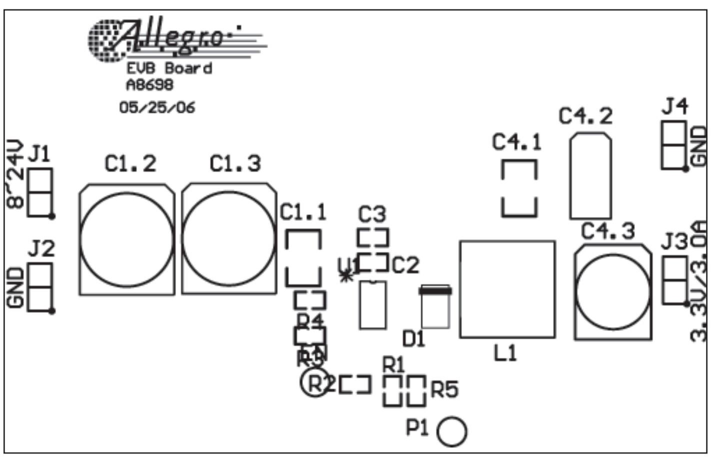
Efficiency versus Load Current
Stabilized with low ESR capacitor



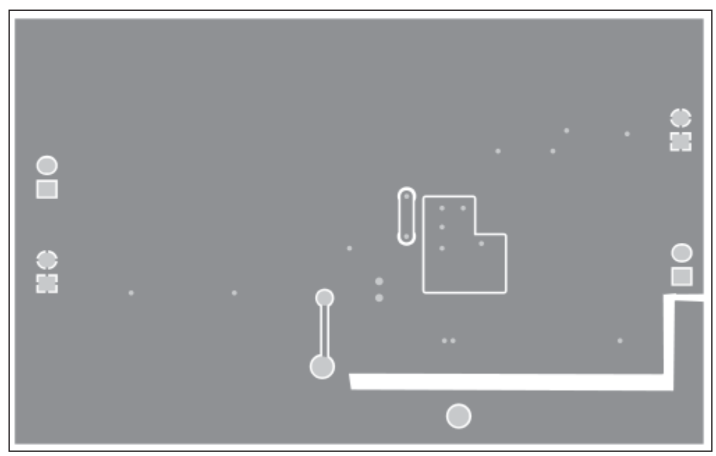
Circuit with Low ESR Capacitor
f_{SW} = 500 kHz nominal at 12 V



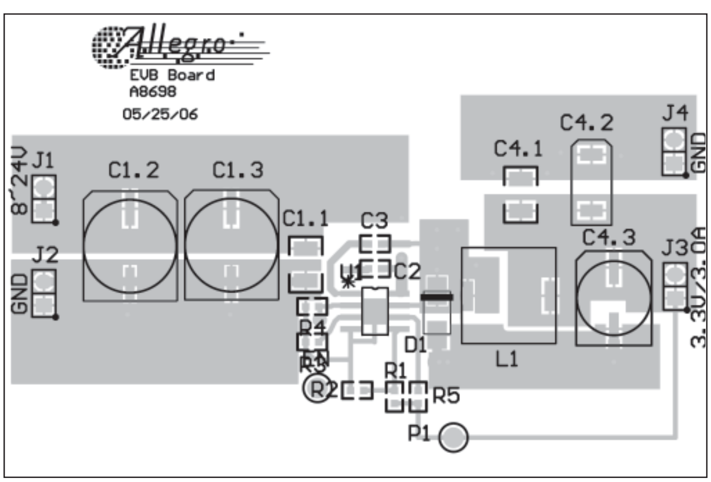
Evaluation Board



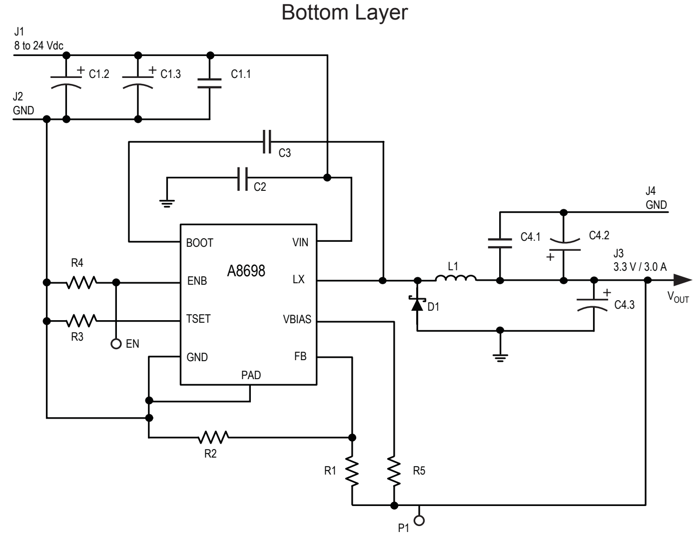
Silkscreen Layer



Bottom Layer



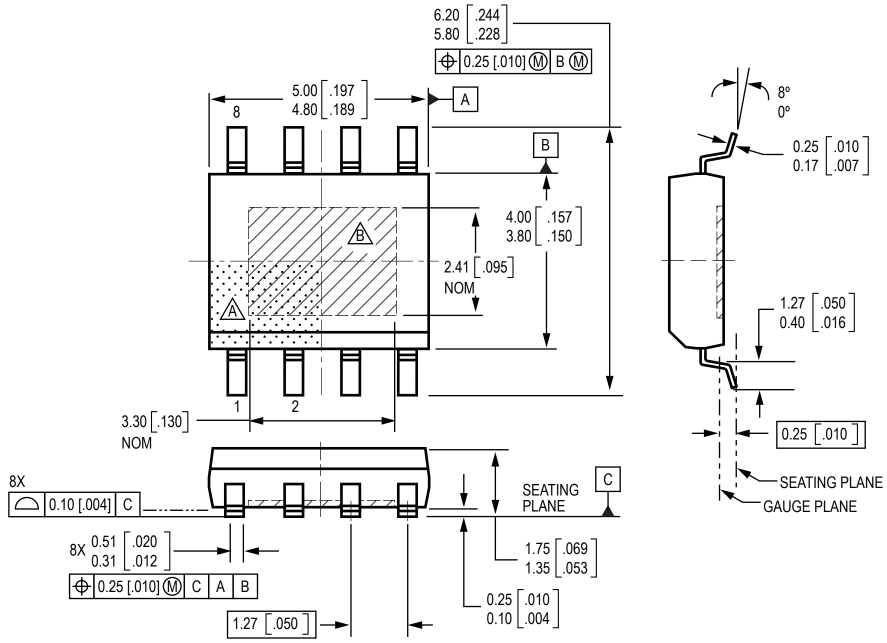
Top and Silkscreen Layers

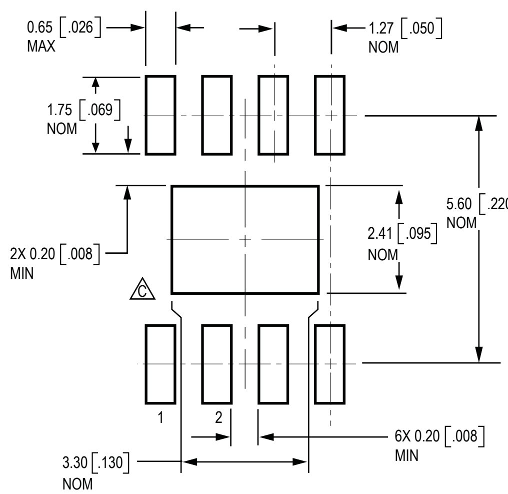


Evaluation Board Bill of Materials

Designator	Quantity	Description	Manufacturer	Footprint	Part Number
C1.1	1	Ceramic chip, 22 µF, 25 V, ±20%, X5R.	Panasonic	1210	ECJ4YB1E226M
C1.2, C1.3	2	Aluminum electrolytic capacitor, 35 V / 82 µF, 930 mA ripple current	Rubycon	8 mm × 12 mm	35V-ZAV-820-8 X 12
C2	1	Ceramic capacitor, X7R, ±10%, 0.1 µF / 50 V	Murata	0603	GRM188R71H104KA93D
C3	1	Ceramic capacitor, X7R, ±10%, 0.01 µF / 50 V	Kemet	0603	C0603C103K5RACTU
C4.2	0	Special polymer cap, 120 µF / 6.3 V, 15 mΩ	Panasonic	7.3 mm × 4.3 mm × 3.1 mm	EEFUD0J121R
C4.1	0	Ceramic capacitor, X5R, ±20%, 47 µF / 6.3 V	Panasonic	1210	ECJ4YB0J476M
C4.3	1	Aluminum electrolytic capacitor, 6.3 V / 330 µF, 450 mA ripple current, 300 mΩ	Panasonic	8 mm × 10.2 mm	EEVFC0J331P
L1	1	Inductor, 33 µH, 53 mΩ, 3.9 A, ±20%	Sumida	10.3 mm × 10.5 mm × 4 mm	CDRH127/LDNP-330MC
D1	1	Schottky diode, 40 V / 3.0 A	Diodes, Inc.	SMA	B340
R1	1	Chip resistor, 6.34 kΩ, 1/16 W, 1%	Std	0603	Std.
R2	3	Chip resistor, 2.0 kΩ,1/16 W, 1%	Std	0603	Std.
R3	1	Chip resistor, 30.1 kΩ, 1/16 W, 1%	Std	0603	Std.
R4	1	Chip resistor, 10 kΩ, 1/16 W, 1%	Std	0603	Std.
R5	1	Chip resistor, 0 Ω, 1/16 W, 1%	Std	0603	Std.
J1, J2, J3, J4	4	Header, 2-pin, 100 mil spacing	Sullins	0.100 in. × 2	PTC36SAAN
P1	1	Test point, Red, 1mm	Farnell	0.038 in.	240-345
EN	1	Test point, Black, 1mm	Farnell	0.038 in.	240-333
U1	1	Wide Input Voltage Step Down Regulator	Allegro	ESOIC8	A8698

Package LJ 8-Pin SOIC





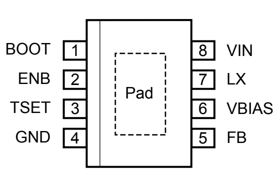
All dimensions reference, not for tooling use
(reference JEDEC MS-012 AA)
Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-9AM); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Pin-out Diagram



(Top View)

Terminal List Table

Number	Name	Description
1	BOOT	Gate drive boost node
2	ENB	On/off control; logic input
3	TSET	Off-time setting
4	GND	Ground
5	FB	Feedback for adjustable regulator
6	VBIAS	Bias supply input
7	LX	Buck switching node
8	VIN	Supply input
–	Pad	Exposed pad for enhanced thermal dissipation

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