AMIS-53000 Frequency Agile Transceiver
Data Sheet

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1.0 Overview of the AMIS-53000

The AMIS-53000 is the latest highly flexible member of AMI Semiconductor's ASTRIC™ family of single-chip wireless transceivers. It is ideally suited for low to moderate data rate, low power, sub 1GHz, narrow band, FSK/GFSK/OOK, multiple channel, wireless applications in the medical, automotive and industrial markets. The AMIS-53000 can easily be interfaced to a base band processor via a serial interface bus.

1.1 Applications for the AMIS-53000

- Medical Implantable Communication Systems (MICS)
- Wireless Medical Telemetry Systems
- Wireless Sensors
- RFID
- Remote Monitoring
- Access Control and Security
- Keyless Entry
- Mobile Wireless Data Terminals
- Keyless Entry
- Tire Pressure Monitors
- Wireless Toys

1.2 Key Features

- Medical implant communication protocol support
- Very low power single-chip CMOS transceiver
- Patented Quick Start crystal oscillator
- Low power receive Sniff Mode™
- Periodic transmit using Burst mode
- Internal low power 10kHz oscillator
- Internal self calibration functions
- SPI/I^2C interface bus
- 3-wire/4-wire serial data interface
- Two analog to digital converter channels
- Internal fractional N frequency synthesizer
- On/off shift key/frequency shift key modulation/Gaussian FSK (BT = 1)
- Internal temperature sensor
- Minimal external components

1.3 Technical Features

- Operating voltage range: 2.2 to 3.3V
- Operating temperature range: -40° to +85°C
- Operating frequency range: 300 to 928MHz
- Data rate:
  - 1 to 19.2kbps (OOK)
  - 2 to 128kbps (FSK/GFSK)
- Transmit output power:
  - +15dBm max (high power)
  - +0dBm max (low power)
- Transmit current: 50mA typical (15dBm)

- Receiver sensitivity
  - –115dBm (OOK @ 1kbps)
  - –105dBm (FSK @ 20kbps)
- Receiver current: 12mA (continuous)
- Minimum RX energy detect time: 130uS (Sniff)

1.4 Circuit Overview

1.4.1. Transmitter

The AMIS-53000 uses a driver and class E power amplifier to output the on/off shift keyed or frequency shift keyed RF waveforms. The class E power amplifier has two output power ranges allowing more efficient output power for the one setting up to 0dBm output and the other setting for output power greater than 0dBm. The class E power amplifier can achieve output power of +12dBm to +15dBm for frequencies in the range of 300MHz to 915MHz. The output power is programmable in each of the two output power bands.

The transmit data can be NRZ or Manchester encoded. Data can also be modulated as on/off shift keyed or frequency shift keyed. Data rates for the OOK modulation can be as high as 19.2kbps. Data rates for the FSK/GFSK modulation can be as high as 128kbps. The carry frequency deviation for the FSK modulation is programmable, typically one half to one times the data rate.

The transmit data output can be wave shaped with a Gaussian format. This can reduce the occupied bandwidth of the signal.

1.4.2. Receiver

The AMIS-53000 has a single receiver channel and a single transmit channel, which can be connected to individual antennas or can be combined into a single antenna. The receiver uses four different methods to receive and recover data that has been on/off shift keyed or frequency shift keyed modulated. The FSK/GFSK data is recovered using either a PLL circuit or a FFT circuit along with a CDR circuit. The OOK data is recovered using an RSSI circuit along an optional CDR circuit. It is suggested that the CDR circuit be used when receiving OOK signals.

1.4.2.1. On/Off Shift Key Modulation

The AMIS-53000 uses a logarithmic received signal strength indicator (RSSI) detector to recover the data from the on/off shift keyed modulated waveform. Data rates can be up to 19.2kbps. The AMIS-53000 has eight discrete data filters for common baud rates. The receiver can detect either NRZ or Manchester encoded data.

1.4.2.2. Low Data Rate Frequency Shift Key Modulation

The AMIS-53000 uses a digital PLL detector to recover the data from the frequency shift keyed data below 20kbps. The recovered data waveform is applied to the clock and data recovery circuit to produce the digital data and a synchronized clock. The receiver can detect either NRZ or Manchester encoded data.

1.4.2.3. High Data Rate Frequency Shift Key Modulation

The AMIS-53000 uses a fast fourier transform (FFT) to recover data from frequency shift keyed modulated waveforms when the data rate is higher than 20kbps. The data rate can be as high as 128kbps. The demodulated data waveform is applied to the clock and data recovery circuit to produce the digital data and a synchronized clock. The receiver can detect either NRZ or Manchester encoded data.

1.4.2.4. Clock and Data Recovery

The AMIS-53000 uses a clock and data recovery circuit along with the frequency shift keyed or on/off shift keyed data detector circuits to recover the data stream. The CDR circuit synchronizes a clock with the data rate of the received data. This same circuit can be used with the on/off shift keyed waveform.

1.4.2.5. Manchester Data Encoding

The AMIS-53000 can encode the data as NRZ or Manchester.

1.4.2.6. Oscillators

The AMIS-53000 requires a single external crystal working with the internal VCO and PLL to generate frequencies from 300MHz to 928MHz. The AMIS-53000 has internal capacitors that eliminate the need for external load capacitors when using a typical 24MHz external crystal. The VCO requires an external inductor and capacitor (including internal capacitance) to produce the desired transmit or receive RF frequency. The AMIS-53000 generates the desired RF transmit and receive frequencies from 300MHz to 928MHz by selecting the proper inductor and capacitor value along with programming the frequency in the AMIS-53000. A patented Quick Start circuit is used to force the crystal oscillator on to the desired frequency in microseconds rather than in milliseconds.

A low power internal 10kHz oscillator provides the timing for Sniff, Burst and housekeeping. The AMIS-53000 self-calibration circuits can tune this oscillator to within two percent of 10kHz.

1.4.2.7. Interface Serial Bus

The AMIS-53000 has separate interfaces for data and control. The transfer of TX/RX data between the AMIS-53000 and an external host/controller is done with a 3-wire serial interface or a 4-wire SPI compatible serial interface. Control information is written to the AMIS-53000 registers or read from the AMIS-53000 registers using either a 3-wire serial interface or a 2-wire I^2C compatible serial interface.

Once the AMIS-53000 configuration registers have data written to them for various operational modes such as, TX, RX, Sniff or other, placing the AMIS-53000 into one of these modes is accomplished through a single write to the command register.

TX/RX Data Interface

The transmit or receive data interface of the AMIS-53000 can be programmed to be either a proprietary 3-wire serial interface or a 4-wire SPI compatible serial bus. The data interface can be set up to do either data transfers into a buffer in the AMIS-53000 or streaming data (data is transmitted as it is received by the AMIS-53000 or data is sent to the host/controller as it is recovered in the AMIS-53000 receiver). When using the buffered data mode, the AMIS-53000 can be the master or slave, but it must be the master to do streaming data.

Control Interface

Once the AMIS-53000 is first powered on, an external host/controller sets the type of interface to the AMIS-53000 (3-wire or I^2C) by simply writing to the AMIS-53000 with the desire protocol. The AMIS-53000 will continue to use that interface protocol until power is removed from the AMIS-53000. The AMIS-53000 is always a slave device for the control interface.

2.0 Operational Specifications

2.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units	Notes
Vdd	DC Supply Voltage	-0.3	3.6	V	
Vin	Input Pin Voltage	-0.3	Vdd+0.3	V	
Iin	Input Pin Current	-10.0	10.0	mA	25C
Tstrg	Storage Temperature	-55	150	C	SSOP
Tlead	Lead Temperature		300	C	10 SEC
ESD_{HBM}	Human Body Model		2	kV	
ESD_{CDM}	Charged-Device Model		750	V	
ESD_{MM}	Machine Model		200	V	

2.2 Recommended Operating Conditions

Table 2: Operating Conditions

Symbol	Parameter	Min.	Max.	Units	Notes
Vdd	DC Supply	2.2	3.3	V	
Idd	Dynamic Current		70	mA	(1) Continuous TX
Idds	Standby Current (off current)		2	uA	(2)
Vss	Ground	0.0	0.0	V	
Ta	Ambient Temperature	-40	85	C	

Notes:
1. Dynamic current is with the transmitter enabled at maximum output power + 15dBm in FSK mode at 928MHz.
2. Standby current is with all analog cells in power down. Other logic powered up with no clocks running. All outputs unloaded and inputs tied high or low. No floating inputs.

2.2.1. Parametric Voltage and Current Levels

(Testing for the below currents assumes a static test setup with measurements performed while static data is applied to the device.)

2.2.1.1. Inputs

Table 3: Pin Input Parameters

Pin	Vil		Vih		Iil (1)		Iih (1)		Notes (2)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Min. uA	Max. uA	Min. uA	Max. uA	
AI					0.0	1.0	-1.0	0.0	Analog input
DISU	0.0	0.3	0.8	1.0	0.0	1.0	-30	-90	CMOS with pull up Schmitt
DISC	0.0	0.3	0.8	1.0	0.0	1.0	-1.0	0.0	CMOS Schmitt

Notes:
1. Iil and Iih are tested at Vdd = VDDmax volts. Not tested at less than room temperature.
2. PU = Pull up, PD = Pull down, SC = Schmitt, SU = Schmitt & Pull up and SD = Schmitt and Pull down.
3. CMOS values are 'Vin * VDD' and TTL values are absolute voltages.

2.2.1.2. Outputs

Table 4: Pin Output Parameters

Pin	Vol (1)		Voh (2)		Iol (1,3)		Ioh (2,3)		Notes
	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Min. mA	Max. mA	Min. mA	Max. mA	
AO									Analog outputs
DO	0	0.4	Vdd-.4		2		-2		CMOS

Notes:
1. Vol, Iol are tested at Vdd = VDDmin volts unless otherwise stated.
2. Voh, Ioh are tested at Vdd = VDDmin volts unless otherwise stated.
3. Polarity on currents indicates direction of current: (+) for sinking and (-) for sourcing.

2.2.1.3. I/O Pins

Table 5: I/O Pin Parameters

Pin	Vil V Min.	Vil V Max.	Vih V Min.	Vih V Max.	Vol V (1)	Vol V Max. (1)	Voh V Min. (2)	Voh V (2)	Iol mA Min. (1)	Ioh mA Min. (2)	Iozl uA Max. (3)	Iozh uA Max. (3)	Notes
AIO													
DIO	0	0.3	0.8	1	0	0.4	Vdd-.4	Vdd	2	-2	1	-1	Schmitt

Notes:
1. Vol, Iol are tested at Vdd = 3.1 volts.
2. Voh, Ioh are tested at Vdd = 3.1 volts.
3. Ioz is tested with Vdd = 3.5 volts.

*** Leakage on I/O pins is typically checked for +/- 10 microamps with the output device turned off and no PU or PD device present.

2.3 Operational Specifications

Table 6: Operational Specifications

Parameter	Min.	Typ.	Max.	Units	Comment
Receiver					
Frequency Range	300		928	MHz	
Sensitivity	-107		-114	dBm	@ 10kHz data rate (FSK/GFSK modulation)
	-104		-111	dBm	@ 10kHz data rate (OOK modulation)
Noise Figure	6.0	7.8	9.0	dB	
IIP2		+60		dBm	Dual tone test using RSSI
IIP3		+5		dBm	Dual tone test using RSSI
Image Rejection	30	40	50	dB	Modulated desired, single tone interferer
Input Impedance		15-j35		Ω	@ 900MHz series equivalent
		72-j62		Ω	@ 433MHz series equivalent
RSSI Gain	14	16	18	mV/dB	
I_{IN}		8		mA	Receiver current consumption at 900MHz
I_{SB} Full Shutdown		2		uA	Standby current (no clocks enabled)
I_{SB} Crystal Mode		2		mA	System clock output enabled (6MHz)
T_{on}		100		us	Standby to receiver on time
T_{RX_TX}/ T_{TX_RX}		100		us	Transition time from RX to TX or TX to RX
LAN					
Input Trim	1.2		4	pF	Internal capacitor range for the receiver input
Output Trim	0.32		0.912	pF	Internal capacitor range for the output of the LNA in the receiver

Table 6: Operational Specifications (Continued)

Parameter		Min.	Typ.	Max.	Units	Comment
Transmitter						
Frequency Range		300		928	MHz	
T_{on}			100		us	Standby to transmitter on time
T_{TX_RX}			100		us	Transition time from TX to RX
OOK On/Off Ratio			60		dB	
FSK Frequency Separation		0		200	kHz	Allowable transmit/receive peak deviation
CW Output Power		-20		15	dBm	Range of output power in the high power mode
		-25		0	dBm	Range of output power in the low power mode
$P_{HARMONICS}$			35		dBc	With complete matching network
TX PA						
Output Cap.		2		7.5	pF	Internal capacitor range for the PA adjustable trim
Output Switch R		5		18	Ω	
On/Off Ratio			60		dB	
Output Harmonics				-35	dBc	With typical 50Ω matching circuits
Operating Current			50	68	mA	15dBm CW
Operating Current			12	24	mA	0dBm CW
MAX Power	High Power	14	16.5	17	dBm	Matching network for 50Ω 928MHz high
	Low Power	-1	4.5	5.7	dBm	
MAX Power	High Power	15.8	16.5	17	dBm	Matching network for 50Ω 433MHz high
	Low Power	3	4	5	dBm	
Crystal Oscillator						
Center Frequency			24		MHz	Trimmed
Tolerance				20	ppm	Required crystal tolerance
Startup Time			50	100	us	Quick Start enabled
Startup Time			2	5	ms	Quick Start disabled
Trim Cap		0		45	pF	Internal trim capacitor (self calibration sets)
Trim Resolution		145	160	175	fF	
Idd			800		uA	Normal operation
Idd			1.5		mA	During Quick Start
10kHz Oscillator						
Output Frequency		9.8	10	10.2	kHz	After trimming
Operating Current		300	375	450	nA	After trimming
Duty Cycle			50		%	
ADC						
Resolution			8		Bits	
FSR		Vss		Vref	V	Full scale input range
Ci			1		pF	Input capacitance
Vref			2.0		V	Internal voltage reference
Reference Offset			1		%FSR	
fclk		0.01		2	MHz	Clock frequency
Conversion Rate				200	KSPS	Clock rate = 2MHz
Conversion Time			10		Tclk	

Table 6: Operational Specifications (Continued)

Parameter	Min.	Typ.	Max.	Units	Comment
Data Filter					
3dB Down Point	110	120	130	$\%F_{DATA}$	AM data filter bandwidth (relative to associated defined data rates)
Temperature Sensor					
Output Voltage	0.93	0.97	1.01	V	At 27°C
Voltage Range	0.61	0.97	1.4	V	Output
Slope		-5.24		mv/°C	dV/dT
RSSI Buffer					
Input Range	0		Vdd	V	
Operating Current	135	185	250	uA	
Unity Gain-BW	615	1000	1700	kHz	100kΩ/100pF load
PLL					
Reference Input Frequency		12		MHz	Transmit mode (24MHz external crystal)
		16		MHz	Receive mode (24MHz external crystal)
Resolution		91.55		Hz	Frequency step size
VCO Gain Constant	9.62	12	14.4	MHz/V	@ 400MHz
	25.6	32	38.4	MHz/V	@ 900MHz
					@ 900MHz, although layout PCB parasitics and component placement will change this value
Settling Time		100		us	Internal loop filter
Phase Noise		-90	-80	dBc/Hz	Internal loop filter @ 10kHz offset
Phase Noise		-120	-110	dBc/Hz	Internal loop filter @ 3MHz offset
Max Spurious Level		-70	-50	dBc	Internal loop filter
POR					
Delay Time	28	43	60	ms	
Brown-out Trip	1.2	1.6	1.8	V	

3.0 Block Diagrams

3.1 AMIS-53000 Overall Block Diagram

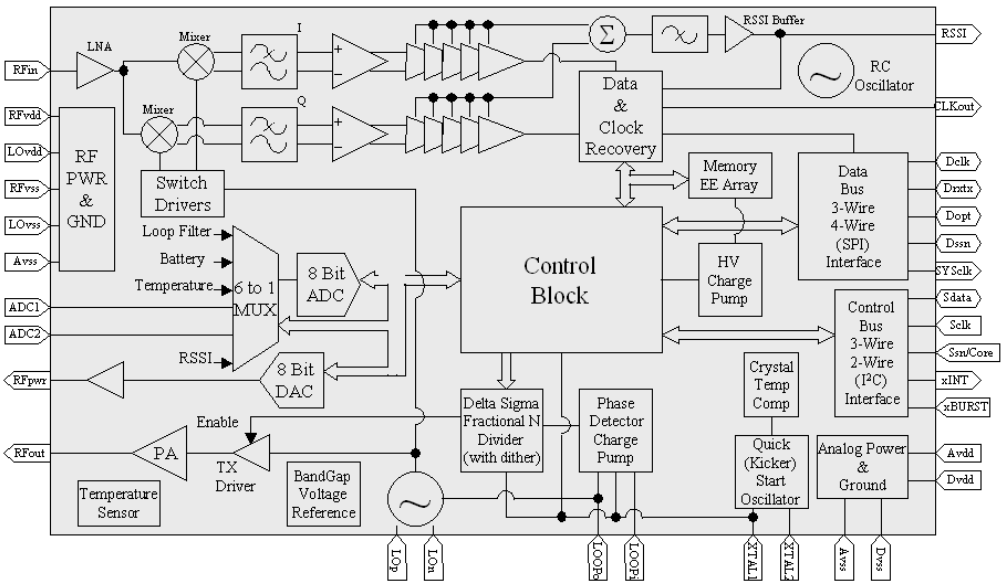


Figure 1: AMIS-53000 Block Diagram

3.2 Package

3.2.1. Pin Definition

Table 7: Pin Definitions

Pin#	-001	-002	Pin Type	Description
1	LNAvdd	LNAvdd	Power	A DC short (inductor) is connected to VDD from this pin
2	RFin	RFin	Analog Input	The RF input to the receiver circuits
3	RFvss	RFvss	Ground	Ground for the RF circuits
4	RFout	RFout	Analog Output	RF transmit output
5	RFpwr	RFpwr	Analog Output	Variable DC voltage output to power the RF transmitter (requires a DC short {inductor} connection to Rfout)
6	Avdd	Avdd	Power	Vdd power for the analog circuits
7	ADC1	ADC1	Analog Input	Input to the analog to digital conversion circuit
8	ADC2	ADC2	Analog Input	Input to the analog to digital conversion circuit
9	RSSI	RSSI	Analog IO	Analog voltage related to the strength of the received RF
10	PEAK	PEAK	Analog	Analog voltage for external auto-slice capacitor
11	Avss	Avss	Ground	Ground for the analog circuits
12	XTAL2	XTAL2	Analog	Connection to an external crystal
13	XTAL1	XTAL1	Analog	Connection to an external crystal
14	INT	INT	Digital Output	Interrupt to external controller
15	Dopt	Dopt	Digital Input	Optional data pin for the 4-wire data interface mode
16	Dssn	Dssn	Digital IO	Active low select line for the data interface

Table 7: Pin Definitions (Continued)

Pin#	-001	-002	Pin Type	Description
17	Drxtx	Drxtx	Digital IO	Serial data input (transmit) or output (received)
18	Dclk	Dclk	Digital IO	Recovered clock output (data interface clock)
19	SYSclk	SYSclk	Digital Output	System clock output
20	Dvss	Dvss	Ground	Ground for the digital circuits
21	Dvdd	Dvdd	Power	Vdd power for the digital circuits
22	CoreReg	SSN	Digital	-001 (control and status for the serial data interface) -002 (decoupling capacitor pin for the internal regulator)
23	SCLK	SCLK	Digital	Bi-directional clock for the 2-wire serial interface
24	SDATA	SDATA	Digital	Bi-directional data for the 2-wire serial interface
25	xBURST	xBURST	Digital Input	Active low input interrupt that will immediately cause a Burst transmission
26	LOOPout	LOOPout	Analog	Output to the optional external loop filter
27	LOOPin	LOOPin	Analog	Input from the optional external loop filter
28	LOvss	LOvss	Ground	Ground for the local oscillator circuits
29	LOn	LOn	Analog	Negative side of the VCO tank
30	LOp	LOp	Analog	Positive side of the VCO tank
31	LOvdd	LOvdd	Power	Vdd for the local oscillator circuits
32	RFvdd	RFvdd	Power	Vdd power for the RF circuits

3.2.2. Block Diagram/Pin Definition

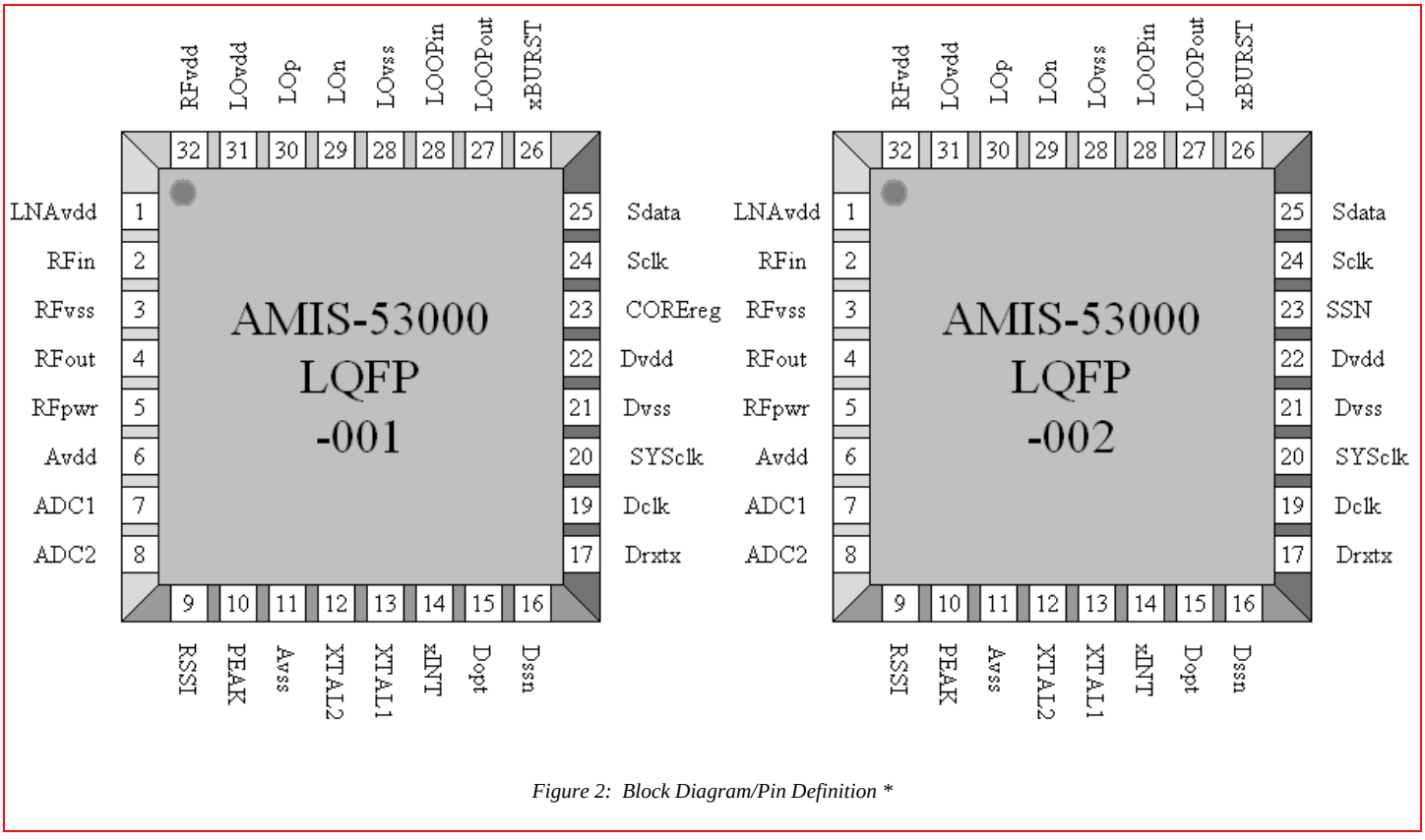


*Figure 2: Block Diagram/Pin Definition **

* Not actual package markings. Please see marking format in 3.2.3.3.

3.2.3. Physical Characteristics

3.2.3.1. Package Type

32 pin LQFP

3.2.3.2. Package Dimensions

Table 8: AMIS-53000 LQFP Package Dimensions

Symbol	Min.	Nom.	Max.	Units
Thickness	-	-	1.60	mm
D	9.00 BSC			mm
D1	7.00 BSC			mm
E	9.00 BSC			mm
E1	7.00 BSC			mm
e	0.80 BSC			mm

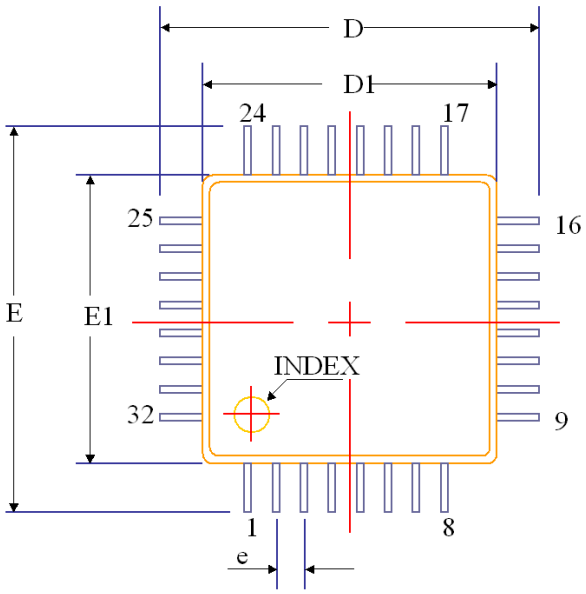


Figure 3: Package

3.2.3.3. Package Marking Format

(AMIS Logo)
AMIS53000a
19608-bbb
XXXXYZZ

Where:
a is the market application
bbb is the AMIS device version
XXXXYZZ is the date and tractability code**** is the country of origin (found on underside of chip).
The year in which the mask work was first fixed in a semiconductor chip product may also appear.

4.0 Acronyms

The following acronyms are used in this document.

AM	Amplitude Modulated signal
ASIC	Integrated circuit designed for a single customer requirement
ASK	Amplitude Shift Key
ASSP	A custom integrated circuit, that may be used in general designs
ASTRIC	AMI Semiconductor's family of wireless products
CCA	Clear Channel Assessment
CDR	Clock and Data Recovery, data is recovered from the received signal using a synchronous clock
CRC	Cyclic Redundancy Checking; data error checking
CW	Continuous Wave, a single frequency or modulated signal carrier
DAC	Digital to Analog Conversion
dB	Decibels; a logarithmic measure of signal level
dBm	Logarithmic measure of signal level above a milli-watt
DFFT	Digital or Discrete Fast Fourier Transform
DPLL	Digital Phase Locked Loop circuit to create a precise frequency
EE	Electrical Erasable Memory
FFT	Fast Fourier Transform; transform between time and frequency
FM	Frequency Modulated signal
FSK	Frequency Shift Key
GFSK	Gaussian Data Waveform Modulated signal
IF	Intermediate Frequency
kbps	Data rate in thousand bits per second
kHz	Frequency in kilohertz per second
LO	Local Oscillator frequency; used to convert signals between RF frequency and IF frequency
LOP	Byte indicating the length of a packet
MHz	Frequency in megahertz
MICS	Medical Implantable Communication System
mV	Milli-volts
OOK	On/Off method of creating an amplitude modulated signal
OTA	Transconductance Amplifier
PLL	Phase Locked Loop circuit to create a precise frequency
POR	Power-on-Reset is a threshold circuit for limiting operation at low voltages
RF	Radio Frequency
RSSI	Received Signal Strength Indication; measurement of RF signal strength
SOF	Byte indicating start of packet in data protocol
VCO	Voltage controlled variable frequency oscillator

5.0 Hardware Description

5.1 Frequency

The AMIS-53000 uses an internal VCO, PLL and trim capacitors with an external oscillator crystal to generate the RF frequencies for both TX and RX. The external crystal is a parallel resonant mode crystal with required loading capacitors. The AMIS-53000 contains internal load capacitors, typically sufficient for use with the suggested 24MHz. It is suggested that a 24MHz with 20ppm tolerance be used with the AMIS-53000.

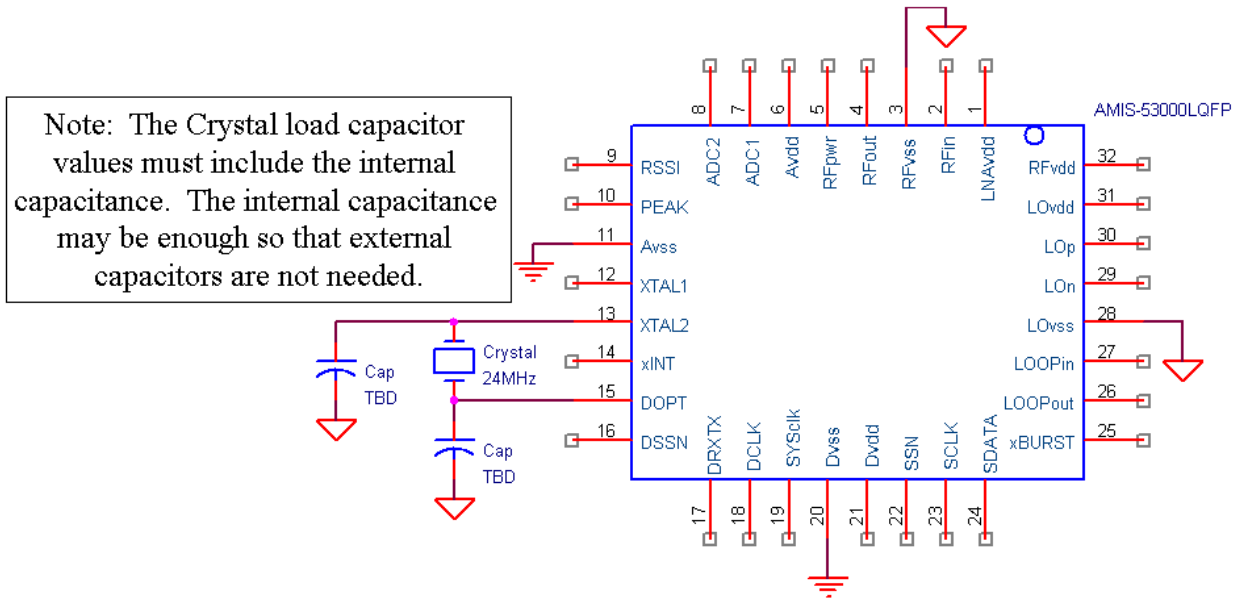


Figure 4: External Crystal Circuit

The internal VCO requires an external parallel LC to set the frequency for RX or TX. There is an internal capacitance that needs to be considered when selecting the values of the inductor and capacitor. The AMIS-53000 is sensitive to the positioning of the LC components in the layout of the PCB. The traces to the LC need to be as symmetrical as is possible. The location of the LC needs to be as close to the AMIS-53000 pins as is practical. A simple layout change to these parameters can mean that the AMIS-53000 VCO frequency will change causing a need to change the values of the inductor, capacitor and/or the values in the registers controlling the RF frequency. The value of the inductor and/or the capacitor may need to be adjusted to allow the AMIS-53000 to calibrate the PLL for a given frequency of operation. The layout of the printed circuit board for the inductor and capacitor should route traces connecting other components away from the inductor and capacitor pads.

The VCO in the AMIS-53000 is a differential negative resistance oscillator (DNRO), commonly found in the literature. It uses an internal voltage variable capacitor (varactor) in combination with an external L and C to provide the desired frequency. The output frequency is found simply by:

$$F_{vco} = \frac{1}{\sqrt{L_{tot} \cdot C_{tot}}} \frac{1}{2 \cdot \pi}$$

Where: Ltot and Ctot are the total inductance and capacitance respectively at the VCO pins. This includes the internal capacitance of approximately 2pF.

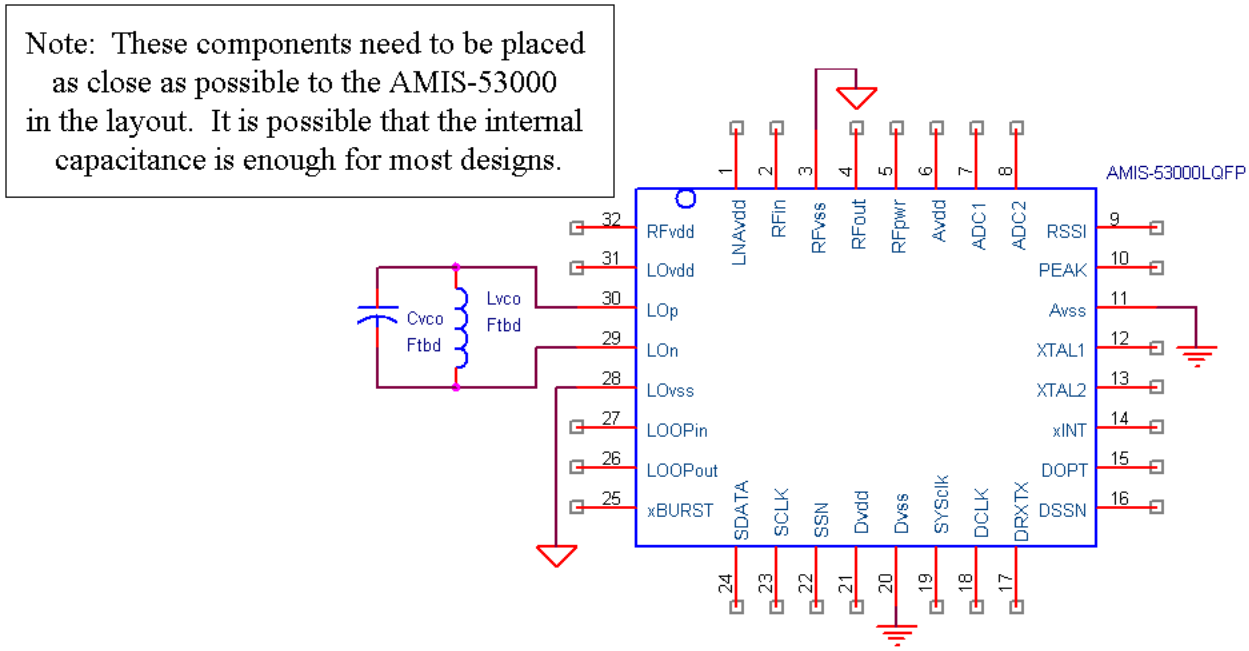


Figure 5: VCO External LC Circuit

The AMIS-53000 has an internal loop filter to work with the PLL in creating the frequency of the device. There is an option to use an external loop filter.

Table 9: Internal Loop Parameters

Filter	Component	Value	Units	Comments
Second Order	R1	60	kΩ	
	C1	64	pF	
	C2	3	pF	
Additional Pole	R	110	kΩ	
	C	1	pF	

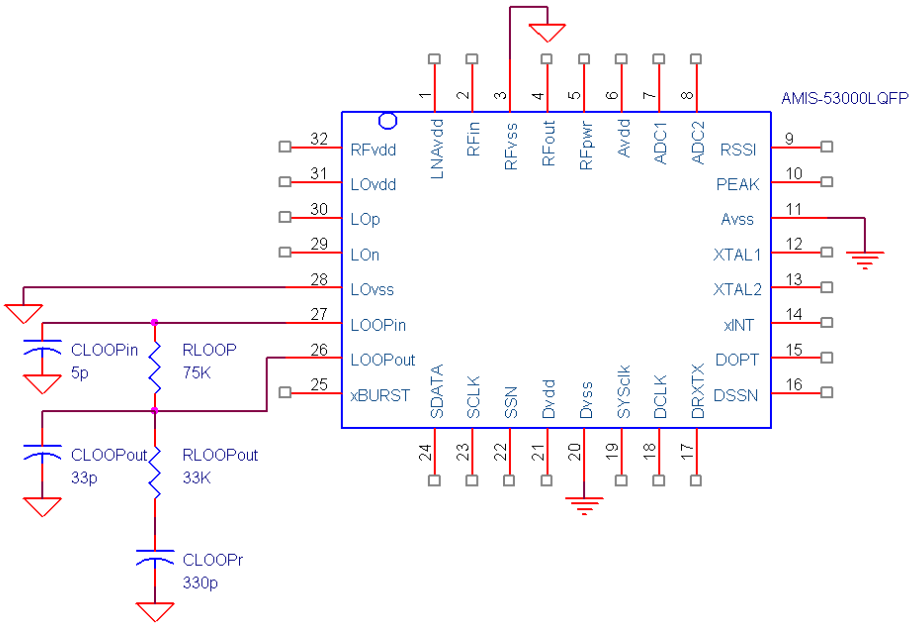


Figure 6: Optional External Loop Filter Circuit

An internal 10kHz oscillator provides timing for functions; Sniff Mode, Burst transmit and housekeeping, when the AMIS-53000 is in its lowest power mode (idle/standby). This oscillator requires no external components. The 10kHz oscillator's internal trim capacitor is trimmed by 8 bits of trim control in a self calibration. Once the trim is set, the oscillator frequency will be accurate to within two percent over specified voltages and temperatures.

5.2 Receiver

The AMIS-53000 has a single channel receiver. The LNA for the receiver input requires a DC connection to ground on the input (must not be an RF ground connection). The LNA for the receiver input requires a DC connection to RFVDD on the output. These connections are supplied through inductors becoming part of the matching circuit for the receiver input.

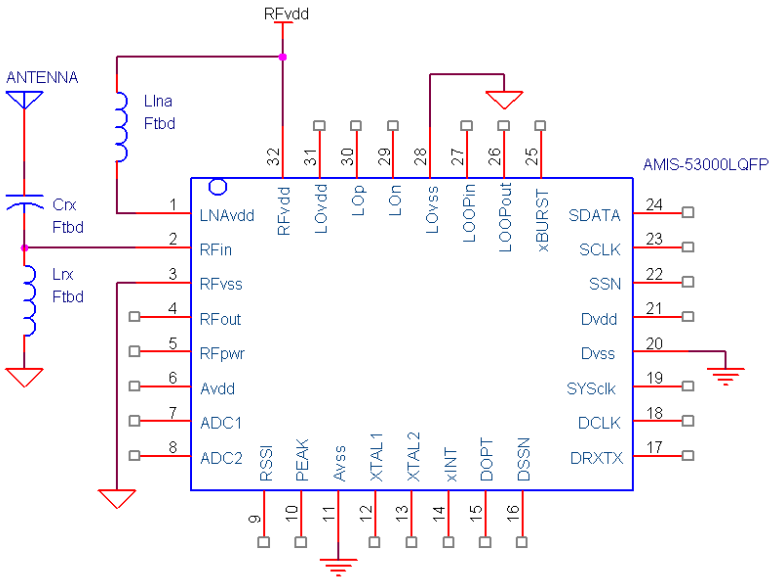
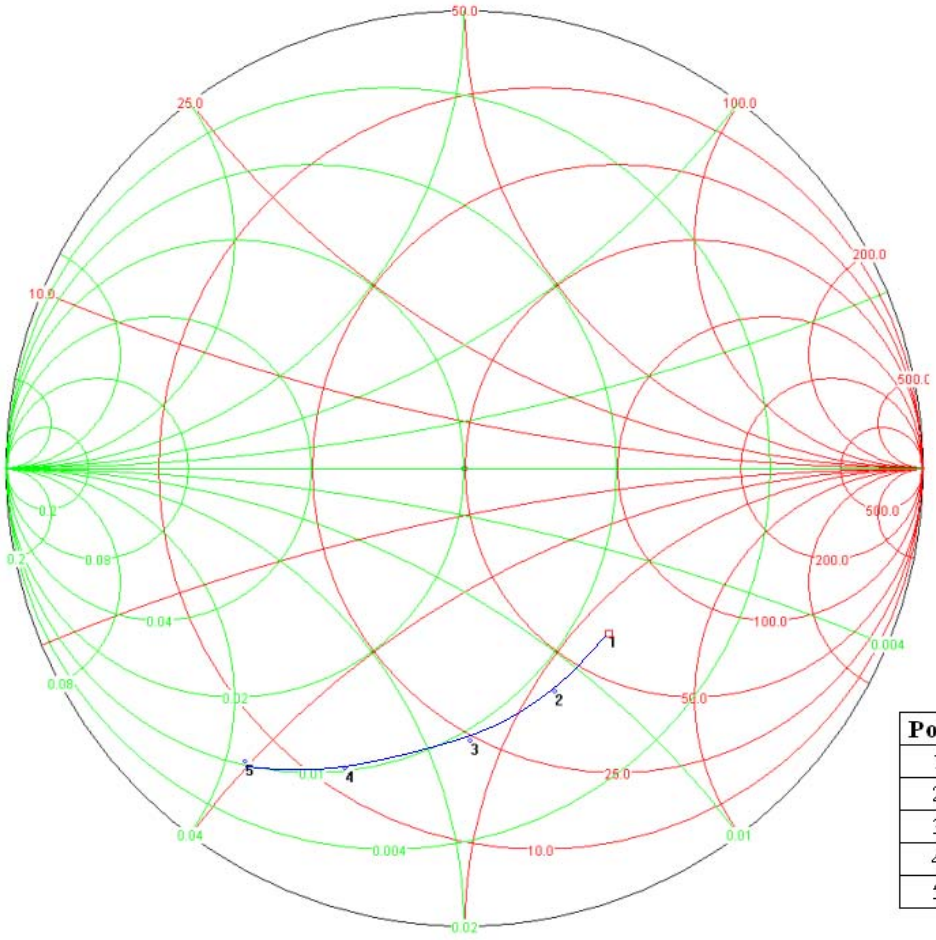


Figure 7: Receiver Input Matching Circuit

5.2.1. Receiver Low Noise Amplifier (LNA)

The receiver input of the AMIS-53000 is a single ended input and single ended output device. The input is matched to 50Ω using an external matching network, which provides a DC path to ground for biasing the receiver's LNA. The output of the LNA is tuned to the desired operating frequency using an external inductor and on-chip capacitor. The inductor is also provides the LNA with DC supply voltage. On-chip tuning capacitors are binary weighted and digitally controlled.

The internal input capacitance is 1.2pF to 4pF. With this capacitance set to the mid value (register set to 0X80), the impedance of the receiver is shown in Figure 8. The internal output capacitance is 0.32pF to 0.912pF.



Point	R+-X	Freq.
1	64.25 –j60.25	300 MHz
2	41 –j55.2	436 MHz
3	24.45 –j44.8	600 MHz
4	12.5 –j32.4	800 MHz
5	6.95 –j24.6	900 MHz

Figure 8: RX Input Impedance

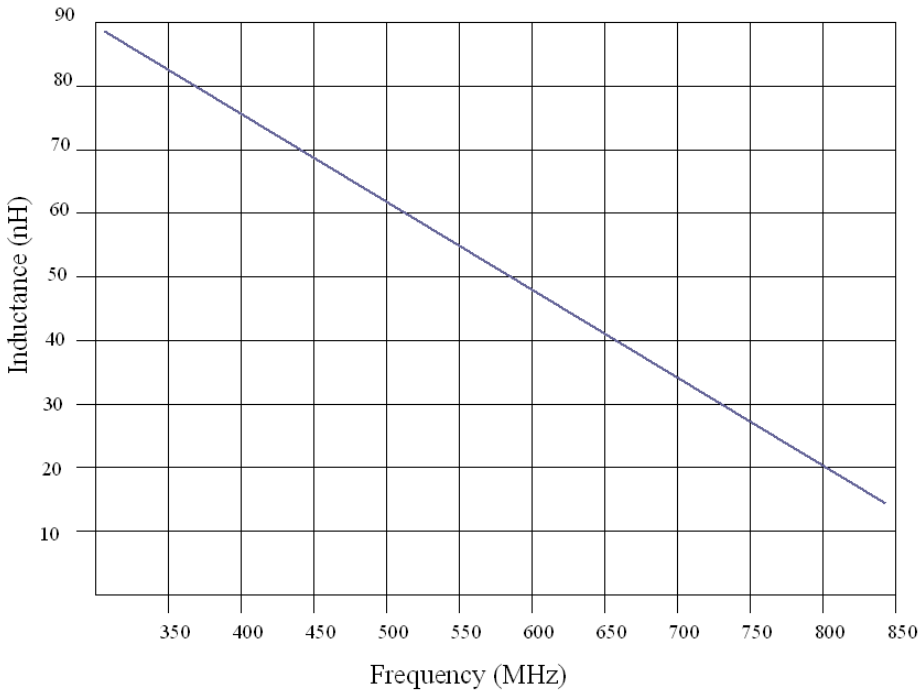


Figure 9: Receiver LNA Output Inductor Selection

5.2.2. IF Filter

A passive poly-phase filter and active filtering are used in the AMIS-53000 for frequency selectivity and rejection of the image frequency. It is designed to provide an optimal image rejection of 50dB at 500kHz.

5.2.3. Data Filter

The OOK low-pass data filter is used for additional post-detection signal filtering in accordance with the OOK signal data rate (1.2, 1.8, 2.4, 4.8, 7.2, 9.6, 14.4, 19.2kHz). The RSSI buffer is used to drive the RSSI signal off chip for external monitoring, and can also be internally configured for monitoring other signals such as the analog temp sense voltage or bandgap voltage.

5.3 Transmitter

The AMIS-53000 transmitter is a two-stage output amplifier. When both stages are selected, the highest output power at frequencies from 300MHz to 928MHz is +15dBm. When only one stage is used, the AMIS-53000 can output up to 0dBm with better power efficiency than when outputting the same power level with both stages. The voltage output level on the RFPWR pin controls the RF output power level of the AMIS-53000. A DC connection must be made between the RFOUT pin and the RFPWR pin. The non-linear output of the AMIS-53000 may require external components to match to a load and to reduce the spurious harmonics.

The output impedance of the AMIS-53000 can be matched to the impedance of an external load, using the spreadsheet AMIS-53RFMATCH.xls provided by AMIS. This spreadsheet is explained in the application note, AMIS-52X00 Antenna Impedance Matching Considerations. The goal of the transmit output matching with this spreadsheet is to optimize the output power while reducing the harmonic power.

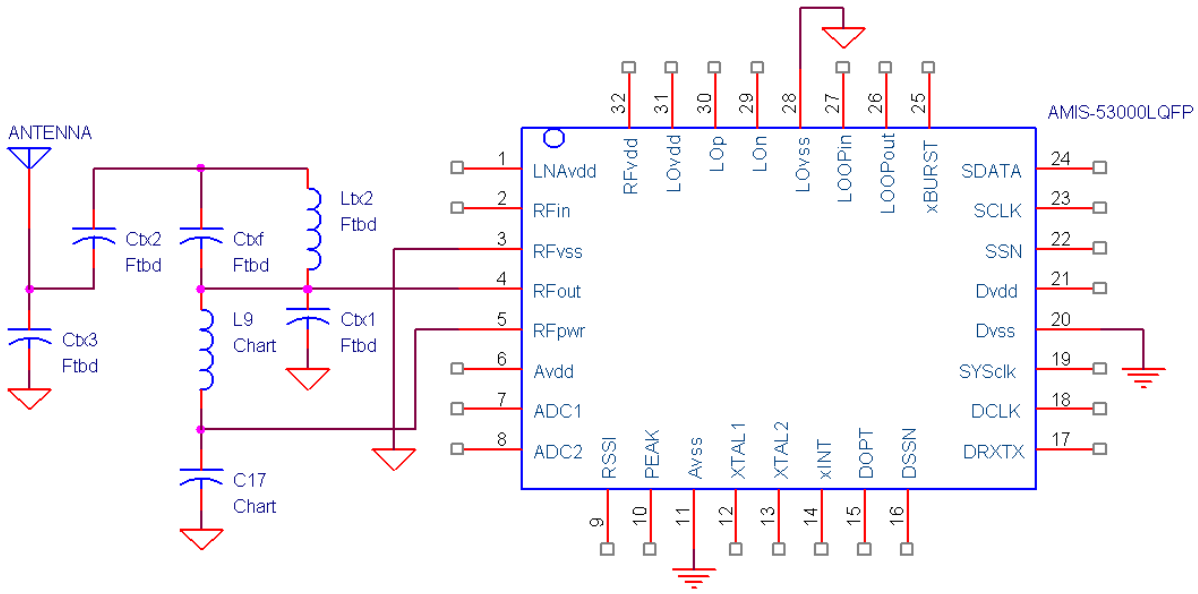


Figure 10: Transmitter Output Matching Circuit

5.4 Single Antenna Option

The AMIS-53000 is designed such that when the transmitter is off or the receiver is off, the pins are grounded. This provides a known impedance for the off port (transmit or receive) in combining the receiver and the transmitter to a single antenna.

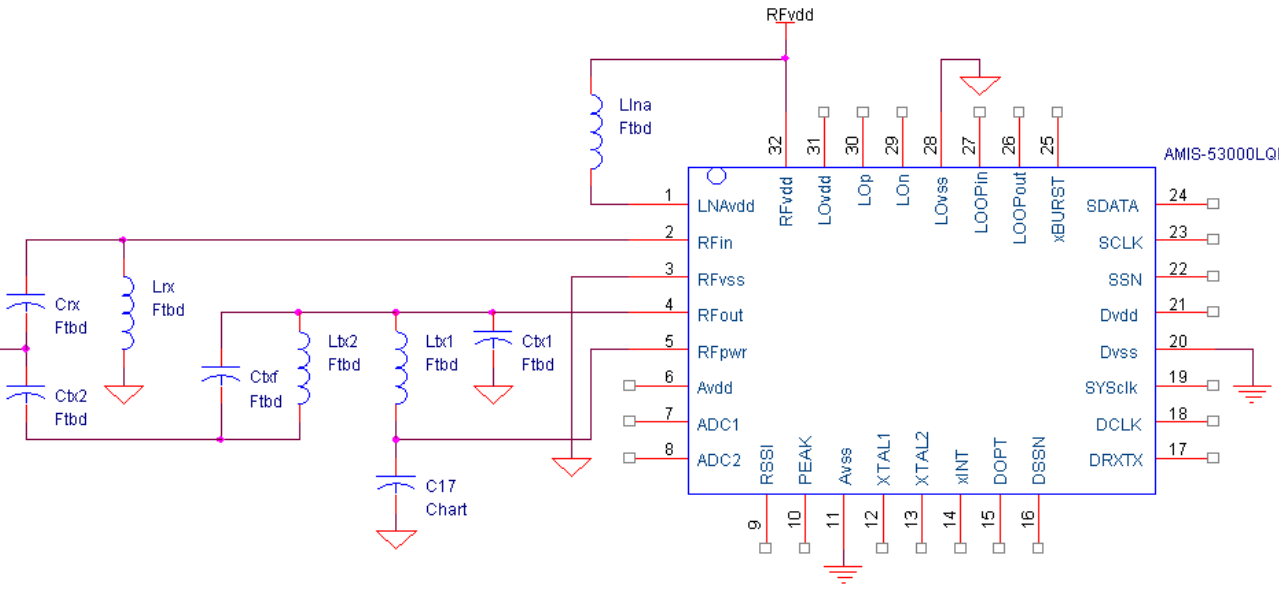


Figure 11: Single Antenna Port T/R Matching Circuit

5.5 Peak

The AMIS-53000 has three modes for slicing the received signal to recover the data. One method is to set a threshold value that is fixed and to which the receiver compares the recovered signal. The other two methods have the AMIS-53000 automatically setting a threshold level to which the receiver compares the recovered signal. Both of these automatic threshold methods require an external capacitor on the PEAK pin to operate.

In the averaging method, the AMIS-53000 simply adds a low pass filter with a cutoff frequency set below the data rate filter setting. This second filter extracts an average RSSI level as the data slice threshold. The capacitor on the PEAK pin sets the time constant (corner frequency) for this filter. A typical capacitor value would allow the average level to settle to 95 percent of the RSSI level in 2 bit intervals (remember that Manchester encoding may have transitions twice the data rate). The average threshold method will have chatter before a signal is received and after the signal ends which the external host/controller must be able to handle.

In the peak method the AMIS-53000 uses a peak detector to find the maximum input signal level and then sets the threshold 6dB lower than that level. The external peak capacitor is used to bleed or discharge the peak voltage in the circuit. The voltage swing on the RSSI for a typical 12dB signal to noise ratio at 10^{-3} BER is 240mV. The capacitor value should not change the voltage by more than this 240mV during a string of zeros. The value is dependent on the number of zeros that are allowed in the chosen data protocol, NRZ or Manchester encoded.

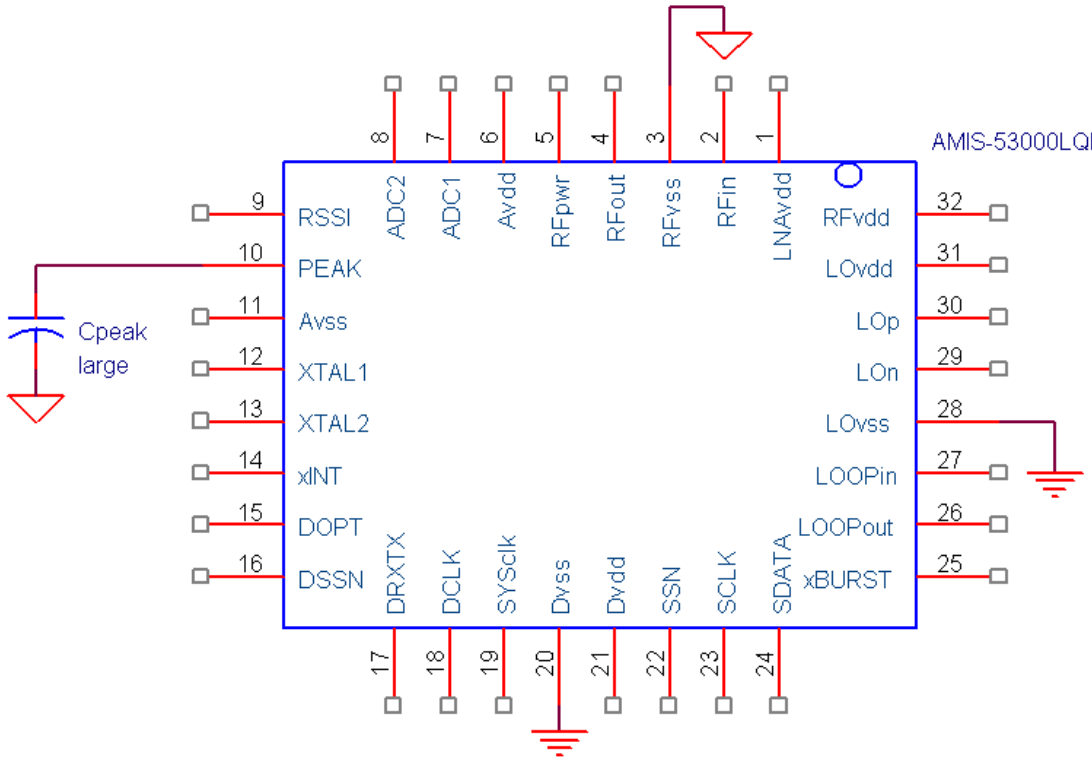


Figure 12: Peak Capacitance Circuit

5.6 ADC

The ADC is a successive approximation analog to digital converter, using an internal 8 bit DAC as the reference. The ADC data for the selected input channel(s) will be stored in the associated register, allowing for external access to the conversion data through the serial interface. Conversion speed is register selectable up to 128kS/s. Commands in the control register allow for single or continuous operation of the ADC.

A voltage regulator generates the 2.0V reference for the ADC and DAC based upon an internal bandgap voltage source. The ADC has six inputs, two of which are available to the designer for use in their application.

5.7 Control Interface Serial Bus

The AMIS-53000 uses a 3-wire or 2-wire I^2C interface to communicate with the AMIS-53000 internal registers. The AMIS-53000 will automatically determine which interface to use by determining the states of the three lines; SDATA, SCLK and SSN (the interface is set when the external host/controller writes the first data to the AMIS-53000). Once the AMIS-53000 has determined the type of interface, it will continue with that configuration until power is removed from the part or the part is reset.

I^2C: If SSN is high and an I^2C start bit is detected, I^2C mode is enabled.

SPI: If SSN is low, and a negative edge on SCLK detected, SPI mode is enabled.

The AMIS-53000 is designed to conform to the Philip Semiconductor I^2C standard with the AMIS-53000 as the slave device.

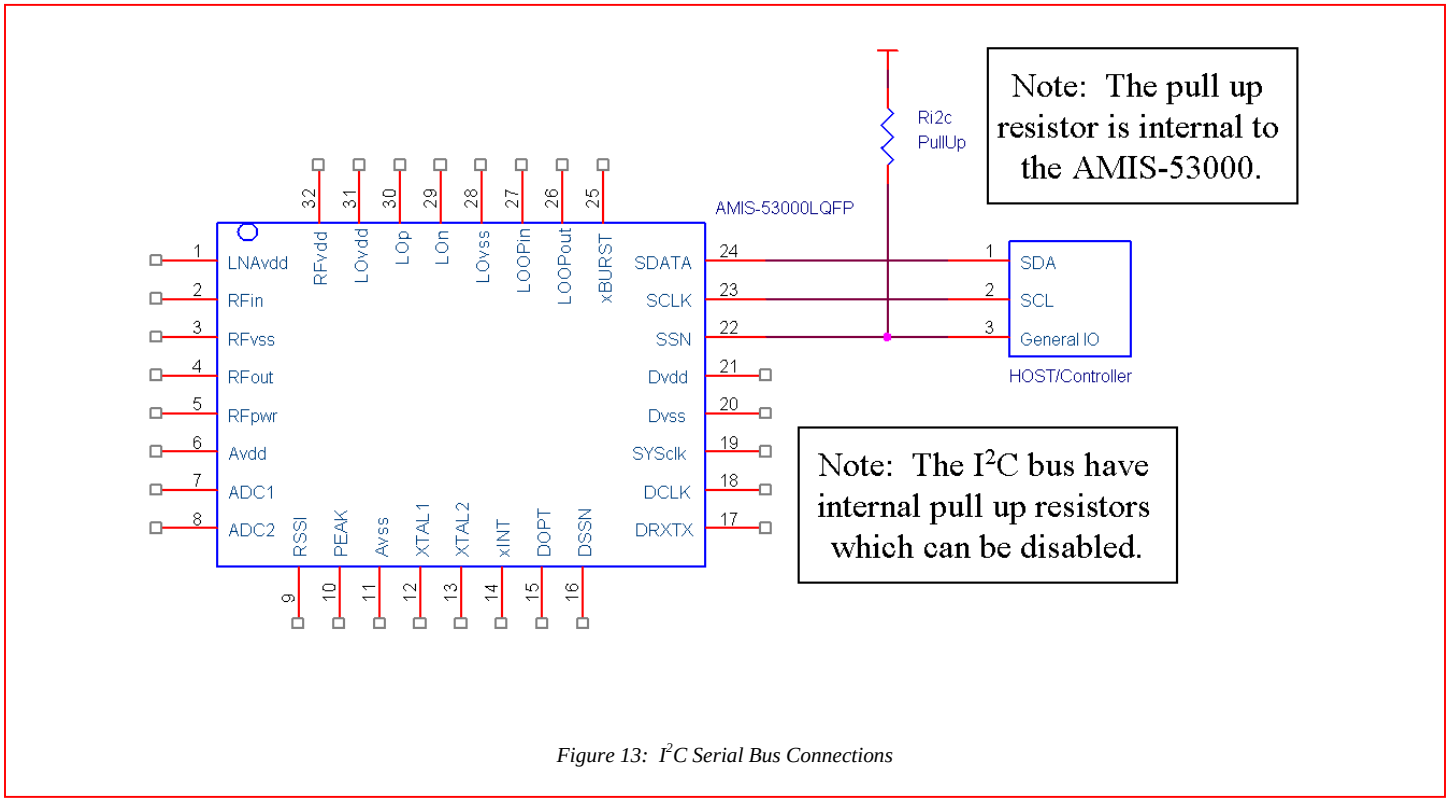
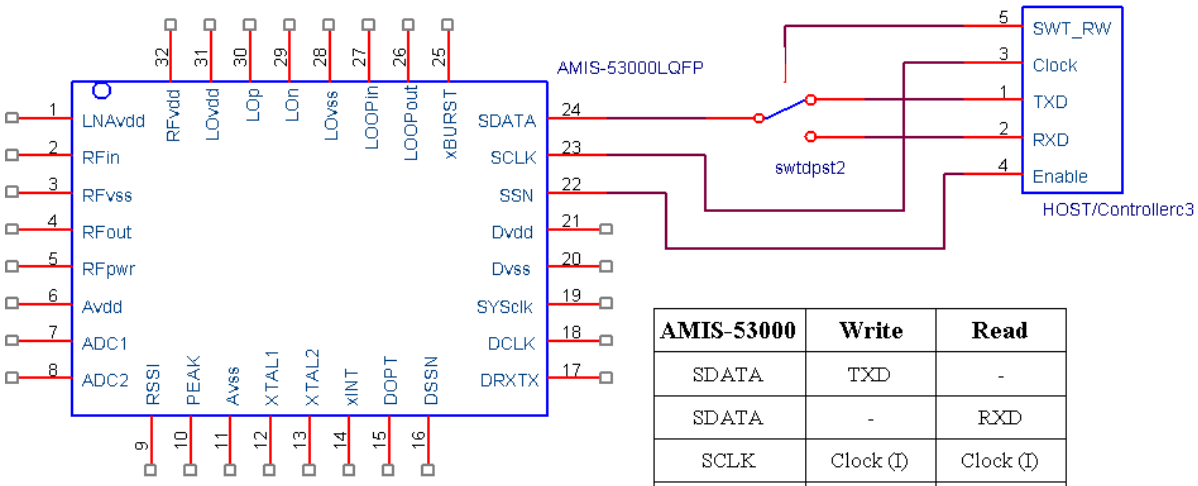


Figure 13: I^2C Serial Bus Connections



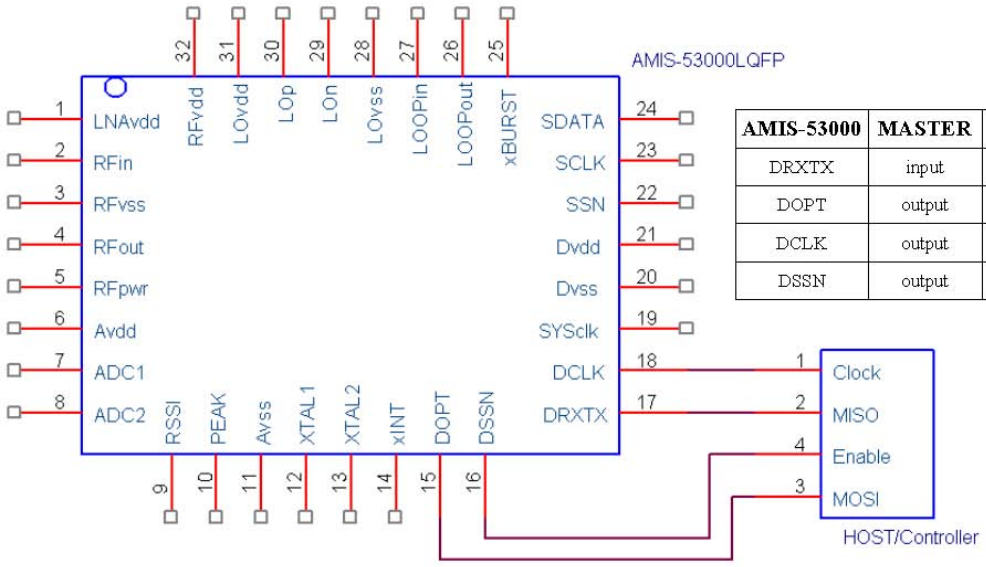
AMIS-53000	Write	Read
SDATA	TXD	-
SDATA	-	RXD
SCLK	Clock (I)	Clock (I)
SSN	Enable (I)	Enable (I)

Figure 14: 3-Wire Control Bus Connections

5.8 TX/RX Data Interface Serial Bus

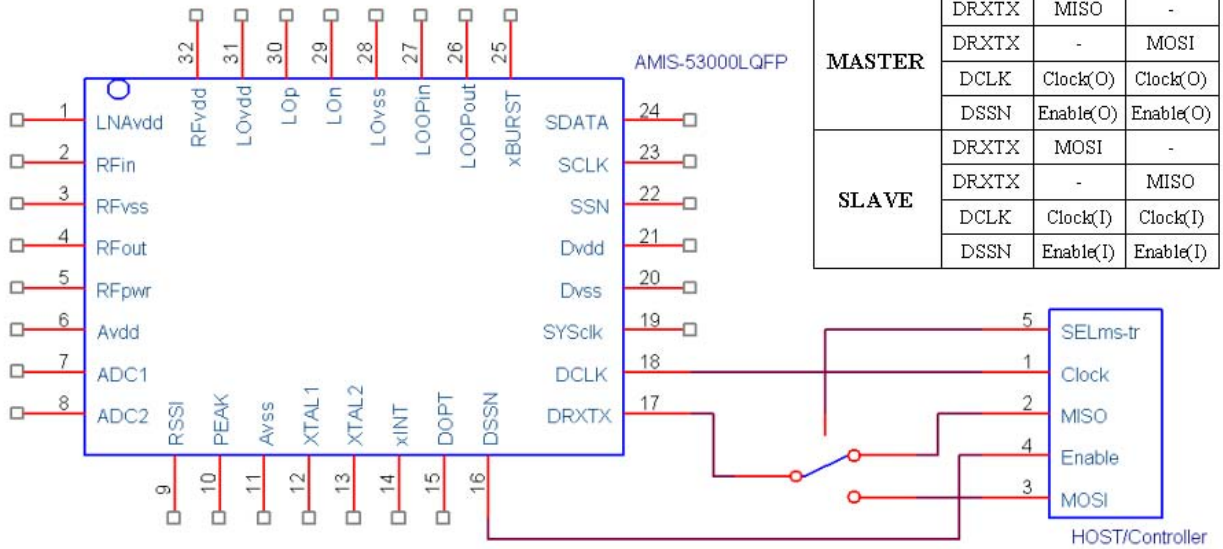
The AMIS-53000 uses a 3-wire or 4-wire SPI serial data interface to transfer data between the external host controller and the AMIS-53000. The interface is selected by writing to a register in the AMIS-53000. The DOPT line is undefined in the 3-wire interface.

The 4-wire interface of the AMIS-53000 is designed to be compatible with the definition of a standard SPI interface. The AMIS-53000 can be a slave or master device. The status of the AMIS-53000, master or slave, and the interface mode, read or write, determine the definition of the DRXTX and DOPT pin's as outputs or inputs.



AMIS-53000	MASTER	SLAVE
DRXTX	input	output
DOPT	output	input
DCLK	output	input
DSSN	output	input

Figure 15: SPI Compatible Serial Data Interface



AMIS53000	Ports	Write	Read
MASTER	DRXTX	MISO	-
	DRXTX	-	MOSI
	DCLK	Clock(O)	Clock(O)
	DSSN	Enable(O)	Enable(O)
SLAVE	DRXTX	MOSI	-
	DRXTX	-	MISO
	DCLK	Clock(I)	Clock(I)
	DSSN	Enable(I)	Enable(I)

Figure 16: 3-Wire Serial Data Interface

5.9 System Clock

The system clock can provide a clock to the external host controller. The clock can be divided down from the 24MHz crystal frequency of the AMIS-53000. When a design desires to use the system clock as the clock to an external host/controller, the system clock can be output under the following:

- Will be output in RX or TX, unless the output is off in general options B (Bit 1:0).
- The output will start back up in idle mode after a packet is received.
- The output will start back up in housekeeping if wake up external host/controller is enabled in housekeeping configuration (Bit 6).

Table 10: System Clock Control

Mode	Control	Bits	Outputs	Comments
	0X0D General Options B	1:0	Frequency: 12, 6, 3MHz or off	
RX				
TX				
Standby	General Options A	2:1	POR state: standby, idle, RX, TX	
		0	Output in standby	
Idle	Idle Config	4:3	Clock cycles before stop	

5.10 Power and Grounds

The AMIS-53000 has four different power inputs and two different grounds. This allows the design of the AMIS-53000 in an application to separate RF power from the analog and digital power. The same applies to the grounds, where a separate ground plane for the RF grounds can reduce the amount of noise induced into the sensitive RF circuits.

5.11 Design Suggestions

The following schematic and layout suggests at least one way to create a printed circuit board for applications using the AMIS-53000.

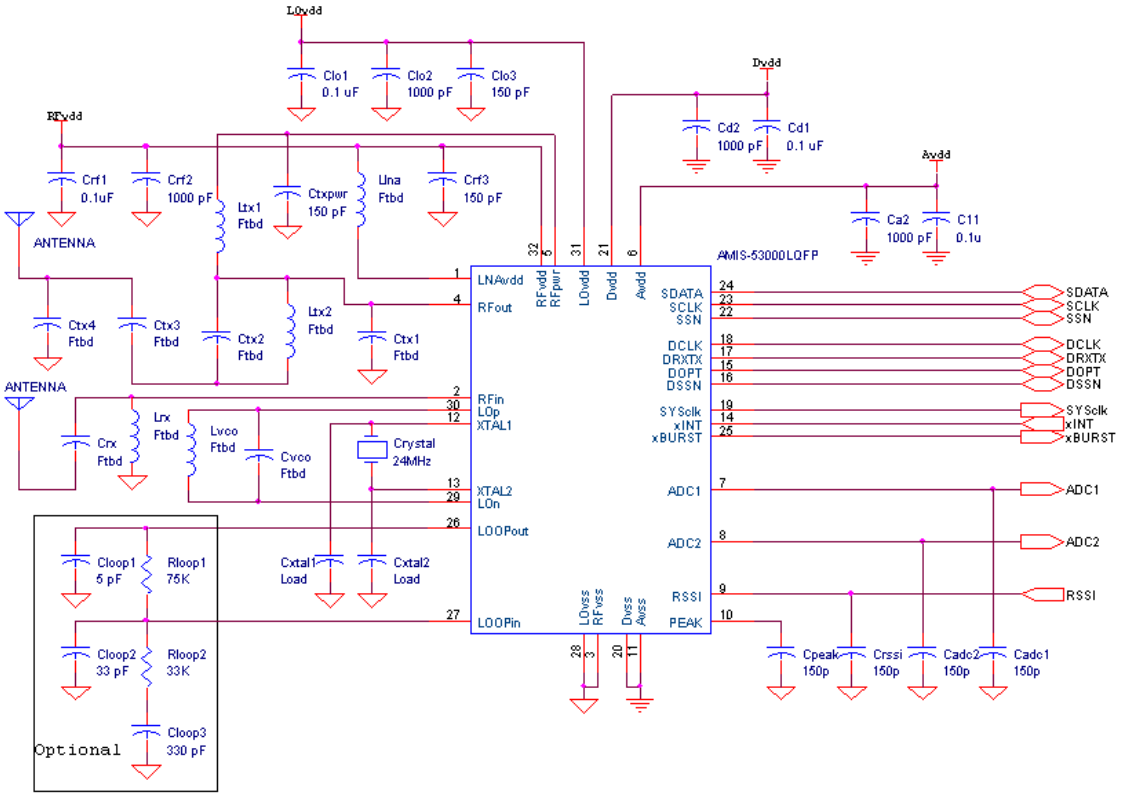


Figure 17: Typical Design Schematic

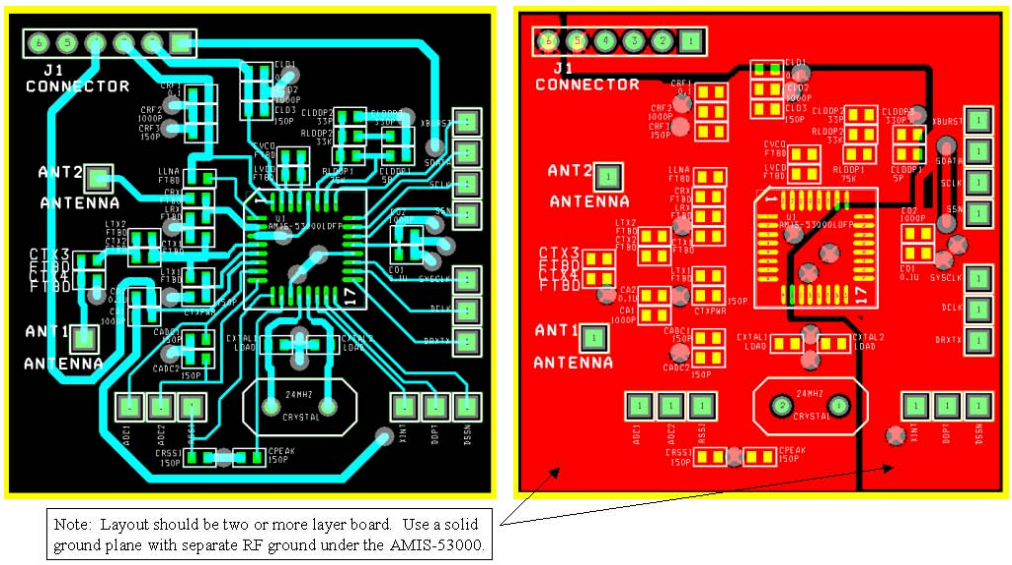


Figure 18: Typical Design Layout Suggestion

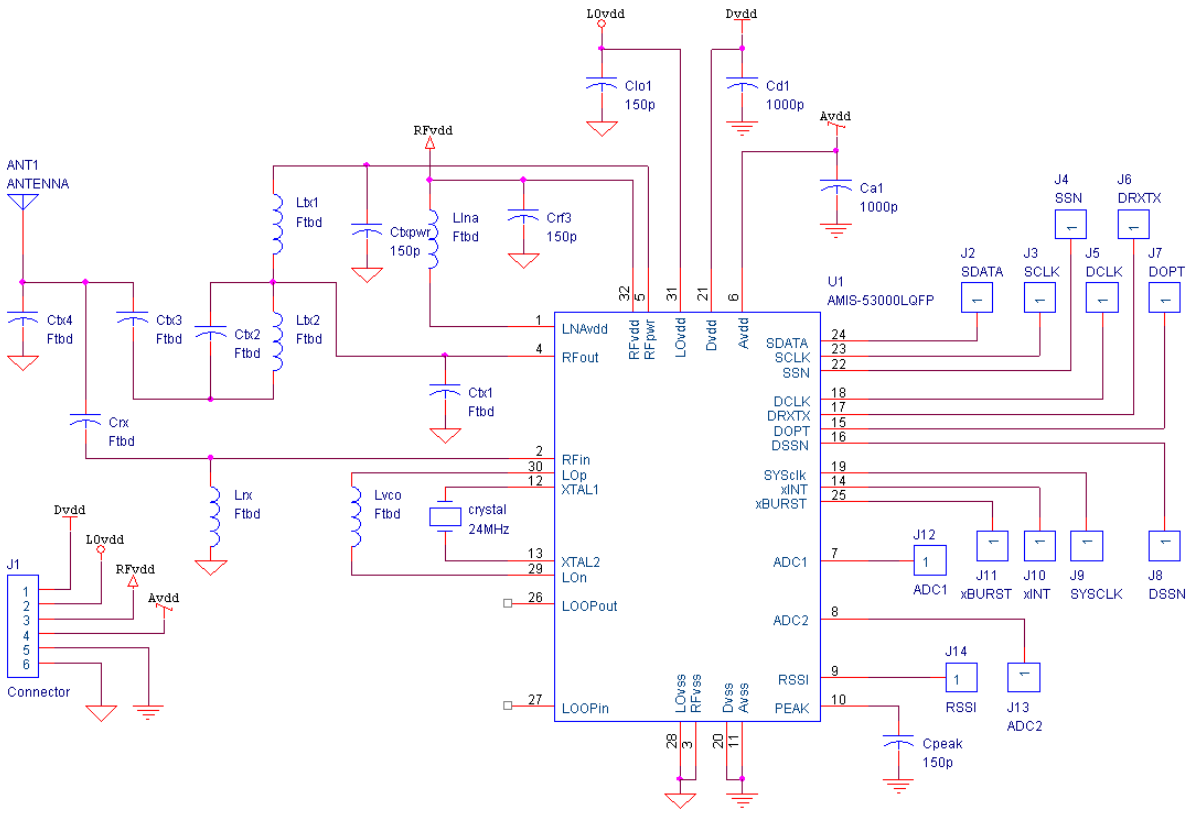


Figure 19: Minimum Design Schematic

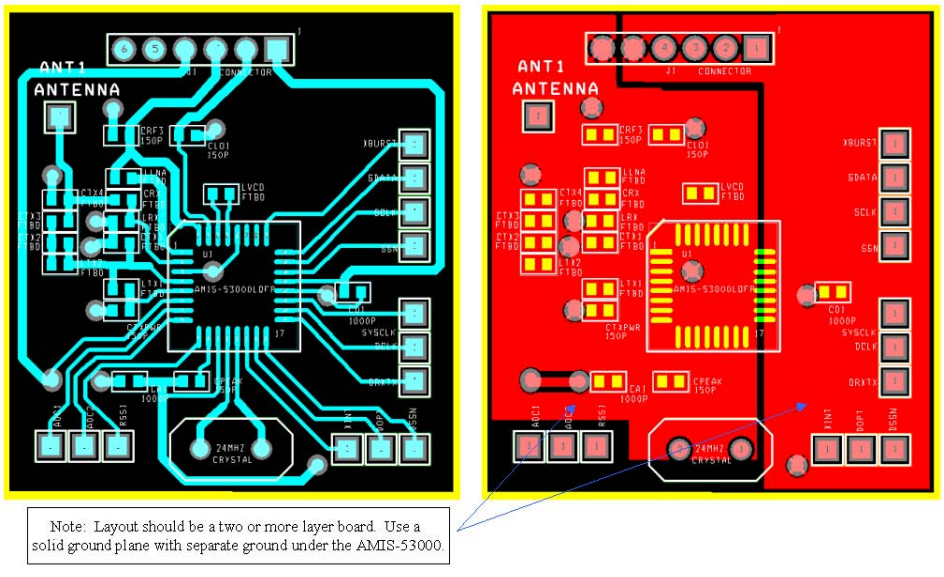


Figure 20: Minimum Design Layout Suggestion

6.0 User's Guide

This user's guide divides the control register description of the AMIS-53000 into functional areas; command register flow diagrams, frequency generation, receiver, transmitter, idle, data/control interfaces, Burst transmit, and MICS features.

6.1 Control Serial Interface Bus Description

Table 11: Control Interface Physical Configuration

Interface	Function	Clock		Data		Select	AMIS-53000
		Pin	Source	Output	Input		
I^2C	Control	SCLK	Master	SDATA	SDATA	None	Slave only
3-Wire	Control	SCLK	Master	SDATA	SDATA	SSN	Slave only

The AMIS-53000 employs two different control interfaces. Communication with the AMIS-53000 control registers is through either a 3-wire bus or through a 2-wire (with third line for control/status) I^2C compatible bus. The state of the control bus is detected by the AMIS-53000 at the first communication, I^2C or 3-wire, and is set in that function (3-wire or I^2C) as long as power remains applied to the part.

- 3-wire control communication bus
- I^2C control communication bus
- AMIS-53000 is always the slave

6.1.1. Control Interface Protocol

The AMIS-53000 control interface allows an external controller to write instructions to the registers of the AMIS-53000 and control the functions of the AMIS-53000. The external controller can also read the registers and status of the AMIS-53000. The control interface can be configured as a slave device in either a 2-wire I^2C interface bus or a 3-wire serial interface.

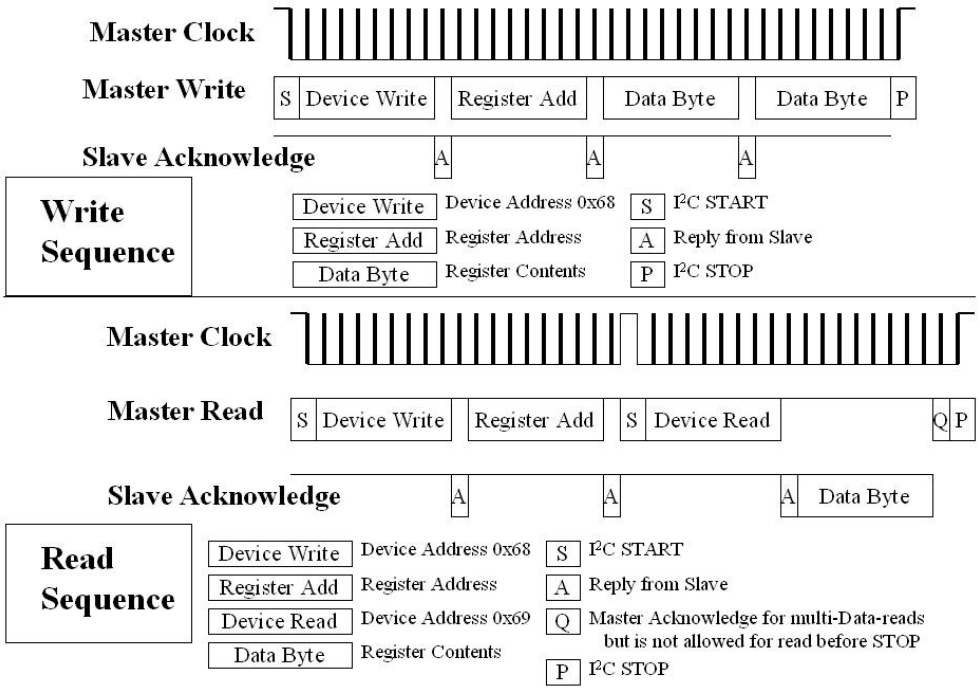


Figure 21: Control I^2C Protocol Format

Table 12: I²C Addressing

Address	Description
0110100X	AMIS-53000 I²C Address
01101000	AMIS-53000 Write Command
01101001	AMIS-53000 Read Command

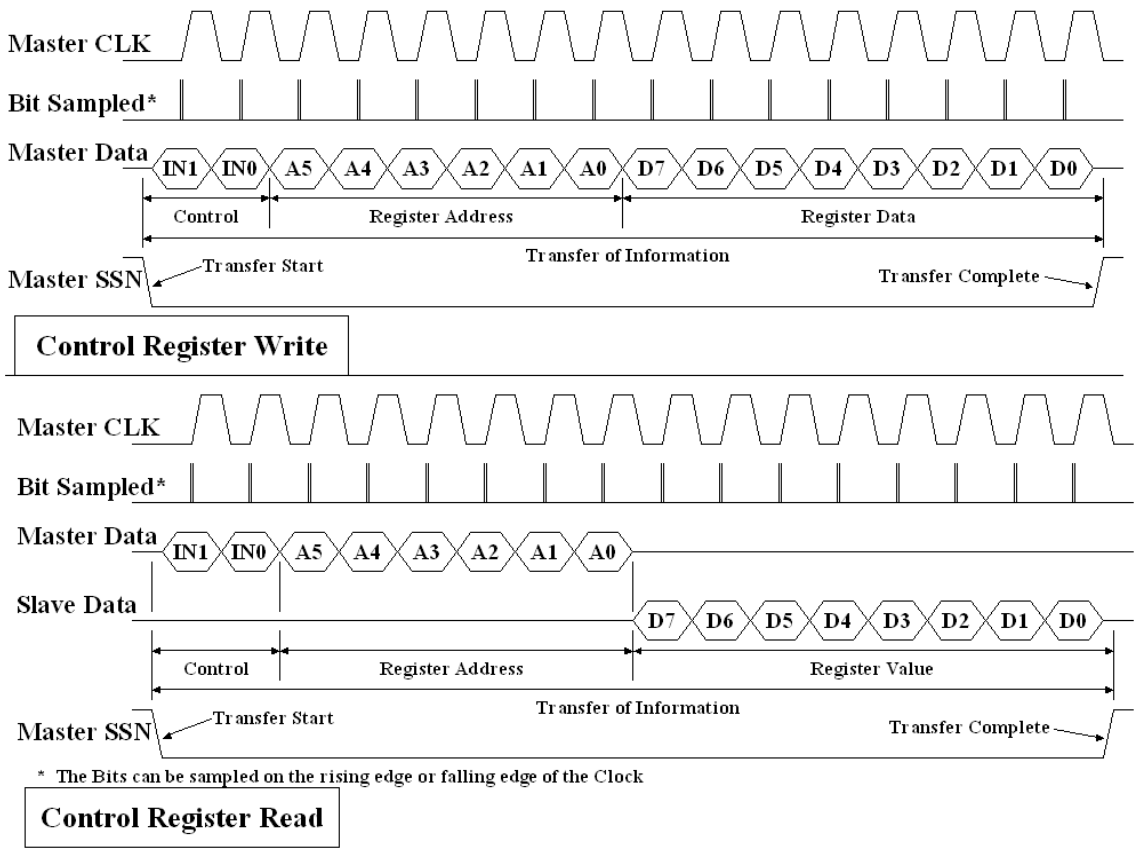


Figure 22: 3-Wire Control Protocol Format

Table 13: 3-Wire Control (IN1 and IN0)

Control Word Bits		Description
IN1	IN0	
0	0	Single Register Read
0	1	Single Register Write
1	0	Sequential Register Read
1	1	Sequential Register Write

- I²C device address:
  - 0x68 HEX for device write
  - 0x69 HEX for device read
- External controller can write registers

- External controller can read registers
- External controller can issue a immediate transmit via the xBURST input
- External controller can receive an interrupt (xINT) from the AMIS-53000

Setup registers descriptions:

I²C/3-wire select- First write to the interface sets the type of interface until AMIS-53000 is power cycled.

6.1.2. Serial Control Interface: Configuration

The AMIS-53000 can automatically detect the type of interface for the serial control bus. The interface pins are then given the definitions as shown in Table 14. The detection depends on the status of the AMIS-53000 pins as shown in Figure 23.

Table 14: Control Port Pin Definitions

Pin Name	I²C Mode	3-Wire Mode
SCLK	SCL	SCLK
SDATA	SDA	R/W controlled
SSN	Internal pull up	SSN

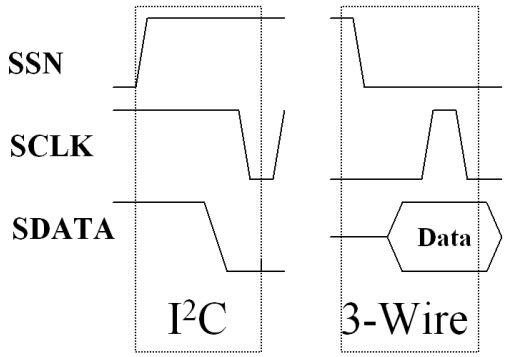


Figure 23: Control Interface Selection

Simply addressing the part with the desired protocol performs initial interface selection. After the first communication with the part, the selection is locked until power is removed from the device. The internal logic for determining which protocol to use on initial power up is as follows:

I²C: If SSN is high and an I²C start bit is detected, I²C mode is enabled.
3-wire: If SSN is low, and a negative edge on SCLK detected, 3-wire mode is enabled.

The internal pull ups on SCLK and SDATA can also be disabled for I²C applications using external pull ups.

Table 15: Control Interface Pull Up Control

Mode	SCLK, SDATA Pull Ups	SSN Pin Configuration
I²C	Controlled by bit 3 of the general options A register	Not used (internal pull up)
3-wire	Controlled by bit 3 of the general options A register	SSN: normal mode

6.1.3. 3-Wire Interface Mode

The AMIS-53000 is always the slave device.

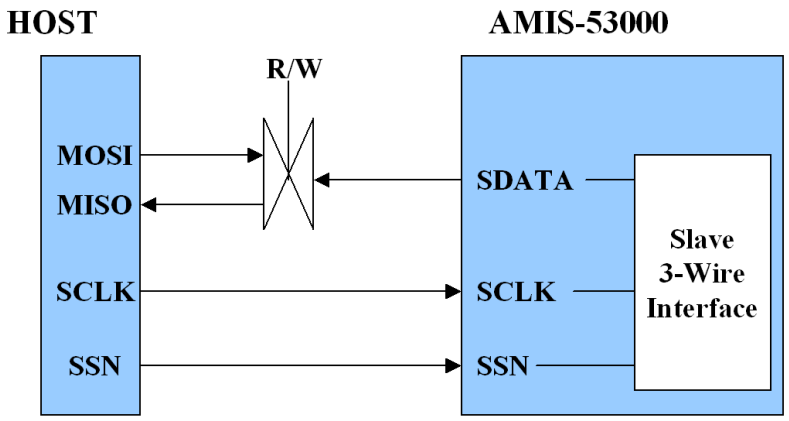


Figure 24: Master/Slave for Bi-Directional 3-Wire Mode

Figure 24 illustrates the connections between the master SPI port and the slave 3-wire port in the AMIS-53000.

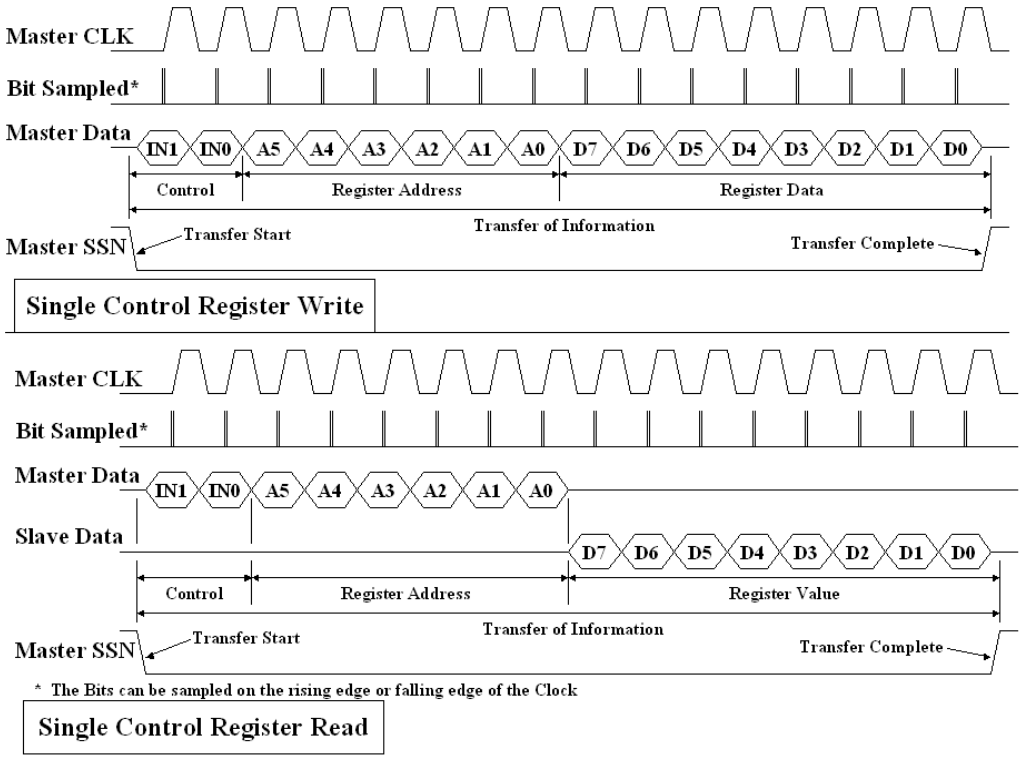


Figure 25: Single Control Register Read/Write Using the 3-Wire Interface

Figure 25 shows a single read or single write control data transfer. The operation starts with SSN transitioning low to indicate a start of transfer. The first two bits transferred are the instruction for the slave interface of the AMIS-53000, IN1 and IN0. Following the instruction are the six address bits to specify which address to read or write from. If the instruction is to write a register, the data to be written to address location A<5:0> is specified with the next 8 bits, D<7:0>. If the operation is a read, the slave output buffer is enabled at the end of the address bits, and the data bits D<7:0> are buffered out of the part MSB first.

For single read/write, the SSN line can remain active between successive read and write operations.

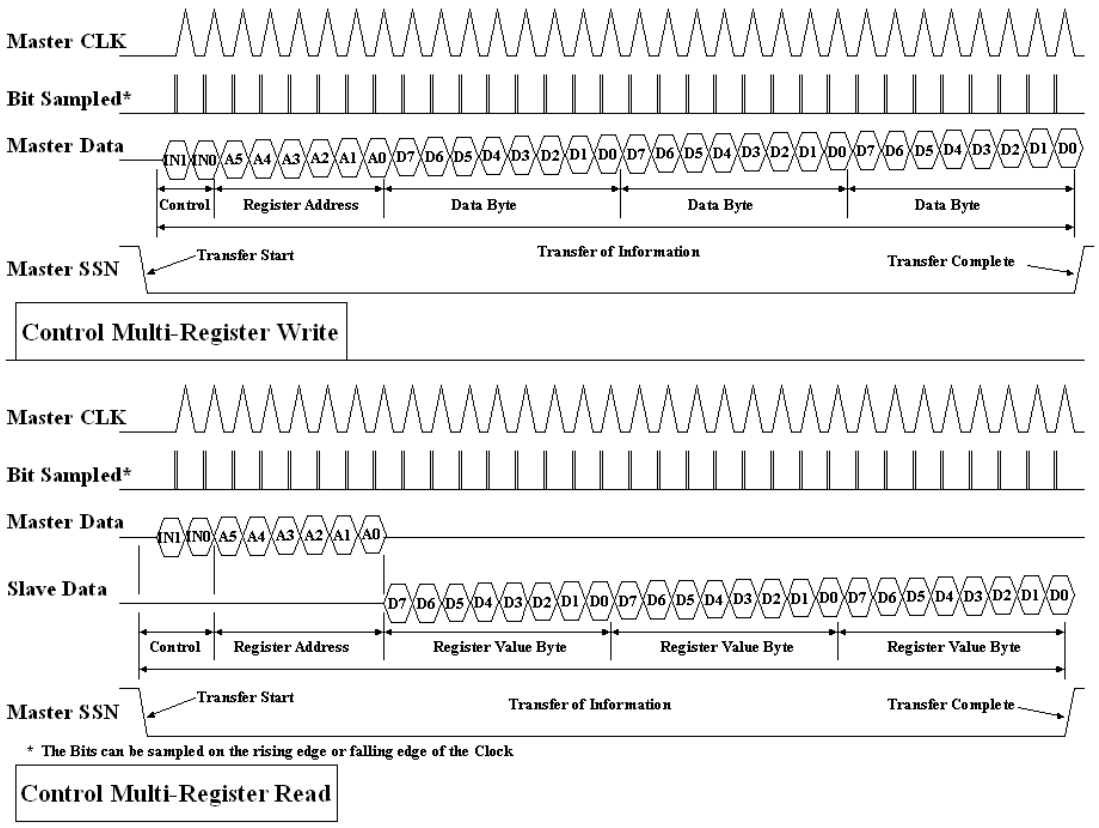


Figure 26: Sequential Control Register Read/Write Using the 3-Wire Interface

Figure 26 is a diagram for sequential reads or sequential writes for 3-wire control data transfer. The format of the instruction and address is identical to that for a single read/write operation, with the address corresponding to the first register location to read or write. The first 8 bits of data transferred correspond to the address selected. The address is internally incremented after each data byte transferred. This task is most useful for writing to or reading from variables spanning over multiple address locations such as the fractional PLL word (registers 03-05).

The SSN line must be de-asserted at the completion of a sequential read/write in order for the slave SPI controller to correctly interpret the next 8 bits as a command and not data.

6.1.4. I^2C Interface

The I^2C interface for the AMIS-53000 is compatible with the Philip Semiconductor I^2C standard, with the AMIS-53000 as the slave device.

6.1.4.1. I2C Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 7-bits for the device address, and 1-bit for a read or write command. For the AMIS-53000, the device address is '0110100' binary. The last bit of the control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. Following the start condition, the AMIS-53000 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving its device address, the AMIS-53000 outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the AMIS-53000 will select a read or write operation.

6.1.4.2. Single Register Write

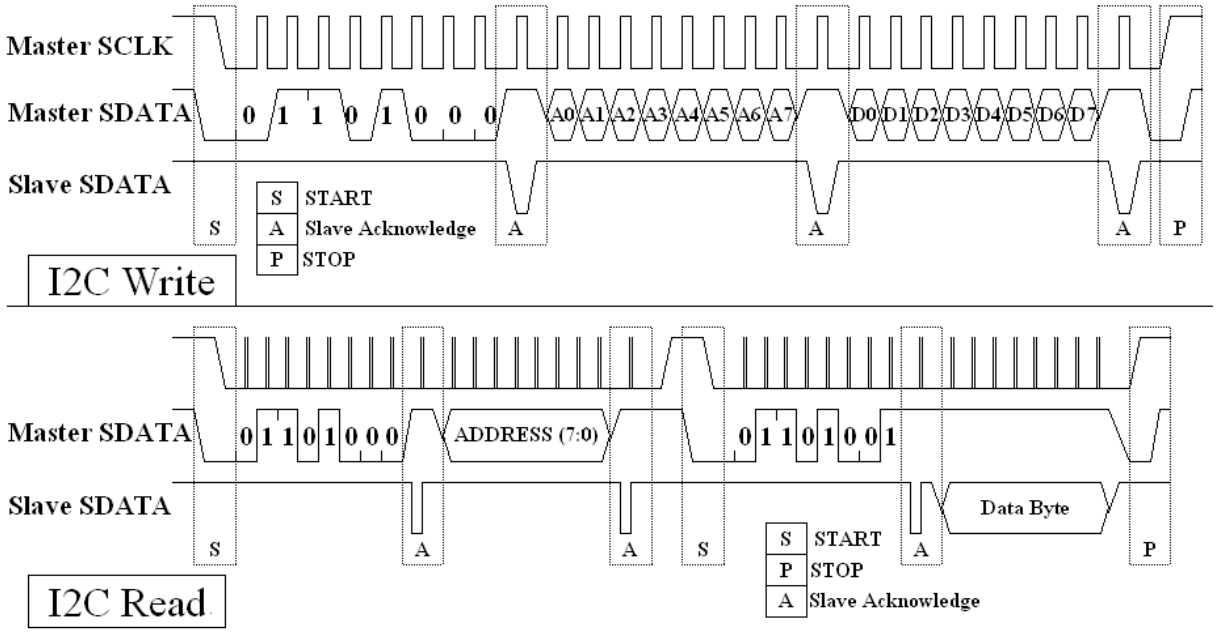


Figure 27: Single Control Data Read/Write with the I²C Interface

The master device issues the start condition, then issues the device address, and then issues the single R/W bit, a logic low state. This indicates to the addressed slave receiver that a byte with a register address will follow after the slave has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the register address to be written with data. After receiving another acknowledge signal from the AMIS-53000, the master device will transmit the data word to be written, and the AMIS-53000 will acknowledge again. The write cycle ends with the master generating a stop condition.

A similar approach is used to read a register value. The master device issues the start condition, then issues the device address, and then issues the single R/W bit, a logic low state. This indicates to the addressed slave receiver that a byte with a register address will follow after the slave has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the register address to be read. After receiving another acknowledge signal from the AMIS-53000, the master device will immediately follow with another start sequence, however, the R/W bit is now set high telling the slave device that the master wants the contents of the register (addressed with the write command) to be placed on the SDA bus line. After 8 bits of data are read by the master, the master does not acknowledge but sends the stop sequence.

6.1.4.3. Sequential Register Write

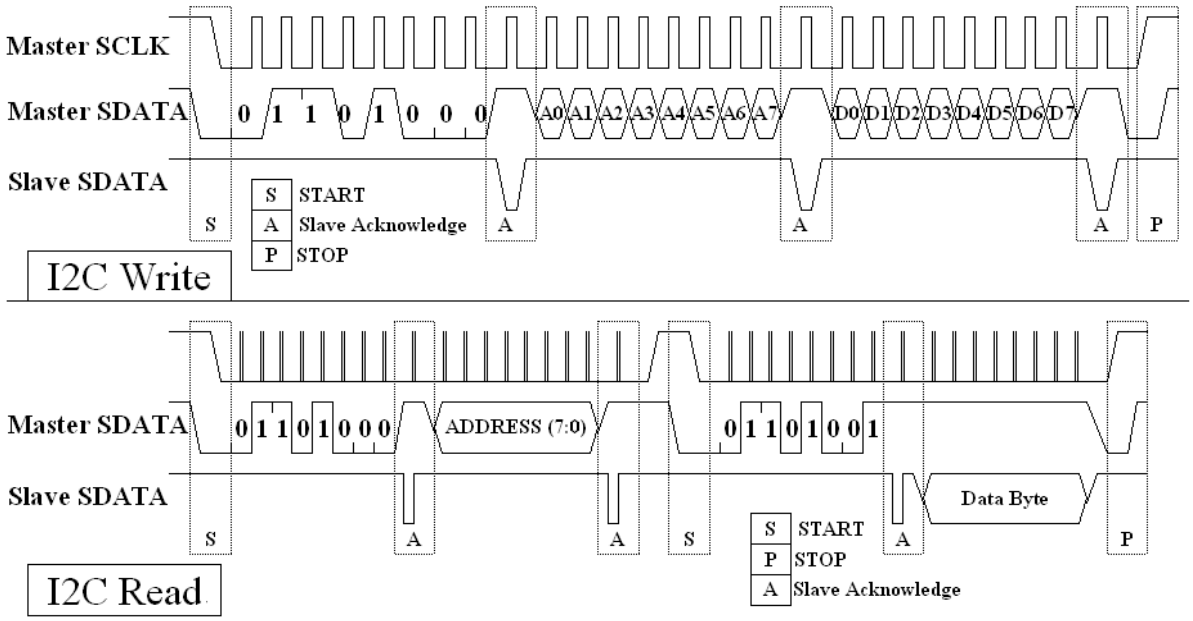


Figure 28: Sequential Control Data Read/Write with the I²C Interface

When setting the AMIS-53000 up for an application it sometimes is nice to write data to a number of registers one after the other. The write control byte, register address and first data byte are transmitted to the AMIS-53000 in the same way as in a byte write. However, instead of generating a stop condition, the master can continue to write register locations. Upon receipt of each word, the address is internally incremented by '1'. If the master should transmit more words than the AMIS-53000 has address locations, the address will roll over.

It is a similar approach to read a register value. The write control byte and register address are transmitted to the AMIS-53000 in the same way as in a byte write. After receiving another acknowledge signal from the AMIS-53000, the master device will immediately follow with another start sequence, however, the R/W bit is now set high telling the slave device that the master wants the contents of the register (addressed with the write command) to be placed on the SDA bus line. After the 8 bits are read by the master, the master acknowledges the reception. The AMIS-53000 will increment the register address and continue to output register values. After the last register value is received by the master, the master does not respond with an acknowledge but sends the stop sequence.

6.1.4.4. Current Address Read

The internal address counter maintains the last address addressed, incremented by '1'. If the last instruction received was to access register N, the current address read operation will read the contents from register N+1. The timing for the current address read is to send a start bit followed by the 7-bit device address, with the R/W bit set to one. The slave will acknowledge, after which the 8-bit register contents will be transmitted. The master does not acknowledge the transmission, but does generate a stop bit.

6.1.4.5. Interface Options

Table 16: I²C Address Auto Increment

Register			Function
Number (HEX)	Name	Bits	
0X0C	General Options A	3	Disable the internal pull up resistors on SDATA and SSN lines
0X0D	General Options B	5,4	Select a clock rate for the interface when the AMIS-53000 is master
		3	Disable auto increment for I²C control interface register addressing

Additional interface options give the AMIS-53000 the flexibility to tailor the interface to specific requirements. These options are available in the interface options register, and can be stored into EE at board assembly to best suit the application.

6.1.4.6. Pull Up Disable

The AMIS-53000 includes built in pull up resistors for use with the I²C operation to reduce the overall system component count. The pull ups are asserted at POR until mode selection occurs. If mode is determined to be 3-wire, the pull ups are removed. If mode is determined to be I²C, this option bit determines whether the pull ups are to be removed.

6.2 Command Register

The AMIS-53000 contains a single 8-bit register that allows single writes to the register to place the AMIS-53000 into a desired mode. It is very important to remember that all registers associated with that mode must be preprogrammed for the single write to this register to operate correctly.

The command register allows the user application to issue a single register write to the AMIS-53000 to initiate the function listed in Table 17. When the function is started, the AMIS-53000 uses the register values associated with the function selected as the parameters of the function. These register values will be the default values or the values the user application has written to the registers before the function is called out in the command register.

Table 17: Command - 0X00 [0]

Bit		Command	Comment
[7:4]	[3:0]		
0000	0000	Standby	Put the part into standby
	0001	Receive	Put the part into receive mode
	0010	Transmit	Put the part into transmit mode
	0011	Idle	Put the part into idle mode
	0100	Idle Return	Use to return to idle after interrupt for HK or receive during sniff
	0101	Write EE	Write the content of the working registers into EE
	0110	Read EE	Read the contents of the EE
	0111	Calibrate QS Osc	Calibrates the Quick Start oscillator
	1000	Calibrate RC	Calibrates the 10kHz RC oscillator
	1001	Calibrate PLL	Calibrates the PLL
	1010	Calibrate LNA	Calibrates the LNA matching
	1011	ROM2Regs	Write the content of the ROM into the shadow registers
	1111	Global Reset	Resets the part completely
[7:6]	[5:0]		
01	XXXXXX 100000	Single ADC Conversion	Do an ADC one time on the channel selected loop filter output
11	XXXXXX 100000	Continuous ADC Conversions	Do an ADC on the channel selected continuously loop filter output

Standby is both a state for the transceiver, and a command given to the transceiver. The actual operation of standby mode can be either a low-power mode where all internal circuitry of the AMIS-53000 except for the interface will be disabled, or a clock-only mode where the crystal oscillator will be enabled to continue providing a system clock for an external microprocessor. A bit available in the general options A register allows selection of power-down or clock-only operation in standby mode.

Many of the instructions for the part are finite in duration and the end point of the task is controlled by the AMIS-53000, such as the calibration instructions. For these instructions, the AMIS-53000 will return to its standby mode at the completion of the task. The user may poll the Status/Flag 1 register busy bit to determine the completion of the calibration instruction. Other instructions such as receive or transmit are indefinite in length and user controlled. To return to the standby state, the AMIS-53000 waits for the standby instruction to end receive or transmit, at which point the transceiver will return to its standby state.

Note that there are two low-power modes for the AMIS-53000; standby and idle.

Standby allows the SYSCLK output
Idle is the very low power state without SYSCLK output

6.3 Functional Flow Diagrams

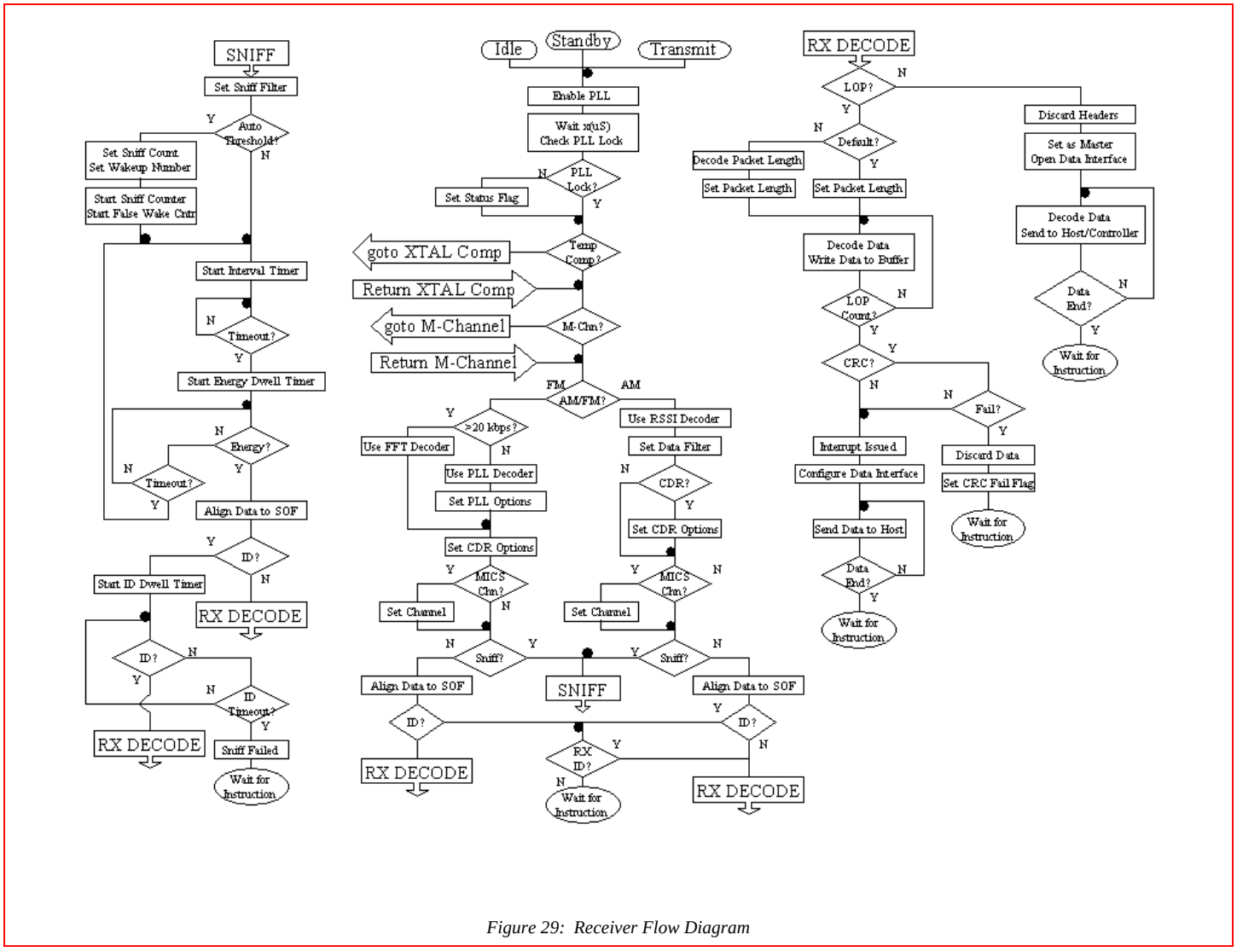


Figure 29: Receiver Flow Diagram

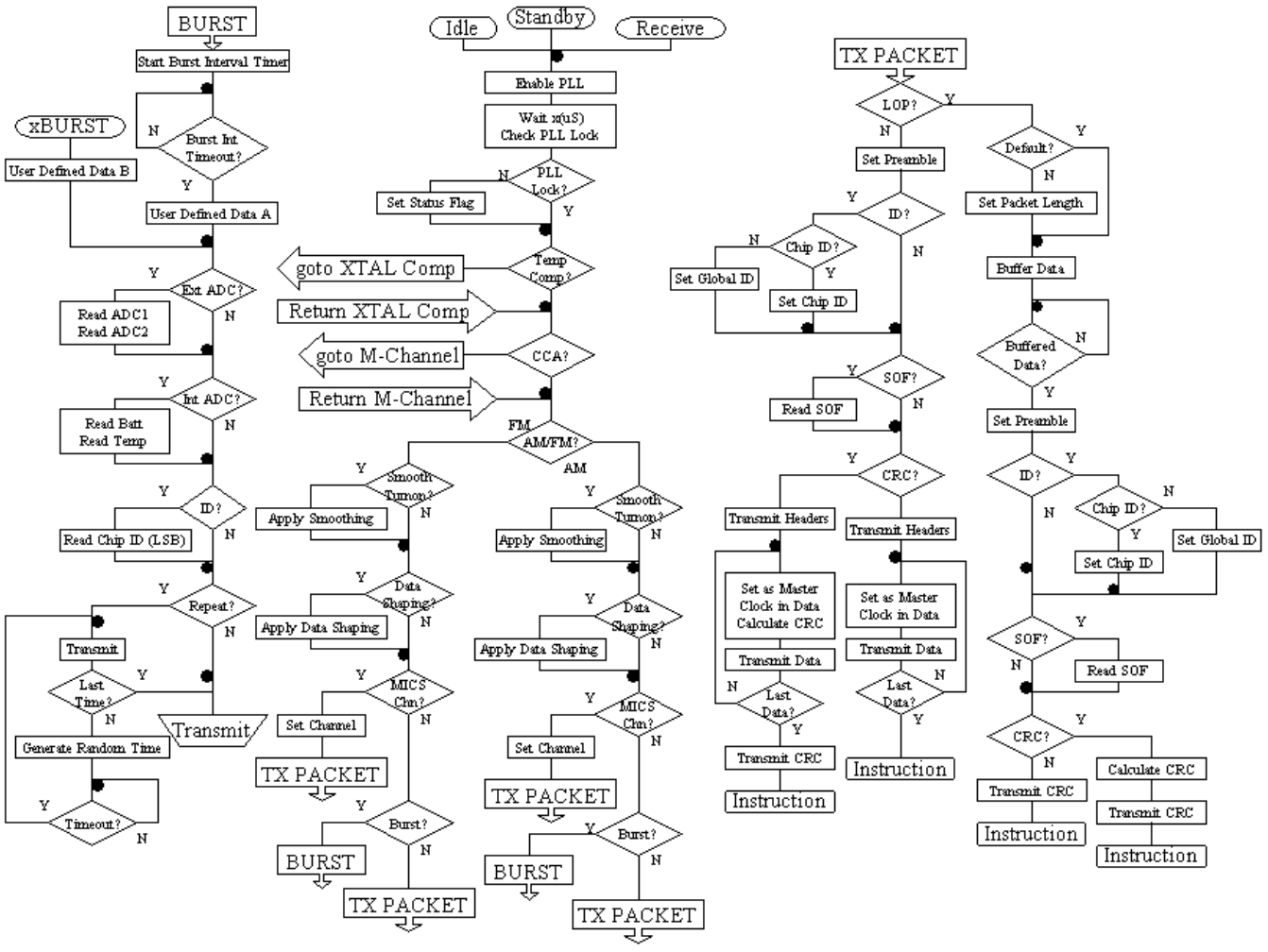


Figure 30: Transmit Flow Diagram

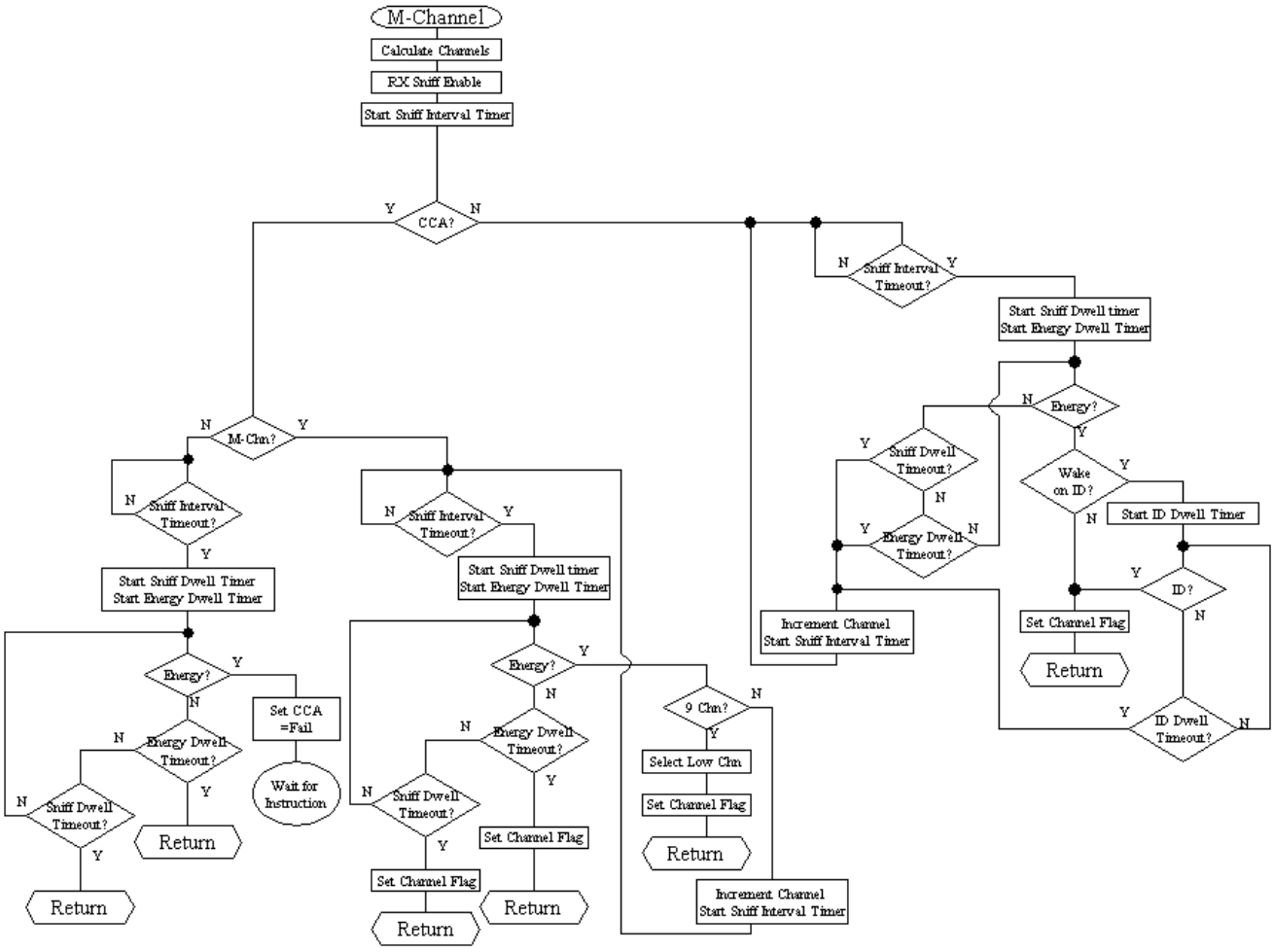


Figure 31: Multi-Channel TX/RX

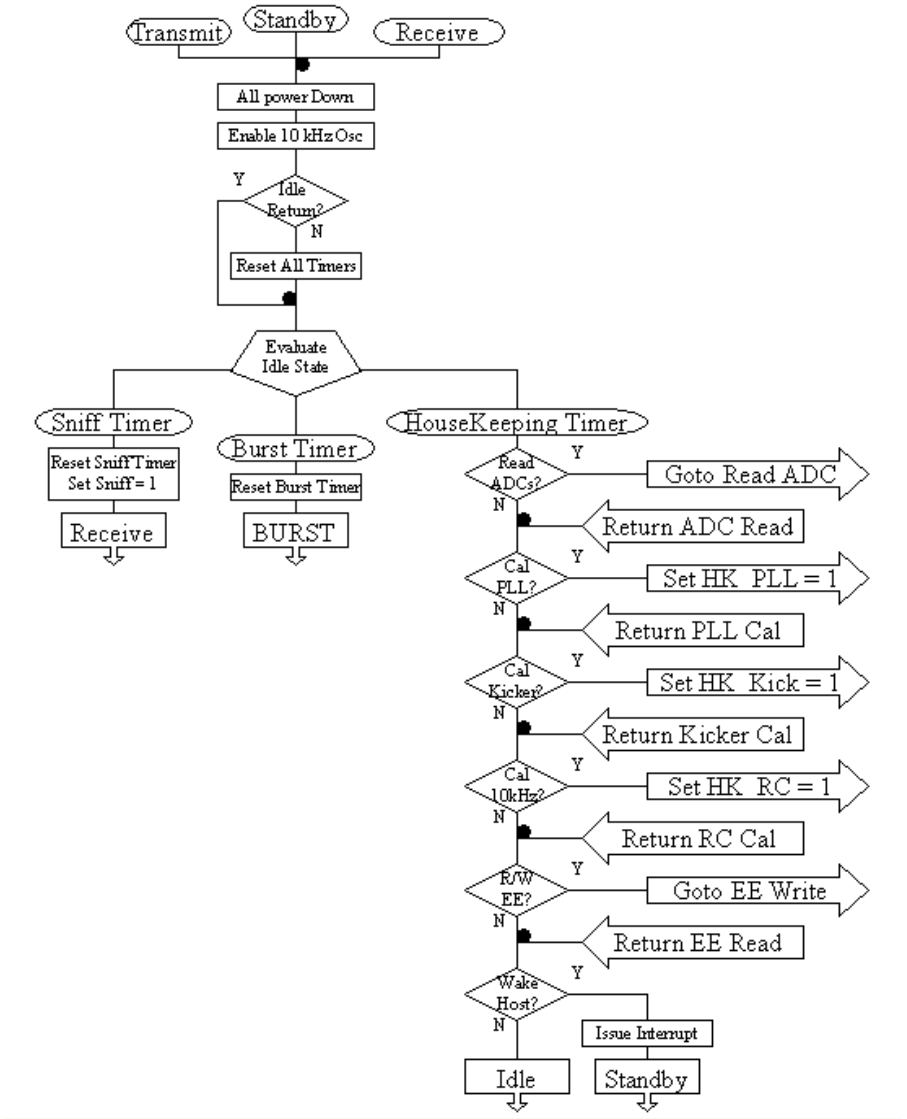


Figure 32: Idle State Flow Diagram

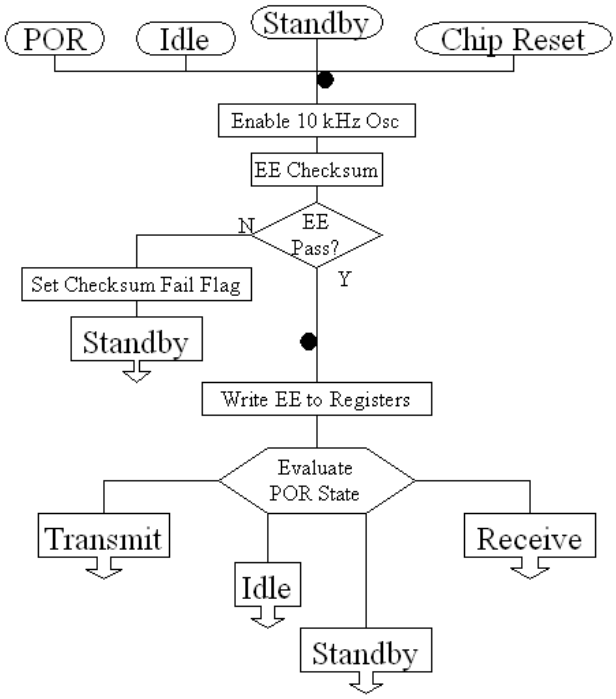


Figure 33: EE Flow Diagram

6.4 Frequency

The AMIS-53000 uses an internal PLL/VCO to generate the RF frequencies for both transmit and receive. Only one set of registers needs to be programmed to generate the TX frequency and to generate the LO frequency to produce the mixing frequency for converting the received signal to the low IF (about 500kHz). The AMIS-53000 can do a self-calibration, which will trim internal capacitance to tune the TX and RX frequencies. The AMIS-53000 needs to run the self-calibration (must be started by the external host/controller) at least once between startup and entering a command such as TX, RX, Sniff, etc.

6.4.1. Frequency Control

AMIS has developed an executable program (AMIS-53CALC.exe, available from AMIS, which generates the register values for the frequency divider and fractional word to produce a given frequency. First, the AMIS-53000 must have the correct LC for the desired frequency connected to the VCO pins. There is internal capacitance that is part of the capacitance for determining the value of the inductor. The following equation can be used to determine the approximate value of the LC components. Remember that the VCO is sensitive to the placement of the LC components - they should be placed as close to the AMIS-53000 as practical (even short traces add significant parasitics) and the traces to the components should be made symmetrical.

$$F_{vco} = \frac{1}{\sqrt{L_{tot} \cdot C_{tot}}} \frac{1}{2 \cdot \pi}$$

Where: Ltot and Ctot are the total inductance and capacitance respectively at the VCO pins. This includes the internal capacitance of approximately 2pF.

The RF PLL is a 24-bit Sigma Delta based fractional N synthesizer used to provide the LO signal for receive, and a direct RF output for transmit.

Setup registers descriptions:

RF Divider- The RF frequency of the receiver must be configured. This is done in two steps, one is setting the RF divider and the other is setting the fractional N word.

RF Frequency- Program the 3 register fractional N word.

Peak Deviation- When the data modulation is to be FSK, the 2 register peak deviation must also be set. The deviation should be set to a value between ½ and 1 times the data rate.

PLL- Configure the parameters for the PLL.

Loop Filter- Configure the parameters for the loop filter.

6.4.1.1. RF Divider

Setting the RF channel frequency is done through the RF divider register, along with the RF frequency 2, 1 and 0 registers. The RF divider register is used to specify the integer portion of the divide value, and the RF frequency 2, 1 and 0 registers are used to specify the fraction. The values are calculated as follows:

$$\text{DivideVal} = \frac{F_{\text{Channel}}}{24\text{MHz}}$$

Where $F_{Channel}$ is the desired RF center frequency. The value for the RF divider register is found by,

$$\text{Integer} = \text{round}(\text{DivideVal})$$

Where integer is the value used for RF divider. The last step is to calculate the fractional value. This is done as,

$$\text{Fraction} = (\text{DivideVal} - \text{Integer}) \cdot 262147$$

Fraction is the value to be used in the RF frequency 2, 1 and 0 registers. As an example, if the desired RF frequency channel is 903.5MHz,

$$\text{DivideVal} = \frac{903.5\,\text{Mhz}}{24\,\text{MHz}} = 37.6458333$$

$$\text{Integer} = \text{round}(\text{DivideVal}) = 38 = 0\text{x}26$$

$$\text{Fraction} = (\text{DivideVal} - \text{Integer}) \cdot 262147 = -92844 = 0\text{xFE\_95\_54}$$

For this example, the RF divider register is written to 0x26, RF frequency 2 is written to 0xFE, RF frequency 1 to 0x95, and RF frequency 0 to 0x54.This value +/- 1 is fed directly to the PLL as N0 and N1. (i.e. if 63, send 64 and 65 to the PLL)

Table 18: RF Divider - 0X05 [5]

Bit	Name	Comment
7:0	RF_divide [7:0]	00h through 0Bh: not allowed 1Ah: divide by 26 1Bh: divide by 27 ---------- 4Ah: divide by 74 4Bh: divide by 75 4Ch through FFh: not allowed

6.4.1.2. RF Frequency 2

Table 19: RF Frequency 2 = 0X06 [6]

Bit	Name	Comment
7:0	RF_FREQ [23:16]	Upper 8 bits of the RF fraction

6.4.1.3. RF Frequency 1

Table 20: RF Frequency 1 - 0X07 [7]

Bit	Name	Comment
7:0	RF_FREQ [15:8]	Center 8 bits of the RF fraction

6.4.1.4. RF Frequency 0

Table 21: RF Frequency 0 - 0X08 [8]

Bit	Name	Comment
7:0	RF_FREQ [7:0]	Lower 8 bits of the RF fraction

6.4.1.5. Peak Deviation 1

The peak deviation for FSK transmissions is determined by the peak deviation 1 register and the peak deviation 0 register. This value is also used inside the DFT FSK detector. Calculation of the value for the peak deviation is straightforward:

$$\text{PEAK\_DEV} = \frac{\text{Peak\_Deviation (Hz)}}{91.5517}$$

The result of this equation, converted to Hex, is entered into the peak deviation registers.

Table 22: Peak Deviation 1 - 0X09 [9]

Bit	Name	Comment
7:0	PEAK_DEV [15:8]	Upper 8 bits of the peak deviation

6.4.1.6. Peak Deviation 0

Table 23: Peak Deviation 0 - 0X0A [10]

Bit	Name	Comment
7:0	PEAK_DEV [7:0]	Lower 8 bits of the peak deviation

6.4.1.7. RF PLL Options

Contains general options for the setup of the RF PLL.

Table 24: RF PLL Options - 0X28 [40]

Bit	Name	State	Comment
7	Kicker Calibration Status	1	The kicker has been calibrated
		0	The kicker has not been calibrated
6	Temperature Compensation Curve	1	Use the Type 1 compensation for external crystal with curves similar to Type 1 (See Figure 32)
		0	Use the Type 2 compensation for external crystal with curves similar to Type 2 (See Figure 33)
5			
4			
3	Internal Loop Filter	1	Enable using the internal loop filter for the PLL (used for calibration)
		0	
2	Charge Pump Current	1	50uA
		0	25uA
1	Ivco[1:0]	11 01 10 00	Ivco= 1.2mA Ivco= 800uA Ivco= 600uA Ivco= auto level control

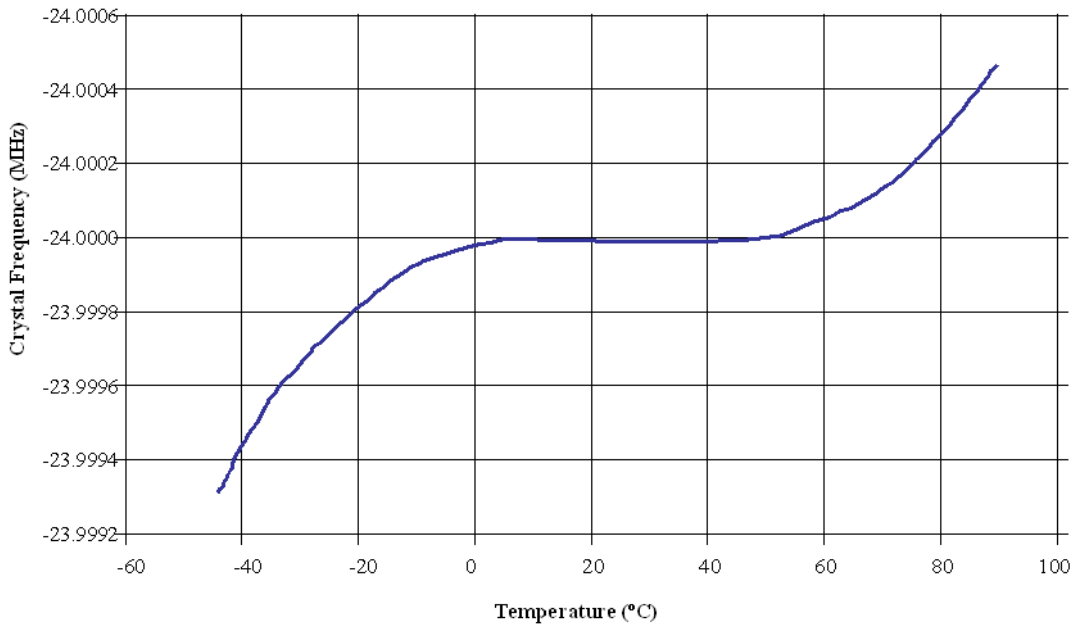


Figure 34: Typical Crystal Temperature Curve for Crystal with Type 1 Characteristics

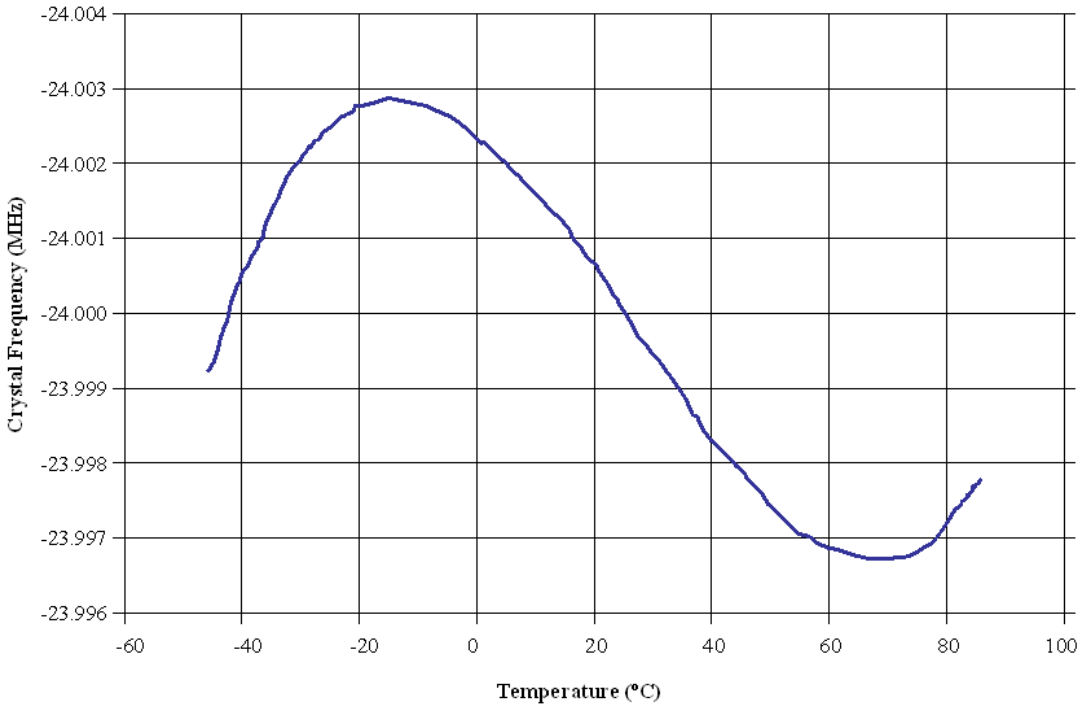


Figure 35: Typical Crystal Temperature Curve for Crystal with Type 2 Characteristics

6.4.1.8. Loop Filter

Table 25: Loop Filter - 0X39 [57]

Bit	Name	Comment
7:0	LOOP_FILTER [7:0]	Internal loop filter

6.4.2. 10kHz Oscillator

The AMIS-53000 has an internal 10kHz oscillator. This oscillator is running whenever the AMIS-53000 is in standby or idle modes. This very low power oscillator provides the clock for timing functions such as Sniff receive, Burst transmit or housekeeping. The oscillator is trimmed in the calibration instructions.

Setup registers descriptions:

10k Oscillator Trim- The value of the calibration for the 10kHz oscillator. (See Section 6.10.1.4)**

6.4.3. System Clock

The AMIS-53000 provides a divided version of the external reference oscillator (typically 24MHz) as an output to an external host/controller or other circuits needing a clock.

Table 26: System Clock Control

Register			Function
Number (HEX)	Name	Bits	
0X0C	General Options A	2,1	11 POR starts in TX
			10 POR starts in RX
			01 POR starts in idle
			00 POR starts in standby
		0	Standby mode with system clock output
0X0D	General Options B	1,0	11 External XTAL reference divided by 2 (12MHz)
			10 External XTAL reference divided by 4 (6MHz)
			01 External XTAL reference divided by 8 (3MHz)
			00 System clock off
0X10	Idle Config	4,3	11 System clock continues for 1024 clock cycles
			10 System clock continues for 512 clock cycles
			01 System clock continues for 256 clock cycles
			00 System clock shuts down after idle command ASAP

Setup registers descriptions:

Crystal Oscillator Trim- The value of the calibration for the 10kHz oscillator. (See Section 6.10.1.1)**

6.4.4. Quick Start

The AMIS-53000 includes the ASTRIC family patented Quick Start oscillator. This circuit uses a "kicker" to force the crystal oscillator close to the final desired frequency. This reduces the time required for the crystal oscillator to settle to the RF frequency.

Table 27: Kicker Calibration

Register			Function
Number (HEX)	Name	Bits	
0X28	RF PLL Options	7	Kicker calibration status

Setup registers descriptions:

Quick Start Trim- The value of the calibration for the kicker. (See Section 6.10.1.3)**

6.4.5. Self Calibration

The AMIS-53000 has internal trim functions for the PLL, TX PLL, RX PLL, 10kHz oscillator, and kicker (Quick Start). A self calibration is started by writing an instruction to the command register. This self calibration needs to be done at least once after the AMIS-53000 has been powered on and before the AMIS-53000 is placed into any mode such as transmit or receive. The application should monitor the status registers and trim value registers to determine that the calibration was successful.

Table 28: Self Calibration Command

Register			Function
Number (HEX)	Name	Code	
0X00	Command	0X07	Calibrate the Quick Start (kicker)
		0X08	Calibrate the 10kHz oscillator
		0X09	Calibrate the PLL
		0X0A	Calibrate the LNA
0X1B	Housekeeping Config	Bit 2	Calibrate PLL during HK
		Bit 1	Calibrate 10kHz oscillator during HK
		Bit 0	Calibrate kicker during HK

Setup registers descriptions:

Status- Contains the results of calibrations, instructions and activity in the AMIS-53000.

Software State- Shows the current mode of the AMIS-53000.

6.4.5.1. Status/Flag1

The purpose of the Status1 register is to provide information back to the host on the status of the part. This register should be queried at the completion of calibration sequences to ensure proper operation. The flags will be reset when the register is read.

CheckSum indicates whether an attempt to read or write the EE has failed due to an incorrect CheckSum.

Instruction enable indicates that the AMIS-53000 is ready to receive an instruction. This can be used to insure that the AMIS-53000 does not miss a command instruction due to the AMIS-53000 not being ready. Along with the busy flag, these status flags can police the flow of commands to the AMIS-53000.

Table 29: Status/Flag1 - 0X01 [1]

Bit	Name	State	Comment
7	PLL xLock	1	PLL out of lock on startup (RX, TX, Sniff, Burst)
		0	
6	TX PLL Cal	1	PLL calibration for transmit failed
		0	
5	RX PLL Cal	1	PLL calibration for receive failed
		0	
4	RC Cal	1	10kHz RC oscillator calibration failed
		0	
3	Quick Start Cal	1	Quick Start calibration failed
		0	
2	CheckSum	1	EE CheckSum failed
		0	
1	Instruction Enable	1	The AMIS-53000 is in a state of operation that can accept instructions
		0	
0	ADC Done	1	ADC conversion complete
		0	

6.4.5.2. Status/Flag2

The Status2 register provides information on the operating status of the part. The busy bit is asserted for any of the following reasons:

Calibration: The busy bit will remain high for the duration of a calibration sequence. Status2 can be repeatedly polled during a calibration sequence to determine when it's complete.

Read/Write EE: While the AMIS-53000 is reading from or writing to the EE, the busy bit will remain set.

Buffered RX: When in receive mode, and a valid chip ID is found, the AMIS-53000 will begin processing of this packet. During the time the packet is being processed, the busy bit will be set high.

Buffered TX: After the command is given for transmit with the buffered packet option enabled, the busy bit will remain high until the part has completed the actual transmission of the packet.

Housekeeping: Busy is asserted during a housekeeping cycle.

Burst TX: Busy is asserted during a Burst transmission.

Status2 also contains information on the reason an interrupt was issued to the external host. The CCA channel status bits provide information back to the host on which channel within the MICS band is being used for communication. After a CCA enabled transmission, these bits will be set to indicate which channel was used. For MICS enabled receivers performing multi-channel Sniff, these bits are used to indicate the channel upon which either energy or an entire packet was found.

If CCA is enabled for operation other than MICS, bit 0 (CCA failed) is used to indicate whether or not the channel is clear. The flags will be reset when the register is read.

Table 30: Status/Flag2 - 0X02 [2]

Bit	Name	State	Comment
7:4	CCA Channel [3:0]		Indicates channel selected during CCA
3:1	Interrupt Type	111 110 101 100 011 010 001 000	RX CRC failed Receive energy dwell timer timed out CCA failed Transmit complete Buffer data for TX Data has been received Housekeeping Low battery
0	Busy	1	AMIS-53000 is busy
		0	

6.4.5.3. Software State

Displays the current mode of the AMIS-53000. This status register can be used to monitor the activity of the AMIS-53000.

Table 31: Software State - 0X3C [60]

Bit	Name	State	Comment
7:0	Software State	1111 1011 1010 1001 1000 0111 0110 0101 0100 0011 0010 0001 0000	Undetermined Startup Copying ROM data to registers Calibrating LNA Calibrating PLL Calibrating 10kHz oscillator Calibrating Quick Start (kicker) oscillator Reading EE data Writing EE data Idle Transmitting Receiving Standby

6.5 Receiver

The AMIS-53000 receiver is designed for either on/off shift key (AM) modulated signals or frequency shift key (FM) modulated signals. The receiver includes all the circuitry to recover data from either the OOK or the FSK modulated signal carrier. The receiver operates on fixed frequencies in the operating frequency range of 300 to 928MHz using an internal fractional N PLL to set the frequency. The receiver can reduce power consumption using the Sniff Mode to acquire the incoming signal. The receiver can set a user defined fixed threshold for data detection or it can form a threshold from the incoming signal for determining the presence of signal and the state of the recovered waveform. The receiver can use a synchronous data detector to extract the data clock and the data from the incoming signal (FSK modulation always uses this method of data detection).

- OOK modulation (AM)
  - Manchester encoding option
  - CDR data detection option (recommended that this be used)
  - Common data rates from 1.2kbps to 19.2kbps or user defined
- FSK/GFSK modulation (FM)

- o Manchester encoding
- o FFT or PLL demodulation (depends on data rate)
- o Common data rates from 1.2kbps to 128kbps or user defined

The AMIS-53000 receiver is a low IF frequency single down conversion, sub-sampling, image rejection architecture with a common AM/FM IF chain. Three demodulators are used for signal detection with additional post-detection and filtering capabilities for data recovery.

- A complex FFT demodulator is used for FSK signals with data rates > 20kbps.
- A digital PLL demodulator is used for FSK signals with data rates less than 20kbps.
- A logarithmic (RSSI) detector is used for OOK/ASK signals.

6.5.1. Receiver Circuit Brief Overview

Clock and Data Recovery: The AMIS-53000 can extract a synchronous clock signal from the received data. In this mode, the data in the received signal is detected, filtered and then fed into the clock and data recovery block where additional digital filtering is performed. The waveform is sampled using a data clock in the AMIS-53000 to synchronously recover the data. Signal sensitivity is improved and the recovered data jitter is reduced by this method.

LO Frequency: A sub-sampling LO frequency architecture is implemented that down converts the incoming RF signal to the IF frequency of about 500kHz. The LO frequency is produced from the internal VCO frequency. The frequency design of the LO signal reduces the power consumption of the AMIS-53000 and simplifies the receiver, achieving reliable, quadrature LO signal generation.

IF Topology: The receiver implements a quadrature down-conversion architecture improving image rejection and creating the signals required for the complex FFT FSK signal detection. The receiver uses this quadrature down-conversion and a combination of passive and active poly-phase filtering to provide image suppression.

Sniff Signal Acquisition: As with earlier ASTRIC devices, the AMIS-53000 can reduce the receiver power requirements by implementing the Sniff Mode for RF signal detection. Sniff Mode is a method using the Quick Start oscillator to quickly wake the receiver, check for signal energy and return to sleep or start the receive function. The Quick Start can start the receiver crystal oscillator in as little as 10 micro-seconds. Using this fast start time, the Sniff Mode can turn on the receiver, check for signal energy and return to sleep in as little as 130 micro-seconds. More information about this Sniff Mode is in Section 6.7.2.

Table 32: Receive Command

Register			Function
Number (HEX)	Name	Code	
0X00	Command	0X01	Instruction to place the AMIS-53000 into receive (remember that all parameters for receive must be set before issuing this command)

Setup registers descriptions:

RX Config- Options for the receiver must be set.

RF Frequency- The RF frequency of the receiver must be configured. (See Section 6.4.1.1)

6.5.1.1. RX Configuration

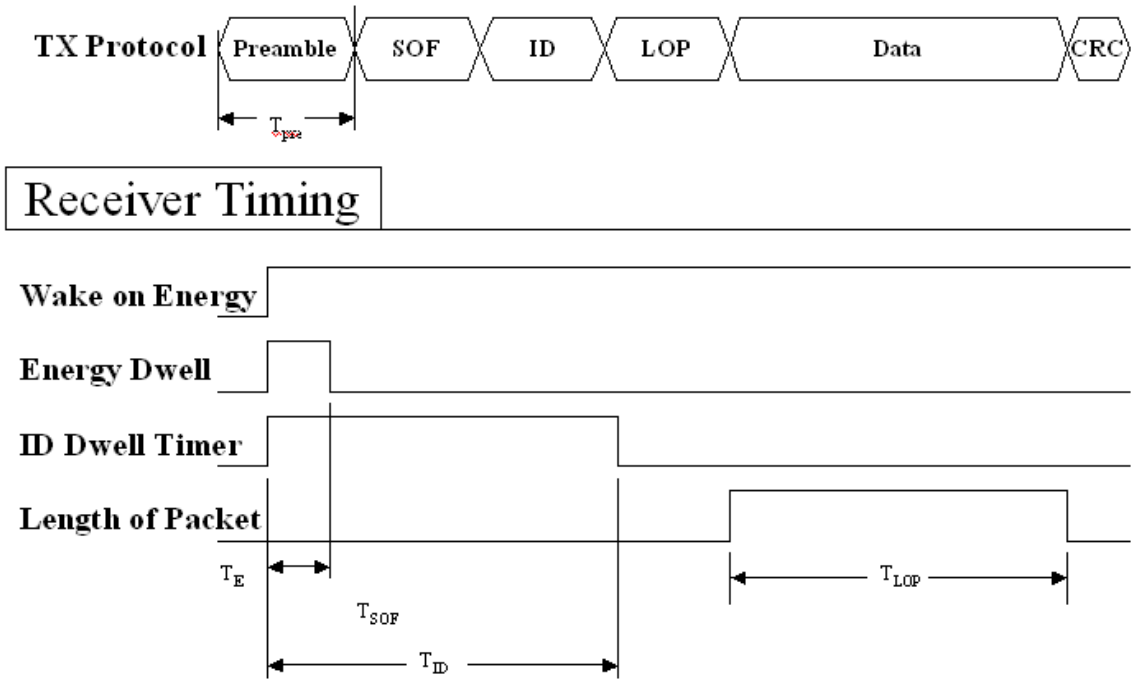


Figure 36: Receiver Timing Chart

Table 33: Receiver Timing

Symbol	Timing				Comments
	Min.	Typ.	Max.	Units	
T_{PRE}	MOD[1]	MOD[1]		D Bits	The TX preamble should be made long enough to allow the receiver to acquire the signal
T_E	0		255	D Bits	The energy dwell timer should be set long enough to allow the receiver to detect the energy[2]
T_{ID}	0		255	D Bits	The ID dwell timer should be set long enough to allow the receiver to detect the chip ID or global ID[2]
T_{LOP}	1	Default	255	D Bits	The length of packet will turn the receiver off after the number of data bits is received

Notes:
1. The need for a preamble and the type of preamble is determined by the data modulation selected.
2. The dwell timers need to be long enough to allow the receiver to stay active from the time it turns on due to energy and the time that the desired event occurs. However, making this number the maximum may in the case of false energy detection or signal corruption may waste system power unnecessarily.

The RX Config register is used to set options for receive mode operation.

Wake on Energy: When enabled, the CDR circuit is held in reset until the energy threshold is met. This option can be used to make the normal receiver function to perform similar to sniff. The energy dwell timer is used to determine how long the receiver will stay on checking for energy (With FF in the energy dwell time register, the receiver will stay on until the threshold is met).

Gate on Energy: This option can be used in FM receive mode only, and will gate the data interface while the energy on RSSI is below the energy threshold.

AM_FM_RX: Sets the mode of operation for receive.

Force MICS Channel: When this bit is set, the bits in Status2 used to show which channel the radio is on can be overwritten to force a particular channel.

Table 34: RX Config - 0X0E [14]

Bit	Name	State	Comment
7	RSSI Active	1	RSSI output during RX
		0	
6	Multi Channel	1	Sniff cycle performed at multiple pre-defined channels
		0	
5	LNA Mode[1:0]	11 10 01 00	No operation defined Linear mode High gain mode Normal gain mode
4			
3	Force MICS Channel	1 0	Force receive mode on a specific MICS channel (status2)
2	AM_FM_RX	1	AM receive mode
		0	FM receive mode
1	Gate on Energy	1	Clock and data outputs gated for RSSI<energy threshold
		0	
0	Wake on Energy	1	Clock and data disabled until energy threshold met

6.5.1.2. Energy Threshold

Sets the threshold for either wake on energy or Sniff Mode. If the automatic noise floor detection is enabled in Sniff, the AMIS-53000 will overwrite the contents of this register each time a new threshold is calculated.

Table 35: Energy Threshold - 0X15 [21]

Bit	Name	Comment
7:0	E_Threshold	Energy detect threshold in DAC Mode = E_THRESHOLD*7.8125mV

6.5.1.3. Receiver Parameters

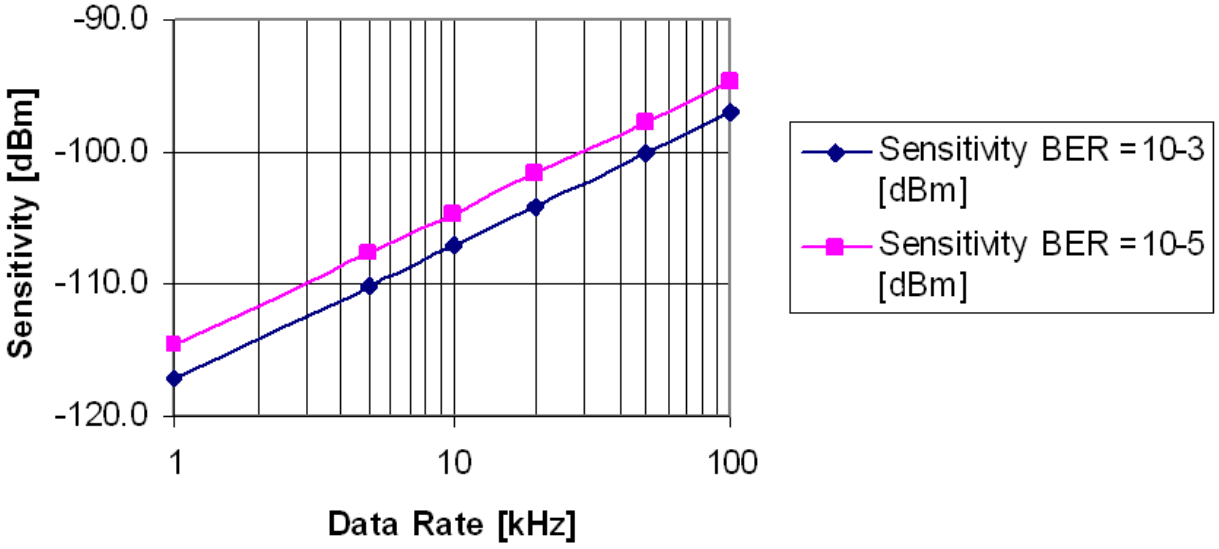


Figure 37: Receiver Sensitivity vs. Data Rate

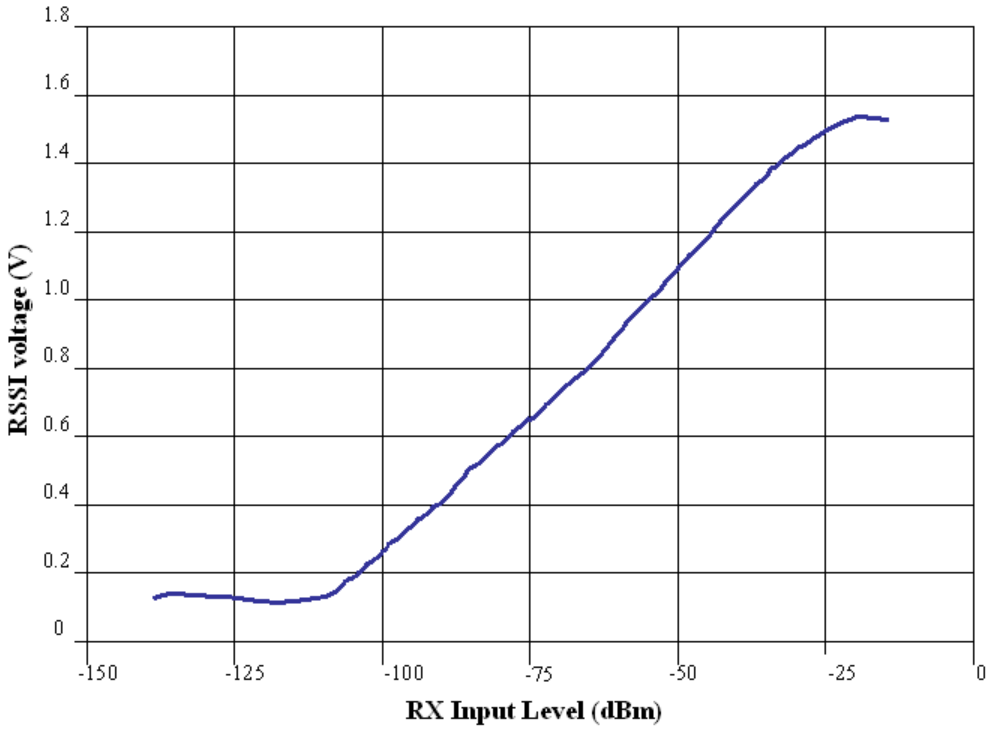


Figure 38: RSSI Curve

6.5.1.4. Data Recovery

Table 36: Receiver Configuration

RX Configuration Registers							Data Rage	Preamble	CDR	SOF
0X0E RX Config		0X1F CDR Options A		0X0B Data Rate Format		0X1E Filter Slice				
Bit 2	Mod	Bit 0	Demod	Bit 3	Code	Bit 1:0				
0	FM	0	FFT	0	NRZ[1]	SLICE[2]	>20k – 128k	10Pattern	Yes[3]	No
				1	Man	SLICE[2]	>20k – 128k	10Pattern	Yes[3]	No[4]
		1	PLL	0	NRZ[1]	SLICE[2]	<20k	10Pattern	Yes[3]	No
				1	Man	SLICE[2]	<20k	All 1 or 0's	Yes[3]	0X55 0XAA
1	AM	0	NA[6]	0	NRZ	SLICE[2]	1k – 19.2k	CW	Opt[7]	0X55
				1	Man	SLICE[2]	1k – 19.2k	CW	Opt[7]	0X0A
		1	NA[6]	0	NRZ	SLICE[2]	1k – 19.2k	CW	Opt[7]	0X55
				1	Man	SLICE[2]	1k – 19.2k	CW	Opt[7]	0X0A

Notes:
1. Long strings of 1's or 0's will degrade the performance of the CDR circuits.
2. SLICE can use the parameters in Table 38.
3. Yes indicates that CDR is always used to detect the data. (SeeTable 41 and Table 42 for CDR parameters)
4. Manchester encoded data requires a SOF. A unique SOF (suggested 0x66) is used to bit-align the Manchester decoder to the recovered data.
5. 0X55 or 0X0A SOF have the following requirements:
   - 0x55 The following is suggested:
     - It is suggested that CDR with fast phase alignment be enabled
     - It is suggested that CDR with activity check be enabled with 8 or 16 bit times
     - It is suggested that the preamble be long enough to trigger activity check (10 or 20 bit times)
   - 0x0A The following is suggested:
     - It is suggested that CDR with fast phase alignment be enabled
     - It is suggested that CDR with activity check be enabled with 4 bit times
     - It is suggested that the preamble be long enough to trigger activity check
6. NA indicates that the parameter is not available for the AM/OOK modulated signals.
7. OPT indicates that CDR is an option to detect the data however, it is recommended that CDR be used. (See Table 41 andTable 42 for CDR parameters)

AM Data Recovery with RSSI

The logarithmic AM detector, used with OOK/ASK modulated signals, produces an RSSI output signal with approximately 18mV/dB output level. A low pass filter provides additional filtering matched to the AM signal data rate (1.2, 1.8, 2.4, 4.8, 7.2, 9.6, 14.4, 19.2kbps). This filtered signal is sampled and compared to the slice threshold to recover the digital data. The slice threshold can be set to a fixed value or it can use a signal tracking circuit to set a peak or average threshold.

The RSSI output signal can also be applied to a clock and data recovery circuit, which synchronizes an AMIS-53000 internal clock with the incoming data rate (See CDR Operation).

Setup registers descriptions:

Slice Threshold- The slice operation needs to be selected, fixed or automatic. The value for the fixed threshold needs to be set.

Filter/Slice- Filter settings and slice mode need to be selected.

Slice Threshold

Sets the data slice level for AM reception. This threshold is used when the slice method sets in the AM data filter and slice options is set to DAC.

Table 37: Slice Threshold - 0X1D [29]

Bit	Name	Comment
7:0	SL_THRESH [7:0]	AM slice threshold in DAC Mode = SL_THRESH*7.8125mV

AM Data Filter and Slice Options

This register contains settings for determining the method of slicing for AM receive mode.

AM_FILTER: Sets the post-detection filter bandwidth for RSSI during AM receive. These filter bandwidths are set for the corresponding data rates. These filter settings can also be used with custom data rates.

AM_HYST: Sets the amount of hysteresis in the AM slice comparator.

AM_SLICE: Used to select the method for providing a reference to the AM slice comparator. DAC Mode: This is a fixed threshold level programmed into the slice threshold register.

Average Mode: This is an automatic threshold level where the AMIS-53000 sets the threshold level to the average level of the RSSI signal. An external capacitor is required on the PEAK pin to set a bandwidth for the low pass filter response of the averaging circuit. Due to the potential for long strings of 1's or 0's in NRZ data this threshold method is not recommended for use with NRZ data.

Peak Mode: This is similar to the average mode, but only the highest level is determined from the incoming signal and the AMIS-53000 sets the threshold to a level 6dB lower than the peak value. An external capacitor on the PEAK pin determines a bleed off (discharge) rate for the peak detector circuit.

Table 38: AM Data Filter and Slice Options - 0X1E [30]

Bit	Name	State	Comment
[7:5]	AM_FILTER[2:0]	000 001 010 011 100 101 110 111	RSSI filter bandwidth =300Hz RSSI filter bandwidth = 600Hz RSSI filter bandwidth = 1.2kHz RSSI filter bandwidth = 2.4kHz RSSI filter bandwidth = 4.8kHz RSSI filter bandwidth = 9.6kHz RSSI filter bandwidth = 19.2kHz RSSI filter bandwidth = 38.4kHz
4	NU		
[3:2]	AM_SLICE[1:0]	00 01 10 11	DAC mode: Slice threshold set in register 1Bh Average mode: AM threshold set using averaging filter Peak detect mode: AM threshold set using peak detector DAC mode: Slice threshold set in register 1Bh
[1:0]	AM_HYST[1:0]	00 01 10 11	0mV slice hysteresis 25mV slice hysteresis 50mV slice hysteresis 100mV slice hysteresis

FM FFT

The AMIS-53000 receiver uses a FFT function to recover data from a FM/FSK modulated signal when the data rate is higher than 20kbps. The FFT detector uses a two-bit DFFT to demodulate the incoming IF signal. This circuit also uses the same clock recovery block (CDR) as the AM detector (See Section 6.1.4) to detect the data.

A pattern of 1's and 0's is required as a preamble. A SOF is not required unless Manchester encoded data is used, requiring a unique preamble to bit-align the Manchester decoder to the recovered data.

Setup registers descriptions:

Data Rate- Can be specified in the discrete data rate register, or specified as a 16-bit word for a user defined data rate. (See Section 7.1.3)

Peak Deviation- The peak deviation register stores the value to be used for both transmit and receive. In the FFT FM receive mode, this value is used to set-up the FFT bins. (See Sections 6.4.1.5 and 6.4.1.6)

FM PLL Detector Loop Filter- For the discrete data rates, the values for the loop filter coefficients are pre-programmed. For user defined data rates, this value needs to be calculated.

PLL Detector Loop Filter Setting

A program (AMIS-53CALC.exe available from AMIS) has been created to aid in the design of loop filter settings.

Table 39: PLL Detector Loop Filter Setting - 0X2B [43]

Bit	Name	Comment
7:0	PLL_CO [7:0]	PLL loop filter setting

FM PLL (Low Data Rate FSK)

The AMIS-53000 uses a PLL function to recover the data from a FM/FSK modulated signal with data rates 20kbps or lower. This circuit uses an A DPLL for demodulation, the output of which is fed to the AM CDR circuit to recover the clock, and additionally filter the output data.

The preamble sent by the AMIS-53000 when configured as NRZ FM is a repeating sequence of 1's and 0's. This gives the CDR circuit and PLL demodulator sufficient edges to acquire lock. Hence, for the NRZ case it is unnecessary to include a SOF byte. In Manchester mode, the preamble is specified as all 1's (or 0's). This gives the clock recovery circuit the most edges for lock acquisition. However, due to the ambiguity of the preamble, a SOF byte is necessary for the Manchester decoding block. The suggested SOF for this is either #55h or #AAh. The length of preamble necessary for this mode is dependant upon the loop bandwidth for the clock recovery PLL.

Setup registers descriptions:

Data Rate- Can be specified in the discrete data rate register, or specified as a 16-bit word for a user defined data rate. (See Section 7.1.3)

Peak Deviation- The peak deviation register stores the value to be used for both transmit and receive. In the FFT FM receive mode, this value is used to set-up the FFT bins. (See Sections 6.4.1.5 and 6.4.1.6)

M PLL Detector Loop Filter- For the discrete data rates, the values for the loop filter coefficients are preprogrammed. For user defined data rates, this value needs to be calculated. (See PLL Detector Loop Filter Setting)

6.5.1.5. Clock and Data Recovery

The AMIS-53000 device performs clock and data recovery for both AM/OOK/ASK and FM/FSK signals. An internal clock in the AMIS-53000 is programmed to be nearly the same rate as the expected data rate in the incoming signal. This clock is then synchronized to the incoming data rate by extracting a clock from the data. This loop recovery method recovers data without much of the jitter and noise associated with wireless communication links.

Before launching headlong into the operation of the detectors, and how to set them up, it is instructive to review the following related registers, setup options and their functions.

Setup registers descriptions:

Fast Phase Alignment: In both the AM and PLL based FM modes (lower data rate), the AMIS-53000 can be configured to quickly acquire phase lock on incoming data. The pattern necessary for the fast phase alignment is simply '1010'. This function can be enabled in the CDR options A register. With this function enabled, the CDR circuit will operate with minimum power consumption until the '1010' sequence is received. A 32-bit correlation is used to not only recognize the 1010 pattern, but also to instantaneously provide a phase correction to the clock recovery circuit allowing very fast (less than 4 bit) lock times locking the incoming data.

Activity Check: This function can be used in conjunction with the fast phase alignment to reset the clock and data recovery block back into its minimal power consumption mode when no transitions are detected on the data line for a specified period. The check can be configured for 4, 8 or 16 bit times.

Over-Sampling Clock (Ts Clock): All three detectors use the Ts clock as the sampling clock for the transition from analog to digital. This clock should be set to the highest rate possible, but not greater than 400x the data rate, to ensure adequate phase information. For the discrete data rates, this value is pre-programmed for those rates.

Data Rate Clamp: The data rate clamp restricts the clock recovery circuit from wandering when an actual signal is not present, and the phase error signals being generated come only from noise. Small fractional values for the clamp can lead to longer lock times since the clock recovery PLL may not be able to make as large of a correction as is necessary all at once.

Channel Clamp: This clamping circuit is used to hold the low data rate FSK PLL detector within the specified limits to prevent the PLL from wandering in the absence of signal.

CDR Operation

This circuit utilizes an all digital PLL (ADPLL) to recover the clock from the raw sliced data. The slicer output is integrated over a bit time to provide a phase error, and the sign of the integration is used to determine the data symbol.

When using the AMIS-53000 in AM mode with any of the packet framing options enabled, it is necessary to have the SOF byte for proper start-up of the AM CDR circuit. It is recommended that the CDR is set up with the activity check, and fast phase alignment features enabled for the packet framing modes. The preamble that the AMIS-53000 will transmit in AM mode is CW, hence the SOF byte is used by the fast phase alignment feature in the CDR to acquire lock. The suggested SOF for AM NRZ format is #55h. This will provide the most transitions for the clock recovery circuit to acquire lock prior to the incoming packet. For Manchester operation, the suggested SOF is #0A. This will provide early transitions for phase lock, and 4 bits to align the Manchester decode.

Because there are no transitions during the preamble in AM mode, the CDR relies on the fast phase alignment for acquiring lock. As this is the case, the length of the preamble can be quite short as long as the activity check is enabled. The preamble should be long enough to trip the activity detection circuitry such that the fast phase alignment circuit is reset at the beginning of the SOF. This guarantees that the fast phase alignment will kick in during the SOF. The suggested length for the preamble is 4 BT's for Manchester with activity check set to 4 BT's, and 10 or 20 for NRZ, with activity check set to 8 or 16 respectively. Note in the NRZ case, enabling activity check will require the data be formatted to guarantee at least one transition in the data during the length of activity check (i.e. every 8 or 16 BT's).

Setup registers descriptions:

ID Dwell- Set a time that the CDR circuit will continue to search for the chip ID.

CDR Config- Set the parameters for the clock and data recovery circuits.

Data Rate- Can be specified in the discrete data rate register, or specified as a 16-bit word for a user defined data rate. (See Section 7.1.3)

Start of Frame- Byte used to tell the AMIS-53000 receiver that data will start. (See Section 7.1.6)

Clock Recovery Loop Filter- For the discrete data rates, the values for the loop filter coefficients are pre-programmed. For user defined data rates, this value needs to be calculated.

Chip ID Dwell Timer

Used to specify how long the clock and data recovery circuit will stay active after energy has been detected, looking for a valid chip ID. The part will look for either the chip ID or the global ID.

Table 40: Chip ID Dwell Timer - 0X14 [20]

Bit	Name	Comment
7:0	C_DWELL [7:0]	00h: Code dwell timer disabled (for standard receive wake on code) 01h – FFh: Code dwell time = C_DWELL*bit time * 8

CDR Options A

This register contains settings for determining the clock and data recovery parameters.

- DR_Clamp: Limits the CDR frequency drift between data packets.
- Channel_Clamp: Restricts the bandwidth to the channel bandwidth.
- Activity Check: Sets a number of bit times that the CDR circuit will shut down if there is no data present.
- Fast Phase Alignment: Forces the CDR circuit to quickly synchronize to the incoming data.
- FM Mode: The FM detector used in the receiver depends on the data rate of the incoming signal.

Table 41: CDR OptionsA - 0X1F [31]

Bit	Name	State	Comment
7,6	DR Clamp<1>	11	1/64
		10	1/32
		01	1/16
		00	1/8
			The clamp restricts the clock recovery PLL to +- the fraction selected of the frequency selected by the BaudCLK which prevents clock wandering between data packets
5,4	Channel Clamp	11	+-150
		10	+-100
		01	+-50
		00	+-16
			The clamp restricts the PLL detector to only lock on signals that are within the specified window, centered +-500kHz of the IF frequency
3,2	Activity Check <1>	11	Reset after 16 bit times of no activity
		10	Reset after 8 bit times of no activity
		01	Reset after 4 bit times of no activity
		00	Activity check disabled, clock recovery will always run
1	FPA Enable	1	The CDR circuit will perform fast phase alignment
		0	CDR always running
0	FM Mode	1	PLL
		0	FFT

CDR Options B

The sample clock values are written from ROM with the discrete data rate selected. The sample rate should be as fast as possible without exceeding 400 samples per bit time.

Table 42: CDR OptionsB - 0X20 [32]

Bit	Name	State	Comment
7	CDR Reset	1	CDR is held reset
		0	
6	NU		
5	NU		
4	NU		
3:0	Sample Clock	1011	45kHz
		1010	90kHz
		1001	187.5kHz
		1000	375kHz
		0111	750kHz
		0110	1.5M
		0101	3M
		0100	6M
		0011	8M
		0010	12M
		0001	16M
		0000	24M

Clock Recovery Loop Filter Setting

A program (AMIS-53CALC.exe available from AMIS) has been created to aid in the design of the CDR loop filter settings.

Table 43: Clock Recovery Loop Filter Setting - 0X2C [44]

Bit	Name	Comment
7:0	CDR_CO [7:0]	Clock recovery filter setting

6.6 Transmitter

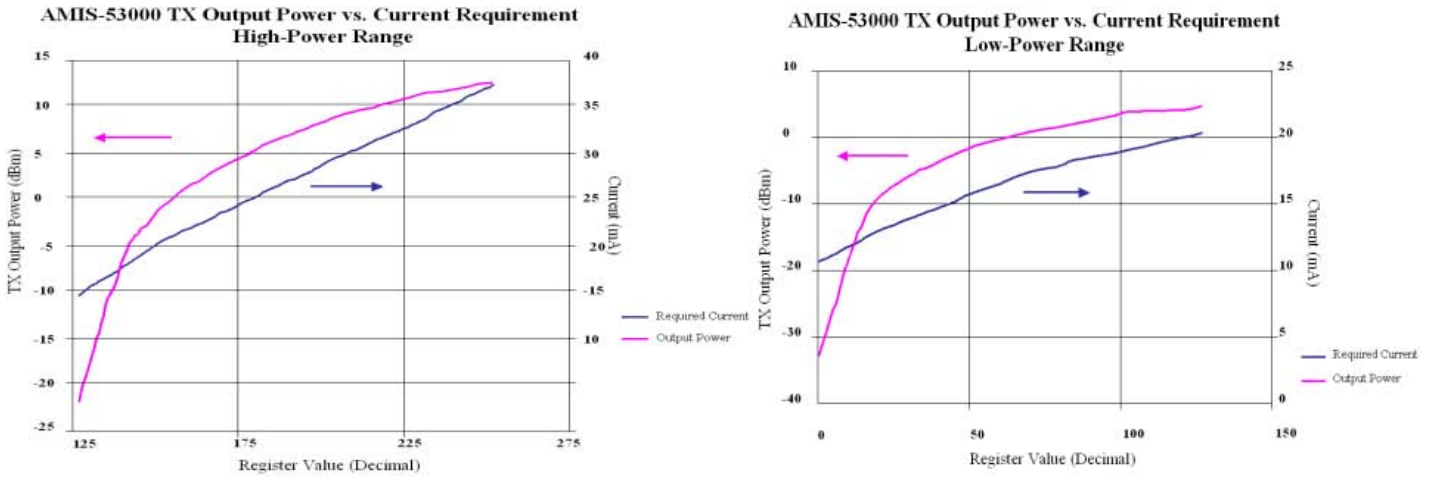


*Figure 39: Typical Output Power vs. Power Register Setting**

*Note: Curve is for output matched to 50Ω.

Table 44: Transmit Command

Register			Function
Number (HEX)	Name	Code	
0X00	Command	0X02	Instruction to place the AMIS-53000 into transmit (remember that all parameters for transmit must be set before issuing this command)

The AMIS-53000 uses a switching class E power amplifier as the high power output driver. The high power PA can be bypassed to allow a high efficiency at a lower output power. The output drivers are turned on and off directly in AM/OOK/ASK data modulation. A direct modulation PLL is used to form the FM/FSK signal for transmission. The PLL loop runs at half of the desired transmit frequency to provide excellent on/off ratio for AM, and to lower current consumption in the PLL.

- OOK modulation (AM)
- FSK modulation (FM)
- Burst mode transmit
- FM wave shaping
- High power and low power range

Setup registers descriptions:

Data Rate- Can be specified in the discrete data rate register, or specified as a 16-bit word for a user defined data rate. (See Section 7.1.3)

RF Frequency- The RF frequency of the transmitter must be configured. (See section 6.4.1)

Output Power- Sets the RF output level for the AMIS-53000.

Peak Deviation- The FM deviation must be set for FM operation. (See section 6.4.1.5 and 6.4.1.6)

TX Config- Options for the transmitter must be set.

Preamble- Set a reasonable length of preamble to insure that the receiver can detect the signal.

6.6.1. TX Config

General options for transmit.

AM_FM_TX: Used to set the mode for transmit.

Shaping: When enabled, the FSK transitions are digitally shaped in the fractional N PLL with a pre-programmed sequence. The filter for the shaping is Gaussian with a BT=1. This reduces the high frequency content of the data waveform that modulates the carrier.

ID for TX: This option specifies which ID the AMIS-53000 will transmit when the use ID bit in general options A is enabled. Global is used to transmit to all devices, chip ID will transmit the transmitters chip ID.

Buffered TX: When this option is enabled in conjunction with use ID and LOP enable, the packet for transmission is loaded into internal RAM prior to the RF being enabled.

Force MICS Channel: When this bit is set to 1, bits[7:4] of Status2 can be written to force the transmitter to operate on a specific MICS channel.

Clear Channel Assessment: When one of the CCA modes of operation are enabled, the AMIS-53000 will enable its receiver to first check for the presence of energy on the specified channel before transmitting.

Table 45: TX Config - 0X0F [15]

Bit	Name	State	Comment
7,6	Clear Channel Assessment	11 10 01 00	Not allowed MICS multi-channel assessment (pre-defined channels) Single clear channel assessment prior to transmit (any frequency) No clear channel assessment performed, normal operation
5	Force MICS Channel	1	
		0	
4	Smooth Turn On	1	Enable smooth power up of PA (reduces the spurious response of the TX on power up)
		0	
3	NU		
2	ID for TX	1	Use the defined chip ID from the chip ID register
		0	Use the defined global ID from the chip ID register
1	Shaping	1	Gaussian FM data shaping enabled
		0	FM data shaping disabled
0	AM_FM_TX	1	AM transmit mode
		0	FM transmit mode

6.6.2. Output Power

C_POWER: Coarse output power control for the power amplifier. When set high, the max out is 15dBm - when set low, the max output is 0dBm.

F_POWER: Fine output power control for the PA. These 7 bits control the voltage on the RFPWR pin via an internal DAC.F_POWER is sent to the DAC as the upper 6 bits. Lower 2 bits are 0.

Table 46: Output Power - 0X18 [24]

Bit	Name	Comment
7	C_POWER	Coarse output power selection sent to PA
6:0	F_POWER [6:0]	Fine output power control (upper 7 bits of the DAC, LSB of DAC=0)

6.6.3. Preamble Length

This byte is used to define the length of preamble to send prior to data in both transmit and Burst mode transmit.

Table 47: Preamble Length - 0X1A [26]

Bit	Name	Comment
7	PreambleLen [7:0]	Length, in bit times, of CW (AM), or ’10 (FM) sent prior to preamble in Burst

Table 48: Suggested Preambles

Modulation	Preamble	Comment
AM NRZ with CDR	CW	SOF required and suggested as 0X55[1]
AM Manchester with CDR	CW	SOF required and suggested as 0x0A[2]
FM FFT	1/0 pattern	No SOF is required
FM PLL (NRZ)	1/0 pattern	No SOF is required
FM PLL (Manchester)	All 1s or 0s	SOF is required and suggested to be 55(Hex) or AA(Hex)[3]

Notes:
1. When using SOF with NRZ data, it is suggested that fast phase alignment is enabled, activity check is set to 8 or 16 and preamble length is 10 or 20 bit times.
2. When using SOF with Manchester coded data, it is suggested that fast phase alignment is enabled, activity check is set to 4 bit times and preamble length is set long enough to trigger the activity check.
3. The length of this preamble is dependent on the loop bandwidth of the recovery clock PLL.

6.6.4. FM Transmit Data Shaping

The AMIS-53000 allows the user to enable data shaping of the data waveform to improve the RF spectral efficiency. When enabled, the clock recovery NCO is used to provide an internal clock at 16 times the selected data rate. This clock is used to cycle through a pre-defined pattern whenever a transition is detected on the TX input. The shaping pattern is Gaussian with a BT=1. The intermediate values for the shaping are determined from the peak deviation register when an external host/controller writes the ‘ROM 2 REGS’ to the AMIS-53000 command register.

6.7 Idle

Table 49: Idle Command

Register			Function
Number (HEX)	Name	Code	
0X00	Command	0X03	Enable the idle state
		0X04	Return to idle state

Table 50: Idle Configuration

Register			Function
Number (HEX)	Name	Bits	
0X02	Status/Flag2	0	AMIS-53000 is busy
0X0C	General Options A	2:1	Select state that AMIS-53000 enters on POR
		0	Output system clock in standby mode
0X0D	General Options B	1, 0	Select the system clock frequency

Note that there are two low-power modes for AMIS-53000 – standby and idle. Standby allows the SYSCLK output. Idle is the very low power state without SYSCLK output.

Table 51: Idle Modes

Idle Tasks	Description
Sniff	Receiver periodic wake up and RF energy detection check
Burst Transmit	Periodic wake and transmit function
Housekeeping	Used to perform periodic temperature correction, calibration or to wake external host/controller
Standby	Low-power mode with no activity may be programmed to continue to output system clock

The AMIS-53000 allows for a low-power mode. Power requirements are reduced when the very low power 10kHz oscillator is the clock for the device. This oscillator runs the timers for either the Sniff wake up timer, the Burst transmit timer or the housekeeping wakeup timer. However, even when the low power 10kHz oscillator is running, the AMIS-53000 can still provide a clock signal output to an external host/controller device such as a microprocessor after reception of a valid data packet or a housekeeping cycle where the AMIS-53000 has been programmed to issue a wake up to the external host/controller.

The AMIS-53000 will return to this low power idle state after activities such as transmit, receive or the various timers are done and the external host/controller writes the 'Return to Idle' instruction to the AMIS-53000 command register.

Setup registers descriptions:

Idle Config- The options for idle mode must be set.

6.7.1. Idle Config

The idle configuration register is used to specify which periodic tasks are performed once the idle command is given in register 0. Any combination of Sniff, Burst and housekeeping can be enabled.

INT to DSSN Timing: This is the time between the AMIS-53000 issuing an interrupt to indicate that data is ready and the time that data transfer starts with the assertion of the DSSN signal.

Idle to System Clock Stop: Once the AMIS-53000 has completed a task and is issued the idle command, the system clock can produce additional clock cycles to allow the external host/controller to finish its tasks.

Table 52: Idle Config - 0X10 [16]

Bit	Name	State	Comment
7:5	Wait timing between INT and DSSN for Sniff Receive	111 … 000	DSSN going active is delayed 8 bit times from INT
			DSSN is immediately active after INT
4,3	Wait timing between idle instruction and system clock shutoff time	11	System clock outputs 1024 clock cycles before shutdown after idle command
		10	System clock outputs 512 clock cycles before shutdown after idle command
		01	System clock outputs 256 clock cycles before shutdown after idle command
		00	System clock immediately shuts down after idle command
2	Housekeeping Enable	1	Periodic housekeeping enabled (HK settings must be set)
		0	
1	Burst Enable	1	Periodic Burst mode enabled (BURST settings must be set)
		0	
0	Sniff Enable	1	Periodic Sniff Mode enabled (Sniff settings must be set)
		0	

6.7.2. Sniff Mode Operation

Table 53: Sniff Mode Configuration

Register			Function
Number (HEX)	Name	Bits	
0X0E	RX Config	1	Force the receiver to not output Clk&Data < energy level
		0	Set the receiver to wake when at energy level threshold
0X10	Idle Config	2	Enable periodic Sniff Mode

The quick start technology enables the AMIS-53000 to operate its receiver in a mode called Sniff Mode. As implemented in the AMIS-53000, this Sniff Mode can wake the receiver and acquire the transmitted message in as little as 130 microseconds.

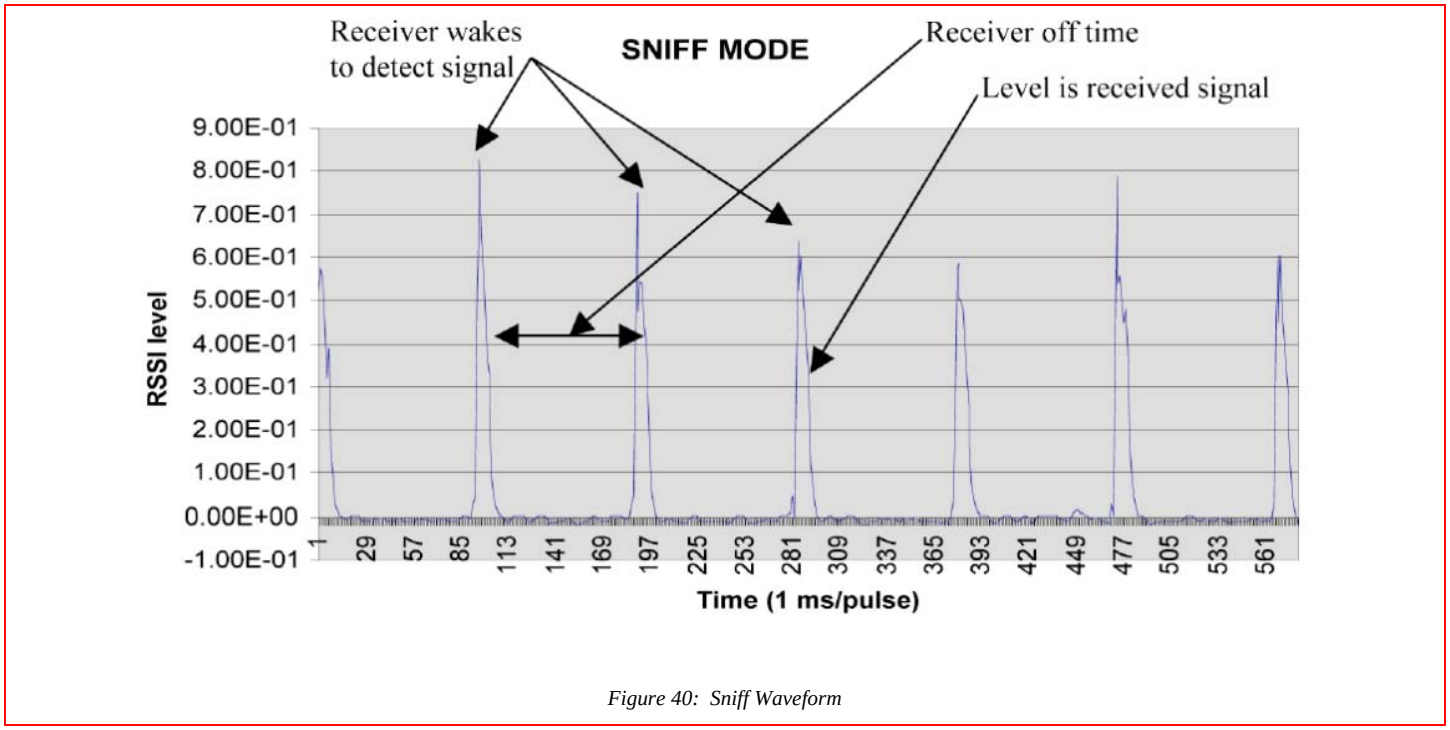


Figure 40: Sniff Waveform

The Sniff Mode of operation puts the AMIS-53000 receiver into a cyclic mode of sleeping and periodically waking to check for received signal energy. When energy is detected the receiver is placed in receive mode and the AMIS-53000 attempts to recover data. The receiver in Sniff Mode can be configured to check for a valid ID. The failure to receive a valid ID will cause the receiver to go back to sleep.

The AMIS-53000 receiver average supply current can be estimated as:

$$I_{AC} = I_{IN}\frac{\tau}{T+\tau} + I_{SM}\frac{T}{T+\tau}$$

Where, I_{IN} is receiver current consumption in continuous receive mode, equal to or less than 12mA;

I_{SM} is receiver current consumption in sleep mode, equal to or less than 2uA;

τ is programmable receiver energy scan impulse on time (sniff time), approximately equal to 130µs minimum;

T is programmable receiver off time period length between receiver energy scan impulses (sniff mode interval).

Setup registers descriptions:

Sniff Config-This sets the options in the Sniff Mode.

Sniff Interval- Set the time interval between receiver wakeups in the Sniff Mode.

Energy Threshold- The threshold for detecting the incoming RF energy must be set (see Section 6.5.1.2).

Energy Dwell Time- Set the time interval that the receiver will remain active looking for RF energy detection.

Code Dwell Time- Once RF energy has been detected the receiver can determine if the message has the unique ID for that receiver. The time interval for looking for this ID must be set. (See Chip ID Dwell Timer)

Threshold- The number of times a wake up is received can be monitored for false wake ups and the energy threshold adjusted to account for the noise level.

6.7.2.1. Sniff Config

The Sniff config register is used to set additional options for the operation of the part during a Sniff cycle, beyond those set in the RX config register.

SNIFF_FILTER: Setting for the energy detection filter. This allows for different settings of the AM data filter between Sniff and receive. The energy dwell timer needs to be extended long enough to allow for this filter to settle during the Sniff cycle.

Auto-Threshold Count Value: Number of Sniff cycles used to determine whether to raise or lower the energy threshold for sniff. Any value other than 0x00 in this register will enable the auto-threshold function.

Multi Channel: This bit is used in MICS mode of operation to enable the AMIS-53000 to scan the nine pre-defined MICS channels programmed into the AMIS-53000.

Sniff Interval Resolution: Determines the clock for the Sniff interval timer.

Table 54: Sniff Config - 0X11 [17]

Bit	Name	State	Comment
7:5	SNIFF_FILTER	000 001 010 011 100 101 110 111	RSSI filter bandwidth =300Hz RSSI filter bandwidth = 600Hz RSSI filter bandwidth = 1.2kHz RSSI filter bandwidth = 2.4kHz RSSI filter bandwidth = 4.8kHz RSSI filter bandwidth = 9.6kHz RSSI filter bandwidth = 19.2kHz RSSI filter bandwidth = 38.4kHz
4,3	Auto-Threshold Count Value	11 10 01 00	100 500 100 Disable This is the number of Sniff cycles to count false wake ups due to the noise level, so that the threshold level can be adjusted. It is adjusted higher when the number of false wake ups exceeds the wake up target number. It is adjusted down when there are fewer false wake ups than the target number. Entering a number other than 00 in this register will enable the auto-threshold.
2	NU		
1	NU		
0	Sniff Interval Resolution	1	Sniff interval timer resolution is 100ms (interval between Sniff signal detection events is (Sniff interval) times (Sniff resolution)
		0	Sniff interval timer resolution is 500us 100ms (interval between Sniff signal detection events is (Sniff interval) times (Sniff resolution)

6.7.2.2. *Sniff Interval Timer*

Used to specify the period (time between Sniff events) of the Sniff operation. The Sniff interval is this value times the Sniff interval resolution value (set in the Sniff config register).

Table 55: Sniff Interval Timer - 0X12 [18]

Bit	Name	Comment
7:0	SNIFF_INT [7:0]	Sniff interval timer =SNIFF_INT* Sniff interval timer resolution

6.7.2.3. *Energy Dwell Timer*

Length of time receiver will stay on in a Sniff cycle checking for the presence of a signal. Also used for a receive command when the wake on energy bit is asserted in RX config. When used for a MICS market device, this may need to be set to 10 milli-seconds for CCA to be compatible with the MICS standard.

Table 56: Energy Dwell Timer - 0X13 [19]

Bit	Name	Comment
7:0	E_DWELL[7:0]	00h: Energy dwell timer not used, energy determined by an impulse sample 01h – FEh: Energy dwell time = E_DWELL * 100us FFh: Receiver remains on until energy threshold is met

6.7.2.4. *Energy Threshold*

Sets the threshold for either wake on energy or Sniff Mode signal acquisition. If the automatic noise floor detection is enabled in Sniff, the AMIS-53000 will overwrite the contents of this register each time a new threshold is calculated.

Automatic Threshold Optimization in Sniff Mode

An option available in the Sniff Mode config register will enable the AMIS-53000 to automatically adjust the energy threshold of the AMIS-53000 to optimize the sensitivity of the Sniff Mode. The target number of wake ups (register 0X2F) allows the user to specify a value for the number of false wake ups the AMIS-53000 is allowed with the selected configuration of the Sniff Mode (by bits [4:3] in the SNIFF_CONFIG register) number of Sniff cycles.

As an example:

If the number of Sniff cycles is set to 500 (Sniff config [Bit 4:3]),
If the target number of false wake ups is set to 50 (target number wake ups),
Then over the course of the next 500 Sniff cycles the radio is triggered falsely by energy:
More than 50 times, the threshold will be increased to reduce the sensitivity,
Less than 50 times, the threshold will be decreased to increase the sensitivity.

Using this option to set the threshold for energy detection can have a dramatic impact on the life of battery powered devices, as the AMIS-53000 will adjust to changing levels of background noise while still maintaining maximum sensitivity, and not wasting power by continually waking and processing background noise.

Additionally, the energy threshold setting can be monitored by an external host/controller. The amount the threshold will increase or decrease is based on Table 57, with the order of the rows in the same order as the AMIS-53000 will evaluate the conditions.

Table 57: Auto Threshold Adjust

Condition	Adjustment
Select the number of Sniff cycles as the test period	
Enter the desired number of false wake ups per period	Note: a false wake up is when the receiver detects energy but fails to detect the ID in the packet
Then if wake ups/period > target	Threshold is increased
Then if wake ups/period < target	Threshold is decreased

The threshold of the AMIS-53000 can vary over a wide range from one device to the next, due to design, manufacturing tolerances, and environment changes; temperature and voltage. This automatic threshold optimization can be used to adjust the threshold by monitoring the level of false wake ups due to background noise. The adjustment in this fashion can reduce the effects of design and manufacturing on the threshold setting of the AMIS-53000.

Setup registers descriptions:

Target- Set a value for the allowed number of false wake ups desired.

Target Threshold

The number of false wake ups occurring during a period of time is used to automatically adjust the energy threshold in the Sniff operation. This allows the AMIS-53000 to automatically adjust its input level to compensate for, manufacturing, components, environment, temperature, and/or voltage.

Table 58: Target Wake Ups - 0X2F [47]

Bit	Name	Comment
7:0	Target [7:0]	The number of wake-ups that the Sniff circuit will try to adjust the threshold to not have more false wake ups or less missed signal detections. This register allows the number to be 0 to 255, but this number should always be less than the number of Sniff count (Sniff config bit 4:3).

6.7.3. Burst Transmit Data

Table 59: Burst Transmission Configuration

Register			Function
Number (HEX)	Name	Bits	
0X10	Idle Config	1	Enable Burst transmissions

Burst mode of transmission is a function that can cause the AMIS-53000 to transmit a message at a programmed time interval or by asserting the xBURST pin to active (the AMIS-53000 must be in the xBURST mode), causing the AMIS-53000 to immediately transmit a message. The Burst mode can also be started by enabling the Burst mode in the idle register and then writing to the command register to set the AMIS-53000 into idle mode. The xBURST modes sets a timed automatic transmission of register values (a message) or ADC conversion values.

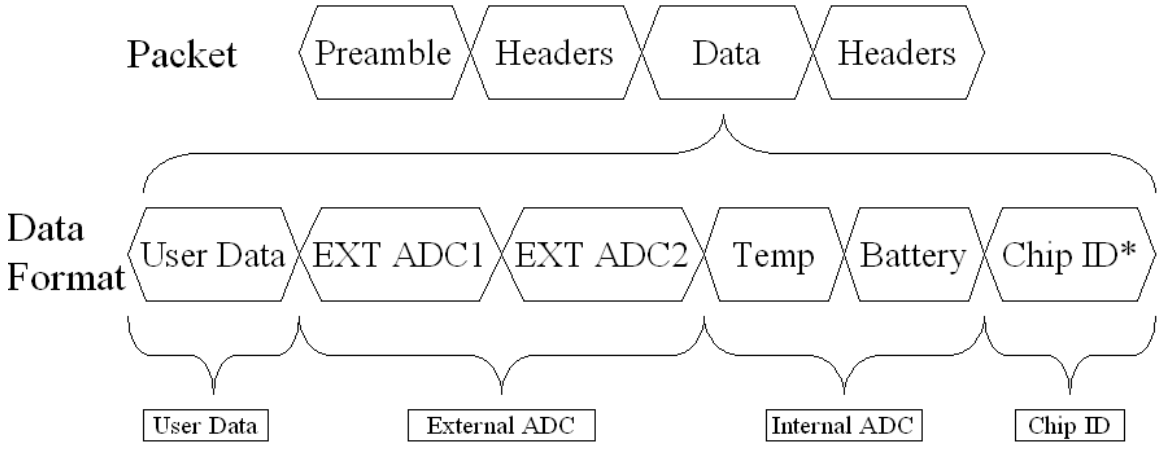
Setup registers descriptions:

Burst Config- Set the Burst transmission parameters.

Burst Interval- Set the time interval between Burst transmissions.

User DataA- Message for timer initiated transmissions.

User DataB- Message for xBURST initiated transmissions.



User Data	Normal Burst	User Defined Data A register contents are sent if register is non-zero
	Interrupt Burst	User defined Data B register contents are sent if register is non-zero
Ext ADC	Enabled	The contents of both external ADC conversions are sent when enabled by BURST CONFIG (Bit 1)
Int ADC	Temp Sensor	The contents of the Temperature Senor and the Battery Voltage (Divided by 2) are sent when enabled in BURST CONFIG (Bit 2)
	Battery Voltage	
Chip ID		The ID in the Chip ID register is sent (LSB first) when enabled in BURST CONFIG (Bit 3)

Figure 41: Data Packet Format Showing Order for Burst TX Content

Used to set the options for the Burst mode of operation:

R_BURST: These bits set the number of times the packet is to be repeated each Burst interval. This can be used to increase the probability that all packets will get through when several Burst transmitters are located in the same area.

Send Chip ID: This option is included to allow for the operating case of having multiple transmitters sending to a single receiver. The multiple transmitters will need to be configured to send the global chip ID in the TX config options so that the receiver will wake on each transmitters packet. Sending the chip ID as part of the payload allows the receiver to differentiate the packets.

Send Internal ADC Data: When enabled, the AMIS-53000 will perform conversions on the battery voltage, and temperature sensor and include these conversions as part of the packet payload.

Send External ADC Data: When enabled, the AMIS-53000 will perform conversions on the two external ADC inputs and include these conversions as part of the packet payload.

Burst Interval Resolution: Used to define the clock frequency for the Burst interval timer.

Table 60: Burst Config - 0X16 [22]

Bit	Name	State	Comment	
7		1		
		0		
6		1		
		0		
5:4	R_BURST[1:0]	00 01 10 11	Packet is sent one time Packet is repeated once Packet is repeated two times Packet is repeated three times	Repeat interval*
3	Send Chip ID	1	Chip ID is included as part of the packet	
		0		
2	Send Internal ADC Data	1	Data for temperature and battery is sent	
		0		
1	Send External ADC Data	1	Data for EXT1, EXT2 is sent	
		0		
0	Burst Interval Resolution	1	Burst interval timer resolution is 15s	
		0	Burst interval timer resolution is 50ms	

NOTE: When the Burst transmission is repeated the interval between transmissions is a random time period produced in a random number generator with the chip ID value used to seed the random number generator.

6.7.3.1. Burst Interval

Defines the period for the normal Burst transmission to occur. This is a cyclic mode and the AMIS-53000 will transmit the contents of a register at the end of each interval. This interval is fixed by the register value unlike the random time interval when the transmission is repeated.

Table 61: Burst Interval - 0X17 [23]

Bit	Name	Comment
7:0	BURST_INT [7:0]	Burst interval= (BURST_INT+1)*Burst interval resolution

6.7.3.2. User Defined Data A

Table 62: User Defined Data A - 0X2D [45]

Bit	Name	Comment
7:0	USE_DATAA [7:0]	Optional data to be sent in normal Burst mode if non-zero

6.7.3.3. User Defined Data B

Table 63: User Defined Data B = 0X2E [46]

Bit	Name	Comment
7:0	USE_DATAB [7:0]	Optional data to be sent in interrupt triggered burst if non-zero

6.7.4. Housekeeping

Table 64: Housekeeping Enable

Register			Function
Number (HEX)	Name	Bits	
0X10	Idle Config	0	Enable housekeeping timed functions

Housekeeping is another periodic operation mode, which can be used to periodically perform operations such as oscillator calibrations, PLL calibration, EE refresh, or temperature compensation. It can also be used to periodically wake an external host/controller to allow it to perform whatever tasks it may need to. The housekeeping configuration register contains the options to specify what is to occur during a housekeeping cycle, and the housekeeping interval timer is used to control how frequently the wake up occurs.

Setup registers descriptions:

Housekeeping Config- Set the Burst transmission parameters.

Housekeeping Interval- Set the time interval between Burst transmissions.

6.7.4.1. Housekeeping Config

The housekeeping configuration register is used to specify which tasks the AMIS-53000 should perform during a housekeeping cycle.

HK Interval Resolution: Used to specify the clock frequency for the housekeeping interval timer.

Wake: When enabled, the AMIS-53000 will enable the system clock output, and issue an interrupt to an external controller.

Write EE: This option is used to store the values of any calibrations that may have been performed during housekeeping. The entire working register bank will be written to EE.

Read INT ADC Channels: The AMIS-53000 will do conversions on the battery voltage and temperature sensor. This can be used as a method to periodically update the temperature compensation loop.

Read EXT ADC Channels: When enabled, the two external ADC inputs will be converted during a housekeeping cycle.

Cal PLL, RC, Kicker: Allows periodic calibration of the oscillators of the AMIS-53000.

Table 65: Housekeeping Config - 0X1B [27]

Bit	Name	State	Comment
7	HK Interval Resolution	1	Five minute resolution setting
		0	One second resolution setting
6	Wake	1	Issue interrupt and enable clock to external host/controller
		0	
5	Write EE	1	Current register data written to EE (performed after all Cal's complete)*
		0	
4	Read INT ADC Channels	1	Temp sensor and battery inputs converted
		0	
3	Read EXT ADC Channels	1	EXT1 and EXT2 ADC inputs converted
		0	
2	Cal PLL	1	PLL calibration performed during housekeeping
		0	
1	Cal RC	1	RC oscillator calibration performed during housekeeping
		0	
0	Cal Kicker	1	Kicker calibration performed during housekeeping
		0	

Note: * Bit 5 is set high to allow the EE to be automatically written after a calibration is complete.

6.7.4.2. *Housekeeping Interval*

Sets the interval (time that the AMIS-53000 is in sleep mode) for the housekeeping routine.

Table 66: Housekeeping Interval - 0X1C [28]

Bit	Name	Comment
7:0	HK_INT [7:0]	Housekeeping interval = (HK_INT+1)* (HK interval resolution)

6.8 Idle Return

Table 67: Idle Return

Register			Function
Number (HEX)	Name	Code	
0X00	Command	0X04	In most conditions, the AMIS-53000 must be returned to idle mode at the end of a task by this command

This command is used to put the part back into idle mode. It should be used by the host to place the AMIS-53000 back into idle mode after the AMIS-53000 has interrupted the host for reception of a packet in Sniff, or to end a housekeeping cycle.

6.9 EE

The AMIS-53000 uses internal EE memory to store register settings (either default factory settings or user defined settings).

Table 68: Calibration Results

Register			Function
Number (HEX)	Name	Bits	
0X00	Command	0X05	Write the register contents to EE
		0X06	Read the contents of the EE
0X01	Status/Flag1	2	EE checksum status
0X1B	Housekeeping Config	5	Write register data to EE (auto after calibration complete)

6.9.1. Write EE

The serial interface provides a means to read and write the working registers of the AMIS-53000. To retain the information held by these registers, on-board EE is provided to store all of the register contents needed for operation. The write EE command copies the current contents of the working registers into EE, along with a CheckSum. The CheckSum is used to verify that the content of the EE is valid when the EE is dumped back into the registers.

6.9.2. Load EE

The load EE command will refresh the contents of the working registers with the values stored in EE, if the EE CheckSum is valid. If the EE CheckSum fails an error bit will be set in the Status2 register.

6.10 Calibrate

Table 69: Calibration Results

Register			Function
Number (HEX)	Name	Bits	
0X00	Command	0X07	Perform a Quick Start oscillator calibration
		0X08	Perform a 10kHz RC oscillator calibration
		0X09	Perform a PLL calibration
		0X0A	Perform a Quick Start oscillator calibration
0X01	Status/Flag1	6	TX PLL calibration status
		5	RX PLL calibration status
		4	10kHz RC oscillator calibration status
		3	Quick Start oscillator calibration status
0X1B	Housekeeping Config	2	Perform the PLL calibration
		1	Perform the 10kHz RC oscillator calibration
		0	Perform the kicker calibration
0X33	Kicker Slope Options	4	Kicker calibration status

Setup registers descriptions:

Trim- Shows the trim value for the circuit.

PLL Trim Target- Set a value that the PLL trim tries to achieve in calibration.

6.10.1. Internal Trim

6.10.1.1. Crystal Trim

Table 70: Crystal Trim - 0X21 [33]

Bit	Name	Comment
7:0	XTAL_TRIM [7:0]	24MHz internal trim caps; FF is max capacitance, 00 is min

6.10.1.2. LNA Trim

Table 71: LNA Trim - 0X22 [34]

Bit	Name	Comment
7:4	LNA_OUT[3:0}	LNA output tank cap trim F is max cap
3:0	LNA_IN [3:0]	LNA input shunt capacitor trim, F is max, 0 is min

6.10.1.3. Quick Start Oscillator Trim

This register contains the value of the trim from the self calibration.

Table 72: Quick Start Oscillator Trim - 0X23 [35]

Bit	Name	Comment
7:0	QS_TRIM [7:0]	Trim for the Quick Start (kicker), this register is written to by the calibration circuit

6.10.1.4. 10K Oscillator Trim

This register contains the value of the trim from the self calibration.

Table 73: 10kHz Oscillator Trim - 0X24 [36]

Bit	Name	Comment
7:0	RC_TRIM [7:0]	Trim for the 10kHz oscillator, this register is written by the calibration circuit

6.10.1.5. Analog Trim1

This is an internal use register with no user defined meaning. This register is set at the factory and changing the value will cause the AMIS-53000 to not operate.

6.10.1.6. Analog Trim2

This is an internal use register with no user defined meaning. This register value is set at the factory and changing the value will cause the AMIS-53000 to not operate.

6.10.1.7. RF PLL Trim

This register contains the value of the trim from the self calibration. This register is valuable to monitor to determine if the PLL trim calibration passed, but with the highest trim value or lowest trim value which indicates that the trim is nearly all the way to the edge of the calibration.

Table 74: RF PLL Trim - 0X27 [39]

Bit	Name	State	Comment
7			
6:4	TX Mode PLL Trim Value	111 -- 000	Max VCO trim value from the self calibration Min VCO trim value from the self calibration
3			
2:0	RX Mode PLL Trim Value	111 -- 000	Max VCO trim value from the self calibration Min VCO trim value from the self calibration

6.10.1.8. PLL Target Value

This register is used by the AMIS-53000 during self calibration. This is an internal use register with no user defined meaning.

6.10.2. Calibrate Quick Start Oscillator

The Quick Start oscillator must be calibrated prior to operations such as Sniff or Burst transmit. This command will perform an internal calibration of the oscillator, write the result to the Quick Start trim register, issue a calibration complete flag, as well as a calibration good/bad indicator. This command can be issued from any valid state that accepts changes in the instructions.

6.10.3. Calibrate 10kHz Oscillator

In any of the idle modes of operation, an internal 10kHz oscillator is used as the timekeeping reference for the interval timers. The calibrate 10kHz oscillator command will enable the crystal oscillator to create an accurate time base to use for the calibration of this oscillator, and then perform the calibration and store the result. A Cal done and status flag will be issued upon completion of the calibration. This command can be issued from any valid state that accepts changes in the instructions.

6.10.4. Calibrate PLL

Calibrate the PLL performs a calibration for the PLL in both transmit and receive mode. The PLL status register reports the calibration value for both modes, as well as the status for the calibration. This command can be issued from any valid state that accepts changes in the instructions.

6.10.5. Calibrate LNA

This command turns on the RF receiver chain and optimizes both the LNA output tuning structure and the LNA input matching trim for maximum signal level on RSSI. This is a calibration typically performed at board assembly in the presence of a known RF signal. The AMIS-53000 will auto-tune both the input and output internal variable capacitances of the LNA to optimize gain, compensating for the tolerance of external components for the match.

6.11 ROM 2 REGS

This command starts internal AMIS-53000 processes such as:

Multi-Channel: Calculates the frequency information to form nine channels of 300kHz bandwidth. Four of these channels are at higher frequencies than the programmed RF frequency and four channels are at lower frequencies.

Wave Shaping: Calculates the voltage steps to form the Gaussian wave shaping of the data for the data rate selected.

Defined Data Rates: Calculates all the parameters for the selected data rate (selected from the defined data rates).

RF Frequency: Calculates the parameters needed to set the TX/RX frequency

AM Filters: Calculates parameters for the filter defined by the data rate selection (defined data rates).

6.12 Chip Reset

Resets the entire chip, similar to a POR. This operation will reset the unlock test MUX register.

6.13 ADC Conversion

Table 75: ADC Configuration

Register			Function
Number (HEX)	Name	Bits	
0X00	Command	010xxxxx	Perform a single ADC conversion (see Table 84)
		110xxxxx	Perform continuous ADC conversions (see Table 85)
0X01	Status/Flag1	0	The ADC conversion has completed
0X1B	Housekeeping Config	4	Do an ADC conversion for the internal measurements
		3	Do an ADC conversion for the external measurements

The AMIS-53000 contains an 8 bit analog to digital converter. This ADC can measure the voltage on a number of internal functions, battery voltage, temperature, received signal strength indication voltage, and loop filter voltage. The results of these conversions are available through reading the registers where that data is stored or by using the feature of the Burst transmission to send that information to another node. The AMIS-53000 also contains two ADC channels available on the device pins. The ADC can convert signals at a conversion rate up to 128k samples/second.

Setup registers descriptions:

Temp- Contains the value from the last ADC of the internal temperature sensor.

Battery- Contains the value from the last ADC of the internal battery voltage (divided by 2).

RSSI- Contains the value from the last ADC of the signal level sample in the receiver.

ADC1- Contains the value from the last ADC of the external analog input.

ADC2- Contains the value from the last ADC of the external analog input.

Loop Filter- Contains the value from the last ADC of the loop filter voltage.

6.13.1. ADC Conversion Results

6.13.1.1. Temp ADC

Table 76: Temp ADC - 0X34 [52]

Bit	Name	Comment
7:0	TEMP_ADC [7:0]	Temperature sensor ADC reading

6.13.1.2. Battery ADC

Table 77: Battery ADC - 0X35 [53]

Bit	Name	Comment
7:0	BATT_ADC [7:0]	Battery voltage ADC reading (V_{batt}/2)

6.13.1.3. RSSI

Table 78: RSSI - 0X36 [54]

Bit	Name	Comment
7:0	RSSI_ADC [7:0]	RSSI voltage ADC reading

6.13.1.4. External Input 1 ADC

Table 79: External Input1 ADC - 0X37 [55]

Bit	Name	Comment
7:0	EXT1_ADC [7:0]	External input 1 ADC reading

6.13.1.5. External Input 2 ADC

Table 80: External Input2 ADC - 0X38 [56]

Bit	Name	Comment
7:0	EXT2_ADC [7:0]	External input 2 ADC reading

6.13.1.6. Loop Filter

Table 81: Loop Filter - 0X39 [57]

Bit	Name	Comment
7:0	LOOP_FILT [7:0]	Internal loop filter

6.13.2. Single ADC Conversion

The single conversion command performs an ADC conversion on the channel specified as part of the command. Once complete, a flag is set, and the 8 bit data for the conversion is available in its associated register.

Table 82: Single ADC Conversions

Register				Function
Number (HEX)	Name	Bits (7:6)	Bits (5:0)	
0X00	Command	01	000001	Perform an ADC on the external input 1
		01	000010	Perform an ADC on the external input 2
		01	000100	Perform an ADC on the internal temperature sensor
		01	001000	Perform an ADC on the Internal battery voltage
		01	010000	Perform an ADC on the receiver RSSI
		01	100000	Perform an ADC on the loop filter

6.13.3. Continuous ADC Conversion

This command can be given to the radio and operate in parallel with transmit or receive. This mode can also be entered into from an idle state. In this mode the specified ADC channel is continuously converted, and its associated register is continuously over written.

Table 83: Single ADC Conversions

Register				Function
Number (HEX)	Name	Bits (7:6)	Bits (5:0)	
0X00	Command	11	000001	Perform continuous ADC on the external input 1
		11	000010	Perform continuous ADC on the external input 2
		11	000100	Perform continuous ADC on the internal temperature sensor
		11	001000	Perform continuous ADC on the internal battery voltage
		11	010000	Perform continuous ADC on the receiver RSSI
		11	100000	Perform continuous ADC on the loop filter

7.0 Data Interface

Table 84: Control/Data Interface Physical Configuration

Interface	Function	Clock		Data		Select	AMIS-53000	Data Buffering
		Pin	Source	Output	Input			
I^2C	Control	SCLK	Master	SDATA	SDATA	None	Slave only	N/A
3 -Wire	Control	SCLK	Master	SDATA	SDATA	SSN	Slave only	N/A
	Data	DCLK	Master	DRXTX	DRXTX	DSSN	Master	Optional
		DCLK	Master	DRXTX	DRXTX	DSSN	Slave	Buffered only
4-Wire	Data	DCLK	Master	DRXTX	DOPT	DSSN	Master	Optional
		DCLK	Master	DRXTX	DOPT	DSSN	Slave	Buffered only

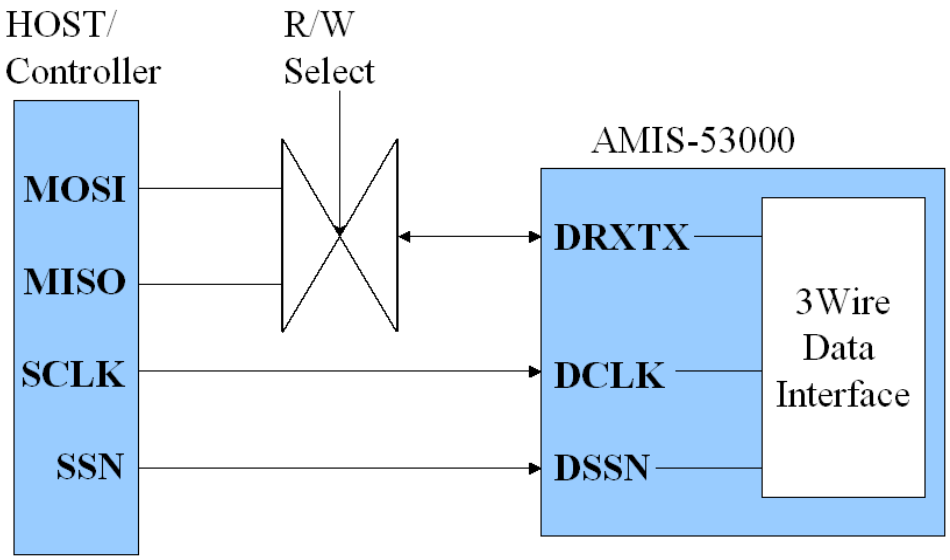


Figure 42: 4-Wire SPI Compatible Data Interface

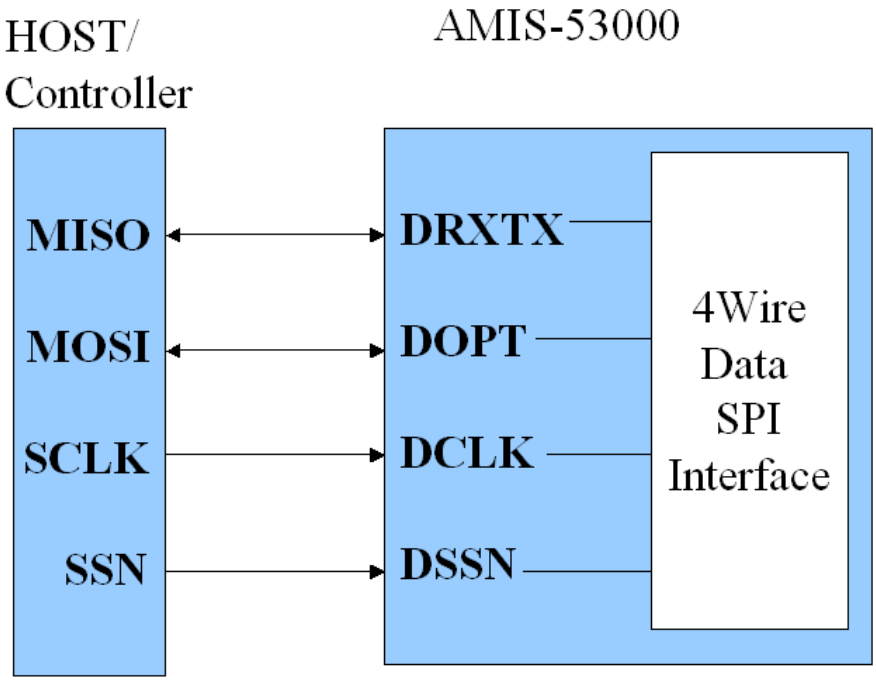


Figure 43: 3-Wire Serial Data Interface

The AMIS-53000 employs two different data interfaces. Transmit and receive data is exchanged with an external controller through either a 3-wire or a 4-wire SPI like interface. Selecting the interface, 3-wire or 4-wire is done by writing to bit 7 of the general options B register.

- SPI serial data interface
- 3-wire serial data interface
- AMIS-53000 can be the slave or master

Setup registers descriptions:

Chip Address- Allows a unique value to be transmitted and received with the data packet to identify a unique radio.

Fixed Data Rates- Select the options for one of several fixed data rates.

General Options A- Configure the interface options.

General Options B- Configure the interface options.

Start of Frame- Set a code value that indicates the start of a data packet.

Preamble Length- Select a type of preamble and set the length in bits. (see Section 6.6.3)

Custom Data Rates- Configure parameters for data rates that are not one of the fixed data rates.

CRC Polynomial- Value of the CRC polynomial.

Default Length of Packet- Set a default length for packets.

Broad Cast ID- A general chip ID allowing for transmissions to be received by all radios.

7.1.1. Chip Address MSB1

The 16 bit ID that can be used for several purposes in the AMIS-53000 is stored in the chip address MSB, and chip address LSB registers.

Table 85: Chip Address1 - 0X03 [3]

Bit	Name	Comment
7:0	Chip_Add [15:8]	Upper byte of chip address

7.1.2. Chip Address LSB

Table 86: Chip Address0 - 0X04 [4]

Bit	Name	Comment
7:0	Chip_Add [7:0]	Lower byte of chip address

7.1.3. Data Rate/Format

The data rate/format register is used to select the data rate and format for both receive and transmit. The DDRATE[2:0} option bits allow selection of one of eight pre-programmed data rates. When one of the discrete data rates is selected, the ROM2REGS command is used to load clock and data recovery settings for the desired data rate into their associated registers.

The Manchester option bit configures the AMIS-53000 to transmit and receive in the Manchester encoded format, while the data interface remains NRZ.

If a data rate other than one of the available discrete rates is desired, the user should set the use custom bit, and then program the custom data rate register for the desired data rate. When the use custom data rate option is enabled, it is up to the user to set the correct sample clock frequency in the CDR options B register, set clock recovery loop filter settings, and if using the PLL based FSK detector, set the PLL detector loop filter.

Note: For data rates that are near one of the pre-defined data rates, a discrete data rate could first be chosen, the ROM2REGS command given to load all of the settings for the various blocks for that data rate, and then the custom data rate option enabled and the new data rate information entered.

For example, if the desired data rate is 100kbps, set DDRATE to 110 for 96kbps operation. Next, issue the ROM2REGS command in the command register. All of the proper settings for the clock and data recovery circuit for a 96k data rate will be loaded into the working registers from ROM (sample clock frequency, clock recovery loop filter settings). Finally, enable the use custom option, and program data rate 1, and 0 with the value for a 100k data rate.

Custom frequency is set in data rate 1 and data rate 0. If custom is 0, ROM contents for selected discrete data rate are loaded into data rate 1 and data rate 0.

Table 87: Data Rate/Format - 0X0B [11]

Bit	Name	State	Comment
7	NU		
6	NU		
5	NU		
4	Use Custom	1	Enables user programmable data rate
		0	
3	Manchester	1	Manchester encoding selected
		0	NRZ encoding selected
2:0	DDRATE [2:0]	000 001 010 011 100 101 110 111	1.2kbps 2.4kbps 4.8kbps 9.6kbps 19.2kbps 57.6kbps 96kbps 128kbps

7.1.4. General Options A

The general options A register contains a number of options that specify the operation of the part in its various modes.

Standby Mode: Determines whether the crystal oscillator is enabled during standby. For applications relying on the AMIS-53000 to provide and external host/controller with a system clock, this bit should be enabled, and is the default state.

POR State: Specifies the power on state of the device. Once this has been stored into EE, the device will power up in the chosen state after the EE has been shadowed into the working registers.

Pull up Disable: For applications not using an open drain type driver to drive the register interface pins (SDATA, SCLK and SSN) the pull ups on these pins can be disabled via this option bit to save power.

Temperature Compensation: When enabled, the ADC output for the temperature sensor is used to compensate the RF center frequency for crystal frequency error. A new correction factor is calculated each time the ADC performs a new conversion on the temperature sensor.

CRC Enable: Enables internal CRC checking in RX, and appends a CRC in TX.

Length of Packet Enable: Allows buffering of packets, also allows CRC when enabled.

Use ID in RX and TX: When enabled, in receive mode the part will not output data until a valid ID is found, and in TX, the part will automatically send preamble and chip ID before enabling the data interface.

Table 88: General OptionsA - 0X0C [12]

Bit	Name	State	Comment
7	Use ID in RX and TX	1	Wake on ID in RX, send ID in TX
		0	
6	Length of Packet Enable	1	Enables the part to frame packets
		0	
5	CRC Enable	1	Enables CRC (packet length must be enabled)
		0	
4	Temperature Compensation	1	RF center frequency temperature compensation enabled
		0	Temperature compensation is disabled
3	Pull up Disable	1	Pull ups on IIC clock and data and SSN pins disabled
		0	
[2:1]	POR State	00 01 10 11	Standby Idle RX TX
0	Standby Mode	1	Crystal only mode, system clock output active
		0	Low-power standby mode

7.1.5. General Options B

General options B contains more option bits for the general setup and operation of the AMIS-53000.

System Clock Output Frequency: Sets the frequency of the output clock on the SYSclk pin when enabled.

RXTX Sampling Edge: Specifies which edge of DCLK should be used to sample the RXTX pin.

Auto Increment Disable: When enabled, a multiple address read or write command on the register interface will read/write only the address given in the command multiple times.

Data Interface Clock Frequency: Sets the clock frequency for the data interface when the AMIS-53000 is configured to be the master of the data interface. For modes in which the AMIS-53000 does not buffer the packet, the interface speed will always be the data rate, regardless of this setting.

Data Interface Slave/Master: Specifies whether the AMIS-53000 is the master or slave for the data interface.

4-Wire Data Interface: Enables the 4-wire SPI data interface. When low, RXTX is bi-directional.

Table 89: General OptionsB - 0X0D [13]

Bit	Name	State	Comment
7	4-Wire Data Interface	1	Enabled
		0	
6	Data Interface Slave/Master	1	AMIS-53000 is slave
		0	AMIS-53000 is master, clock speed determined by bits 5, 4
5,4	Data Interface Clock Frequency	11 10 01 00	1MHz 500kHz 100kHz Baud clock
3	NU		
2	RXTX Sampling Edge	1	Data bits are sampled on the rising edge of DCLK on the interface
		0	Data bits are sampled on the falling edge of DCLK on the interface
1,0	System Clock Output Frequency	11	12MHz (24MHz external crystal)
		10	6MHz (24MHz external crystal)
		01	3MHz (24MHz external crystal)
		00	Off

7.1.6. Start of Frame

The start of frame byte is transmitted when this register is non-zero. It's used as an aid for the receiver clock and data recovery circuit in modes where the fast phase alignment feature is enabled.

Table 90: Start of Frame - 0X19 [25]

Bit	Name	Comment
7:0	SOF [7:0]	8-bit code sent prior to chip ID in TX and Burst

7.1.7. Data Rate 1

The data rate 1 and data rate 0 registers are used to set user defined data rates. These registers are loaded from ROM when a discrete data rate is selected. The following equation is used to calculate the value for CUST_DR:

$$\text{CUST\_DR} = \text{DataRate} \cdot \frac{2^{22}}{F_{\text{sample\_clock}}}$$

where DataRate is the desired data rate, and F_{sample_clock} is the frequency selected for the sample clock. This register is loaded with the discrete rate if selected.

Table 91: Data Rate1 - 0X29 [41]

Bit	Name	Comment
7:0	CUST_DR [15:8]	Upper byte of user defined data rate/discrete data rate

7.1.8. Data Rate 0

Table 92: Data Rate0 - 0X2A [42]

Bit	Name	Comment
7:0	CUST_DR [7:0]	Lower byte of user defined data rate/discrete data rate

7.1.9. CRC Polynomial

This register allows a designer to change the CRC Polynomial used in the AMIS-53000. The register represents the presence of the powers in the CRC equation. For example:

The Polynomial x8+x5+x2+x+1 is encoded by assuming the polynomial will always have a high order bit.

So the binary representation is: 1 0010 0111

This is set as the value 0X27 (HEX) in the register

(See "Koopman, P. & Chakravarty, T., " Ccylic Redundancy Code (CRC) Polynomial Selection For Embedded Networks" DSN04, June 2004." for more information.)

Table 93: CRC Poly - 0X30 [48]

Bit	Name	Comment
7:0	CRC_POLY [7:0]	CRC polynomial value

7.1.10. Default Length of Packet

This register allows a default value for the LOP (5 bytes) such that the AMIS-53000 does not have to send the LOP with a buffered packet.

Table 94: Default LOP - 0X31 [49]

Bit	Name	Comment
7:0	DEFAULT_LOP [7:0]	Default value for the length of packet to be used in buffered TX/RX

7.1.11. Broadcast ID 1

Many applications in the wireless market make use of a broadcast function where the master note in a system can transmit to all wireless nodes in the network without addressing each node individually, but still not broadcasting to nodes in another network.

Table 95: Broadcast ID1 - 0X3A [58]

Bit	Name	Comment
7:0	Global_ID1 [7:0]	Lower byte of the global address

7.1.12. Broadcast ID 0

Table 96: Broadcast ID0 - 0X3B [59]

Bit	Name	Comment
7:0	Global_ID0 [7:0]	Upper byte of the global address

7.2 TX/RX Data Interface Protocol

The AMIS-53000 TX/RX data format can be streaming data where the transmitter transmits each bit of data as it is received or it can be packetized. Packetized data can be in packets up to 256 bytes. Packetized data can add a preamble, start of frame, identification code, length of packet, and CRC error CheckSum.

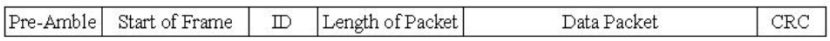


Figure 44: Data Protocol Format

- Streaming or packetized data
- Buffer size is 256 byte maximum
- Packet overhead

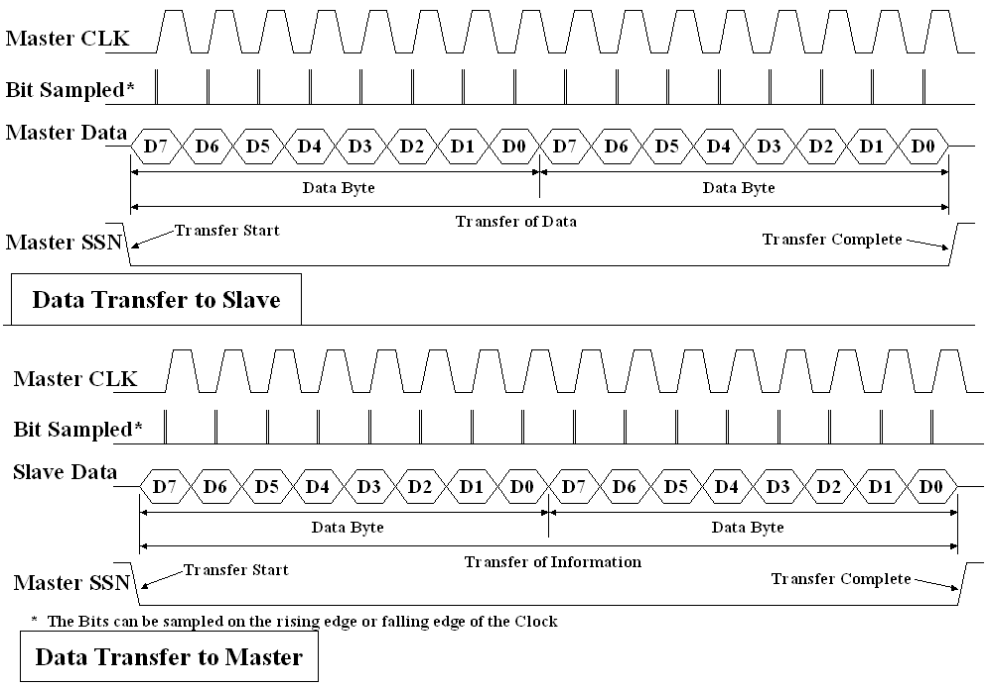


Figure 45: 3-Wire Data Transfer Protocol

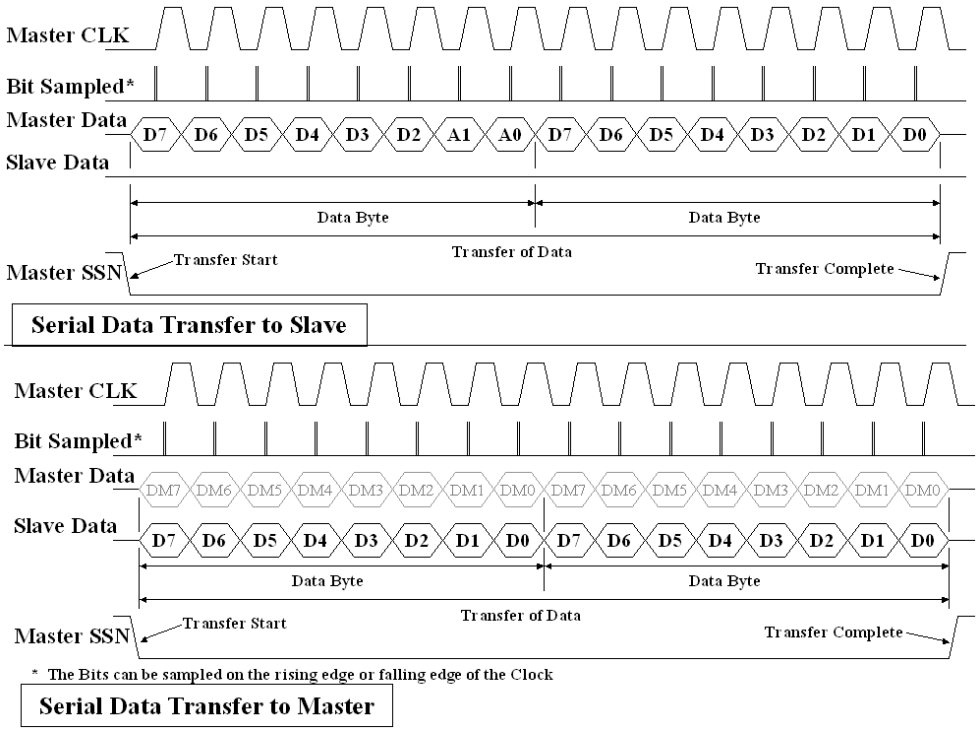


Figure 46: 4-Wire Data Transfer Protocol

Table 97: TX/RX Data Protocols

Modulation	Detector	CDR	Preamble	SOF	ID/LOP/CRC	Slice
AM	RSSI	Opt[1]	CW	Yes[2]	See Table 98	Fixed/Auto
FM (<20kbps)	PLL	Yes	1 0 pattern	-------	See Table 98	----------
FM (>20kbps)	FFT	Yes	[3]	[4]	See Table 98	----------

Notes:
1. The use of the CDR function to recover the data is recommended for AM/OOK modulation.
2. The SOF for AM modulation is suggested to be 55 (HEX) for NRZ and 0A (HEX) for Manchester encoded data.
3. The preamble for FM (FFT) with NRZ data is a 1 0 repeating pattern. The preamble for FM (FFT) with Manchester encoded data is all 1s or all 0s.
4. A SOF is only required for FM (FFT) when the data is Manchester encoded. The suggested SOF is a pattern of 55 (HEX) or AA (HEX).

Table 98: Interface Data Protocols

TX/RX Data Protocol		Interface Data Protocol		Comments
LOP	CRC	Interface	Data	
N	N	Active	Stream[1]	Data is streamed out the interface as it is received
N	N	Active*	Stream	* Data is streamed out the interface starting with the wakeup on ID
Y	N	Interrupt	Buffered	An interrupt is issued when data reception is complete
Y	Y	Interrupt	Buffered	An interrupt is issued when data reception is complete

Notes:
1. When the interface uses streaming data, the AMIS-53000 must be the master.

The serial data interface for the AMIS-53000 can be configured to be a 3-wire interface or a 4-wire SPI interface. The AMIS-53000 can be configured to act as a master or a slave for both receive and transmit operation. Bit 2 in the general options B register allows the user to select whether DATA will be sampled on the rising, or falling edge of DCLK. The setting for the sampling polarity applies to all modes.

Table 99: Serial Data Interface Configuration

General Options B			Data Port Configuration						
Bit 7	Bit 6	Bit 2	# Port Pins	AMIS-53000	Edge Sample	Pin Function Definition			
						DCLK	DSSN	DRXTX	DOPT
0	0	X	3	Master	X	Output	Output	I/O	X
0	1	X	3	Slave	X	Input	Input	I/O	X
1	0	X	4	Master	X	Output	Output	Output	Input
1	1	X	4	Slave	X	Input	Input	Output	Input
X	X	0	X	X	Falling				
X	X	1	X	X	Rising				

7.2.1. AMIS-53000 in Master Mode

In receive mode, the DSSN pin will transition low when the AMIS-53000 has received data. Immediately following the transition of DSSN, the AMIS-53000 will provide a synchronized bit clock on DCLK, and the received data will appear on DRXTX.

In transmit mode, the transition of DSSN is used to signal an external host/controller that the AMIS-53000 is ready for transmit data and is ready to receive that data on the DRXTX pin. Immediately following the transition of DSSN, the AMIS-53000 will provide a synchronous clock on DCLK for the host/controller to use for loading transmit data into the AMIS-53000.

7.2.2. AMIS-53000 in Slave Mode

The AMIS-53000 cannot be the slave for streaming data. The requirements of adding header information such as preamble or SOF requires that the AMIS-53000 be in control of the data interface transfer. The receiver has similar requirements with removing the header information.

As the slave for the data interface, the AMIS-53000 will simply issue an interrupt to the external host indicating data is available after a data packet has been received.

For buffered transmit operation, the AMIS-53000 will issue an interrupt indicating it is ready to load the packet. After the packet is received by the AMIS-53000, the transmitter is enabled, any packet formatting is done and the packet is sent.

7.2.3. Manchester Operation

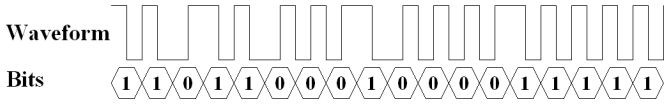


Figure 47: Manchester Coded Data

If the Manchester option is selected in the data rate and format register, the AMIS-53000 will internally encode and decode both transmit and receive data respectively. The format for the signal interface remains NRZ in this mode.

7.2.4. Packet Framing

Three options bits located in the general options A register determine the method with which the transceiver will process packets: use ID, length of packet (LOP) enable and cyclic redundancy check (CRC) enable. An additional bit in the TX config register enables the buffered TX mode of operation.

Table 100: Register Configuration Bits

General Options A			TX Config		SOF	Use	Comments
Bit 7	Bit 6	Bit 5	Bit 3	Bit 2	All		
0	X	X	X	X	X	No ID	
1	X	X	X	X	X	ID	
X	0	X	X	X	X	No LOP	
1	1	X	X	X	X	LOP/ID	The ID must be enabled with LOP for data alignment
X	X	0	X	X	X	No CRC	
1	1	1	X	X	X	CRC/ID/LOP	
X	1	X	1	X	X	Buffer/LOP	TX must have LOP enabled when using data buffering
X	X	X	0	X	X	No Buffer	
X	X	X	X	0	X	Chip ID	
X	X	X	X	1	X	Global ID	
X	X	X	X	X	0x00	No SOF	
?	X	X	X	X	All other	SOF	Certain configurations require SOF to detect ID byte

7.2.5. Use ID

Table 101: ID

Register			Function
Number (HEX)	Name	Bits	
0X0C	General Options A	7	Wake on ID in RX/send ID with TX
0X0F	TX Config	2	Select either the chip ID or global ID to be used in transmissions
0X16	Burst Config	3	Send ID with Burst packet

The chip ID is a 16 bit word which can be programmed in registers 3 and 4. In receive mode, when the use ID bit in general options A is set, the AMIS-53000 will not begin exporting or buffering data until a valid ID matching the value stored in the chip address registers is received. The ID is used in more advanced modes of operation for byte alignment. In addition to waking on its own unique ID, the AMIS-53000 will also wake on a pre-defined global chip ID. The default value for the global ID is in the register table. This value can be overwritten, but is not stored in EE so care must be taken when overwriting the value.

With the use ID bit enabled in transmit mode, the AMIS-53000 will transmit the chip ID prior to enabling the data interface. An additional option bit in the TX config register allows selection of either the chip ID or global ID value for transmit.

In either transmit or receive, when the use ID bit is enabled without LOP enabled, the AMIS-53000 will not buffer data. Hence when enabled stand alone, the data interface must be configured with the AMIS-53000 as the master.

7.2.6. Length of Packet Enable

The length of packet enable (LOP) bit located in general options A, enables the AMIS-53000 to buffer packets. The use ID bit must be used in conjunction with LOP to allow the receiver to byte align on incoming data.

In receive mode with the LOP enabled, the AMIS-53000 will interpret the first byte following either a valid chip ID, or global ID to be the length of the incoming packet. This byte specifies the number of bytes following the LOP to be received (non-inclusive of the CRC if enabled). When enabled, the AMIS-53000 will buffer the incoming packet into internal RAM. Following reception of the last byte of the packet, an interrupt is issued on the interrupt pin, and depending on the configuration of the data interface, the packet will either be sent out of the data interface by the AMIS-53000 as master, or wait for the external host/controller to stream the packet out as the master.

Having the LOP enabled in transmit mode allows for the use of the buffered TX packet option in transmit, or the AMIS-53000 can still act as master and process the packet on the fly. With LOP enabled, and buffered TX disabled, the AMIS-53000 must be the master for the data interface. In this mode, the preamble and chip ID (or global ID) will be sent before the data interface is activated. Once the DSSN is pulled low by the AMIS-53000, the first byte received into the part is expected to be the LOP byte. Transmission continues until the AMIS-53000 has determined that all bytes have been received, at which point the data interface is disabled, and the AMIS-53000 will return to standby. When buffered TX is enabled, after the transmit instruction is given to the AMIS-53000, an interrupt from the AMIS-53000 will be issued indicating the part is ready to load in the data packet. The actual loading of the data packet depends on the data interface setup as to whether the AMIS-53000 is master or slave. The first byte is again expected to be the LOP byte. After the complete packet is loaded into the radio, the RF will be enabled, the preamble and chip ID transmitted, followed by the packet. After completion of the transmission, the AMIS-53000 will return to standby.

7.2.7. CRC Enable

The CRC enable located in general options A is the final tier of intelligence for the AMIS-53000 packet handling capability. In order for the AMIS-53000 to do CRC checking, this option must be used in conjunction with both use ID and LOP enable. Operation of the interface for both receive and transmit with the CRC enabled is no different from that explained under the LOP enabled section. With the CRC enabled, the AMIS-53000 will append the calculated CRC in transmit as the last byte. In receive mode, interrupts to the external controller will only be issued for packets passing the CRC.

7.2.8. SOF Byte

Table 102: Suggested SOF

Modulation	Detector	Coding	Preamble	SOF
AM	RSSI	NRZ	CW	55 (HEX)
		Manchester	CW	0A (HEX)
FM (<20kbps)	PLL	1 0 pattern	1 0 pattern	Not required
FM (>20kbps)	FFT	NRZ	Repeating 1/0	Not required
		Manchester	All 1's or 0's	55 (HEX) or AA (HEX)

Depending on whether the mode of operation is AM or FM, NRZ or Manchester, it may be necessary for a SOF byte to precede the chip ID. This byte is user programmable, and is used to ensure proper CDR operation and bit alignment prior to reception of the chip ID. When the contents of the SOF byte register are loaded to any non-zero value, this byte will be transmitted prior to the chip ID. For modes not requiring the SOF byte, setting this register to 00h will prohibit transmission of this byte. More information on when the SOF byte is required is in the clock and data recovery section.

7.2.9. Timing Diagrams for Various Packet Framing Modes

7.2.9.1. Use ID Enabled, No CRC, No Packet Length

Table 103: Receive

Parameter	Action
ID	Data interface immediately ready after ID detected
No LOP	Radio stays in RX until instructed to change
	Data is shifted out data port as received
No CRC	Error checking is not performed and CRC is not attached to packet

Table 104: Transmit

Parameter	Action
Transmit	Transmit command immediately powers the transmitter on
	Transmits preamble
ID	Transmits the ID
	Starts data interface and uses a synchronous clock to clock in the TX data (master only)
	Transmits each bit as received
	Transmitter returns to standby after transmission complete

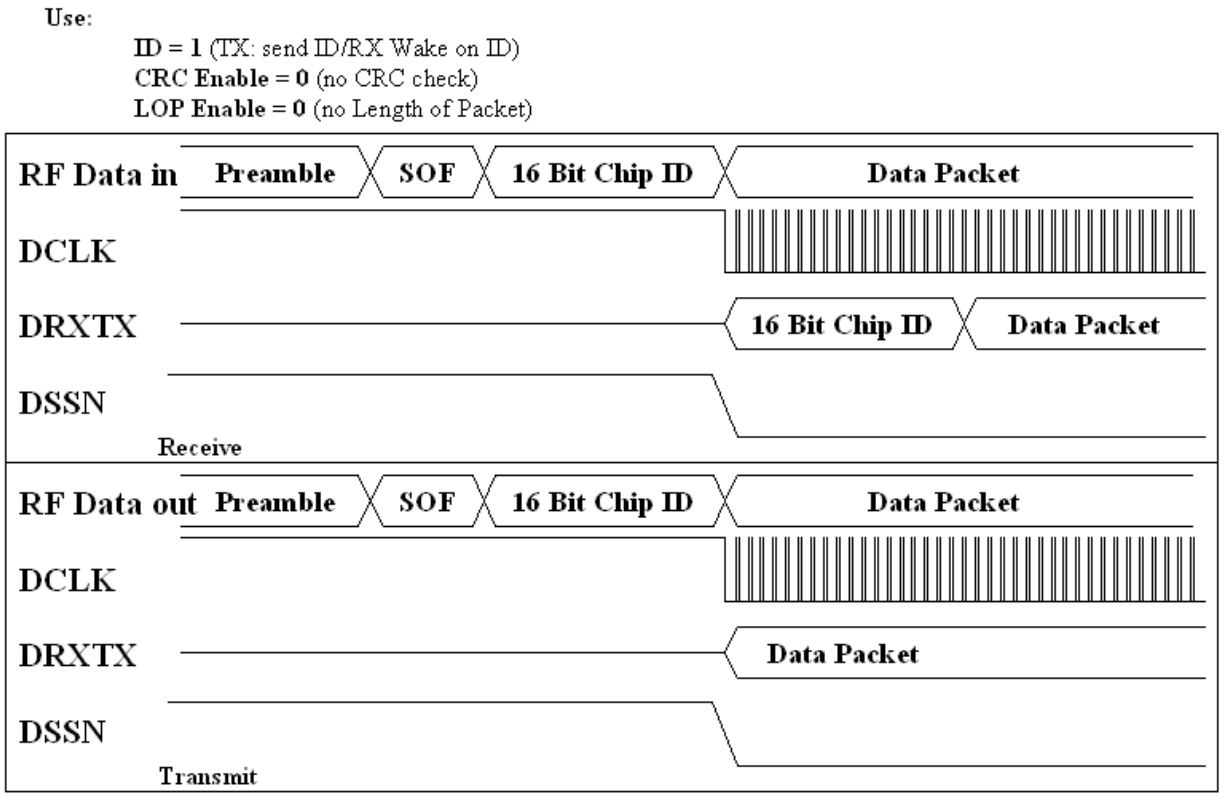


Figure 48: Data Interface Protocol (ID only)

7.2.9.2. Use ID Enabled, No CRC, LOP Enabled

Table 105: Receive

Parameter	Action
ID	Data interface immediately ready after ID detected
LOP	Receiver loads rest of packet into buffer memory
	After last data byte is received, radio returns to the previous state
	An interrupt is issued to the external controller/microprocessor
	Data is transferred out the port with the AMIS-53000 as master or the external controller as master
No CRC	Error checking is not performed and CRC is not attached to packet

Table 106: Transmit

Parameter	Action
Buffered Transmit	If buffered transmit is selected, the AMIS-53000 will open the data interface and transfer all TX data into memory with AMIS-53000 as master or external controller as master
Transmit	Transmit command (or end of TX data transfer) immediately powers the transmitter on
	Transmits preamble (length of preamble as specified)
ID	Transmits the SOF and the ID
	Starts data interface and uses a synchronous clock to clock in the TX data (master only) or clocks data out of memory (buffered TX)
	After the packet is transmitted, the transmitter returns to standby state

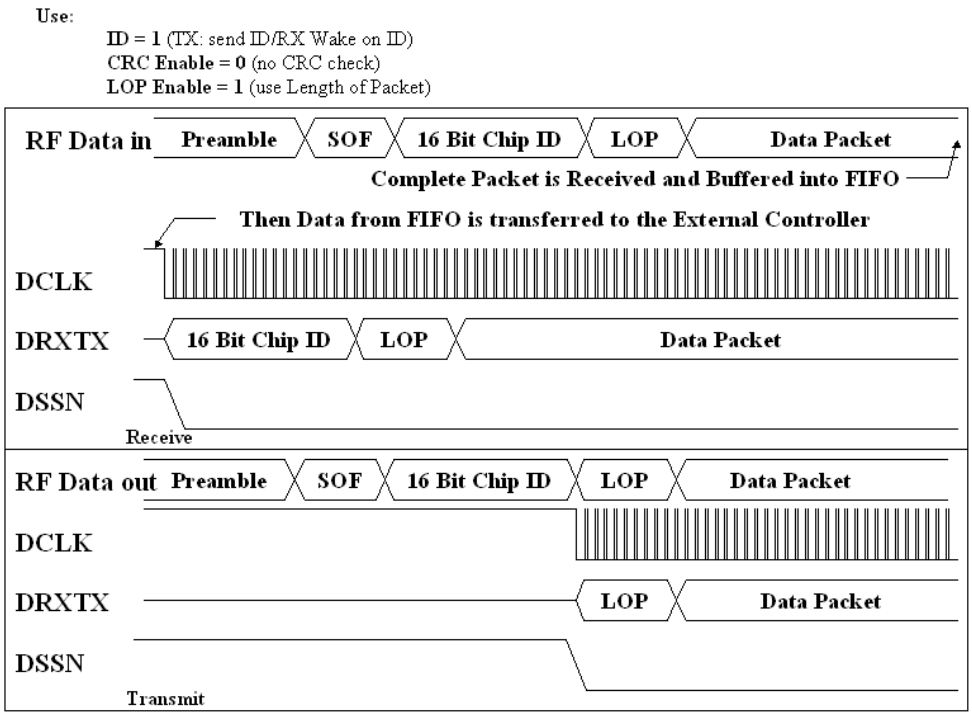


Figure 49: Data Interface Protocol (ID and LOP)

7.2.9.3. Use ID Enabled, CRC Enabled, LOP Enabled

Table 107: Receive

Parameter	Action
ID	Data interface immediately ready after ID detected
CRC	As soon as the ID is validated, the CRC starts processing the data
LOP	The LOP is received
	The rest of the received data packet is buffered into memory
CRC Invalid	The last byte is the CRC and if invalid, the receiver waits for a command from the external host/controller, or if the receiver came from idle it will return to receive
CRC Valid	Receiver returns to previous state and an interrupt is issued to the external controller
	The data interface is started and the data is sent to the controller, except for the CRC

Table 108: Transmit

Parameter	Action
Buffered Transmit	If buffered transmit is selected, the AMIS-53000 will open the data interface and transfer all TX data into memory with AMIS-53000 as master or external controller as master
Transmit	Transmit command (or end of TX data transfer) immediately powers the transmitter on
	Transmits preamble (length of preamble as specified)
ID	Transmits the SOF and the ID
CRC	The CRC begins processing the data with the ID
	Starts data interface and uses a synchronous clock to clock in the TX data (master only) or clocks data out of memory (buffered TX)
LOP	The first byte is defined to be the LOP of the packet
CRC Byte	At the end of the packet, the data stops and the CRC value is sent
	After the packet is transmitted, the transmitter waits for a command from the external host/controller

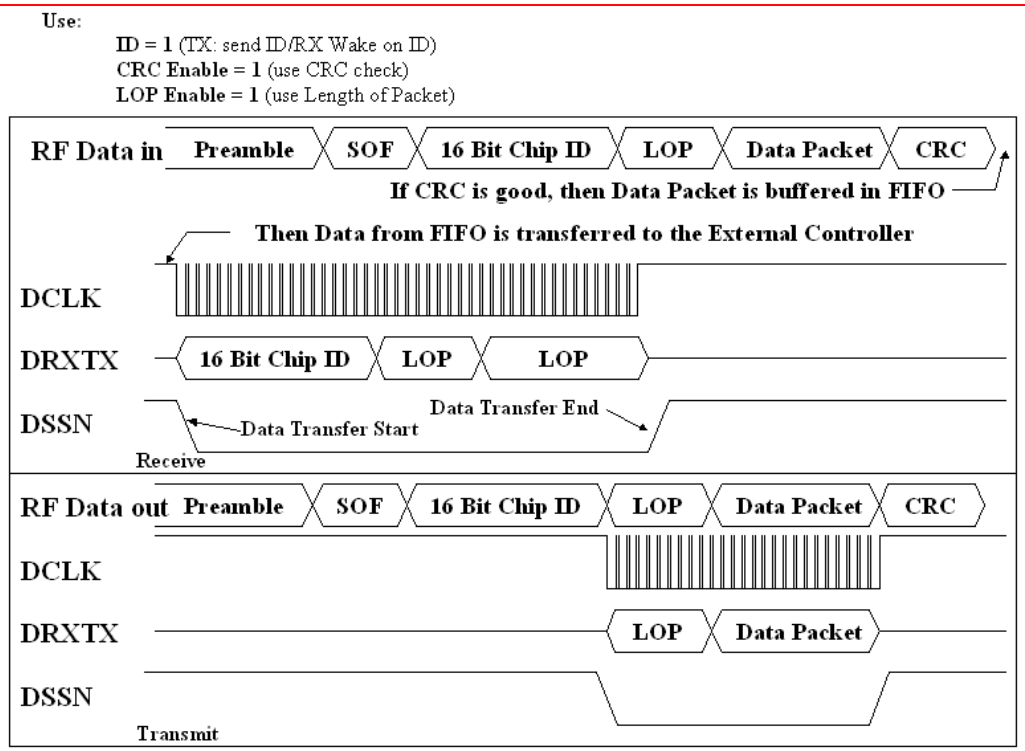


Figure 50: Data Interface Protocol (ID, LOP and CRC)

8.0 General System Functions

8.1 Pull up Disable

The AMIS-53000 includes built in pull-up resistors for use with the I^2C operation to reduce the overall system component count. The pull ups are asserted at POR until mode selection occurs. If mode is determined to be 3-wire, the pull ups are removed. If mode is determined to be I^2C, this option bit determines whether the pull ups are to be removed.

Table 109: I^2C Pull Up Control

Register			Function
Number (HEX)	Name	Bits	
0X0C	General Options A	3	Disable internal pull up resistors on I^2C bus

8.2 Brown-Out POR

The brown-out POR serves two purposes. The first is to provide a POR signal to reset the digital when power is initially applied to the part. The second is to provide a POR should the voltage on the supply drift below normal operating range to prevent a brown-out condition.

Table 110: Power-on-Reset Start Up State

Register			Function
Number (HEX)	Name	Bits	
0X0C	General Options A	2,1	00 Standby
			01 Idle
			10 RX
			11 TX

8.3 Temperature Sensor

The temperature sensor is created by using a Darlington pair of PNP transistors. The two transistors create a 5mV/°C slope that can be sensed with an analog to digital converter. Without amplification, an 8 bit ADC with a 2V reference voltage will have a resolution better than two degrees.

The temperature sensor can be trimmed to an accuracy of 3°C. As the trim is increased, the output voltage also increases.

The temperature voltage relationship is given by:

$$V = 1.1172 - T \cdot 0.00531$$

Where V is the output voltage and T is the temperature in Celsius.

Setup registers descriptions:

ADC Temperature- Register shows the value of the temperature sensor ADC. (See Section 6.13.1.1)

8.3.1. Crystal Temperature Compensation

An on-chip temperature sensor combined with an on-chip A/D and a look-up table enable the part to maintain RF frequency accuracy within ± 2.5ppm over all operating voltages and temperatures (-45°C to 85°C). This function can be enabled via configuration bit 4 located in general options A. When this function is enabled, a new calculation for the center frequency word will be performed whenever the temperature sensor storage register is updated with a new value. Therefore it is possible to update the compensation value either in housekeeping, as part of a Burst transmit cycle, or as controlled externally by issuing the instruction to perform an ADC measurement of the temp sensor.

Table 111: RF Frequency Temperature Compensation

Register			Function
Number (HEX)	Name	Bits	
0X0C	General Options A	4	Enable RF frequency temperature compensation

8.4 Software

The version of the AMIS-53000 is written to a register at the end of the manufacturing process. This code can help AMIS wireless product support when there is an issue with the AMIS-53000.

Setup registers descriptions:

AMIS ID- Register contains a code showing the version of the AMIS-53000.

8.4.1. AMIS Part Revision Code

Table 112: AMIS Part Revision Code - 0X41 [65]

Bit	Name	Comment
7:0	AMIS_ID [7:0]	Revision status of the AMIS-53000

9.0 Built-in Test Functions

The AMIS-53000 has a number of test registers. These registers are not available to the general user of the AMIS-53000. However, many of these registers control test features that are useful in the development of applications using the AMIS-53000.

Setup registers descriptions:

Test Unlock- A special code is required to unlock the functions of the test registers.

Test- Registers that route signals to pins for monitoring or turn internal circuits off for test.

9.1 TM Unlock Register

The developer designing the AMIS-53000 may desire to use some of the test modes to monitor the operation of the AMIS-53000 or to determine the activity of some parameter. These registers are locked from use by a code word. To unlock the test registers contact AMIS wireless product support to obtain the code. Enter this code in the unlock register to access the test registers. This register will be reset with a reset of the part and thus will lock the user out of the test registers.

Setup registers descriptions:

Test Unlock- Register contains a code about the state the AMIS-53000 is operating in.

** Registers with the ** mark can be trimmed if the test registers are unlocked.

Table 113: Test Unlock Code - 0X40 [64]

Bit	Name	Comment
7:0	UNLOCK [7:0]	Code to unlock operation of the test registers (contact AMIS for the code to unlock the test register functions)

9.2 Test Registers

The following registers allow for signals to be routed to pins for monitoring. They also turn functions in the AMIS-53000 on and off for measuring the operational parameters of the AMIS-53000.

9.2.1. IF Amp Manual Trim A

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.2. IF Amp Manual Trim B

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.3. PLL Manual Trim

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.4. PLL Test Modes

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.5. Power Down RF Sections

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.6. Analog Test Mode

Digital Pad Test: All digital pads except system clock out, and xInterrupt are 1mA I/O with pull ups and Schmitt triggers. The SYSclock and xInterrupt pads are 2mA outputs.

Auto Increment Disable: This disables the automatic incrementing of the I^2C register addresses. It can allow repeated writes to the same register, useful for adjusting a parameter to optimize its value.

Table 114: Analog Test Mode - 0X47 [71]

Bit	Name	State	Comment	
7	CAP_TRIM	1	Enable the test mode for determination of capacitance trim value	
		0		
6	Pipe ADC1 to Data Filter	1	Enable the ADC1 input channel as a direct input to the data filter	
		0	Normal operation	
5	Brown-Out Power Down	1	Override the brown-out POR to allow test at any voltage	
		0		
4	Auto Increment Disable	1	Address increment disabled (IIC only)	
		0		
3		1		
		0		
2	Ignore XTAL Control	1	Ignore crystal control (digital clock gating)	
		0		
1	Dig Pad Test A	1	Enabled: Input	Enabled: Corresponding output
			SSSN DClock DSSN xBurst	Doptional RXTX xINT sysClk
		0	Disabled	
0	Dig Pad Test B	1	Enabled: Input	Enabled: Corresponding output
			Doptional xBurst RXTX	SSSN xINT DSSN
		0	Disabled	

9.2.7. RF Test Modes

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.8. Analog Test MUX

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.9. RF Test MUX

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.10. Digital Test MUX A

Table 115: Digital Test MUX A - 0X4B [75]

Bit	Test Pin	Comment				
7:4	MUX to SCLK	1111 - 0000	1111	Space Q channel CLK	0111	Energy dwell enable
			1110	Mark Q channel CLK	0110	PLL increment
			1101	NC	0101	TX enable
			1100	Data Q channel	0100	10kHz clock
			1011	PN code from ΣΔ	0011	Software state [3]
			1010	Start	0010	Bandgap ready
			1001	Analog data out	0001	ADC CLK
			1000	PLL detect/data out	0000	Normal/system clock
3:0	MUX to Dopt	1111 - 0000	1111	Space I channel CLK	0111	Code dwell enable
			1110	Mark I channel CLK	0110	PLL decrement
			1101	PLL detect/NCO out	0101	Kicker
			1100	Energy detected	0100	PLL Z
			1011	Data I channel	0011	Software state [2]
			1010	RF PLL CLK feedback	0010	PLL xReset
			1001	Is locked (encoder)	0001	ADC power down
			1000	TX data	0000	D optional

9.2.11. Digital Test MUX B

Table 116: Digital Test MUX B - 0X4C [76]

Bit	Test Pin	Comment				
7:4	MUX to xINT	1111 - 0000	1111	Encoder in	0111	Cal done kicker
			1110	Decoder in	0110	PLL in range
			1101	Sniff	0101	INT0
			1100	ΣΔ output	0100	Transmit done
			1011	RF PLL (reference CLK)	0011	Software state [1]
			1010	Brown-out output	0010	Xtal on
			1001	Receive done	0001	ADC done
			1000	TS CLK	0000	xInterrupt
3:0	MUX to xBurst	1111- 0000	1111	Recovered clock	0111	PA enable
			1110	Decoder out	0110	PLL cal timer overflow
			1101	Encoder out	0101	PLL cal enable
			1100	CDR enable	0100	xtal PD
			1011	Baud clock (CDR out)	0011	Software state [0]
			1010	CRC failed	0010	isStopMode
			1001	RX enable	0001	Watch dog reset
			1000	NC	0000	SSN normal mode

9.2.12. Digital Test MUX C

Table 117: Digital Test MUX C - 0X4D [77]

Bit	Test Pin	Comment				
7:4	MUX to Data SSN	1111 - 0000	1111	Encoder in	0111	RAMBist bad
			1110	Decoder in	0110	EE BIST done
			1101	EE BIST good	0101	EE BIST bad
			1100	EE low voltage detect	0100	Busy
			1011	CPENA	0011	Instruction enable
			1010	ROM BIST done	0010	Bandgap power down
			1001	ROM BIST bad	0001	XTAL
			1000	RAM BIST done	0000	Data SSN normal mode
3:0		1111- 0000				

9.2.13. Digital Test Mode A

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.14. Digital Test Mode B

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.15. Digital Test Mode C

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.16. Digital Test Mode D

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.17. Memory Test Mode Address

This register is used for factory testing of the AMIS-53000 and has no user functions.

9.2.18. Memory Test Mode Data

This register is used for factory testing of the AMIS-53000 and has no user functions.

10.0 Register Definition

Table 118 below contains the address for all of the internal registers. Once the EE has been written, the POR states for the registers become the data last written. Should the CheckSum fail, all registers will return to the POR state shown, and an error flag will be written to a status register.

Table 118: Register List

R/W	Address		Register Name	Description	POR State	EE	Section
	Hex	Dec					
R/W	0x00	0	Command	Instruction register	0000_0000		6.2
R/W	0x01	1	Status1	Part status, flags	0000_0000		6.4.5.1
R/W	0x02	2	Status2	Part status, flags	0000_0000		6.4.5.2
R/W	0x03	3	Chip Address 1	Upper 8 bits of chip address	0000_0000	X	7.1.1
R/W	0x04	4	Chip Address 0	Lower 8 bits of chip address	0000_0000	X	7.1.2
R/W	0x05	5	RF Divider	Integer portion of RF frequency	0000_0000	X	6.4.1.1
R/W	0x06	6	RF Frequency 2	Upper 8 bits of RF fraction	0000_0000	X	6.4.1.2
R/W	0x07	7	RF Frequency 1	Center 8 bits of RF fraction	0000_0000	X	6.4.1.3
R/W	0x08	8	RF Frequency 0	Lower 8 bits of RF fraction	0000_0000	X	6.4.1.4
R/W	0x09	9	Peak Deviation 1	Upper 8 bits of FM deviation	0000_0000	X	6.4.1.5
R/W	0X0A	10	Peak Deviation 0	Lower 8 bits of FM deviation	0000_0000	X	6.4.1.6
R/W	0x0B	11	Data Rate / Format	Set discrete data rate and encoding option	0000_0000	X	7.1.3
R/W	0x0C	12	General Options A	General options for interface, POR state, etc.	0000_0000	X	7.1.4
R/W	0x0D	13	General Options B	General options for interface, POR state, etc.	0000_0000	X	7.1.5
R/W	0x0E	14	RX Config	Receiver options	0000_0000	X	6.5.1.1
R/W	0x0F	15	TX Config	Transmit options	0000_0000	X	6.6.1
R/W	0x10	16	Idle Config	Idle mode options		X	6.7.1
R/W	0x11	17	Sniff Config	Sniff Mode options	1011_0100	X	6.7.2.1
R/W	0x12	18	Sniff Interval	Interval between Sniff cycles	0000_1010	X	6.7.2.2
R/W	0x13	19	Energy Dwell Time	Length of time to dwell in Sniff Mode	0000_0000	X	6.7.2.3
R/W	0x14	20	Code Dwell Timer	Number of bit times to wait for code after energy	0000_0000	X	6.5.1.5
R/W	0x15	21	Energy Threshold	Threshold for wake on RSSI, Sniff and CCA	0000_0000	X	6.5.1.2
R/W	0x16	22	Burst Config	Burst transmit options	0000_0000	X	6.7.3
R/W	0x17	23	Burst Interval	Interval timer for burst transmit	0001_1000	X	6.7.3.1
R/W	0x18	24	Output Power	Output power	0001_0000	X	6.6.2
R/W	0x19	25	Start of Frame	Byte used for burst transmit/CDR wake up	0001_0000	X	7.1.6
R/W	0x1A	26	Preamble Length	Length of CW, or '10' repeated in Burst/TX (BT's)	0001_0000	X	6.6.3
R/W	0x1B	27	HK Config	Housekeeping options register		X	6.7.4.1
R/W	0x1C	28	HK Interval	Interval timer for housekeeping		X	6.7.4.2
R/W	0x1D	29	Slice Threshold	Energy threshold for AM DAC mode data slice		X	6.5.1.4
R/W	0x1E	30	Filter/Slice	AM/RSSI filter setting and AM slice mode		X	6.5.1.4
R/W	0x1F	31	CDR Options A	Clock and data recovery options A		X	6.5.1.5
R/W	0x20	32	CDR Options B	Clock and data recovery options B	1000_0000	X	6.5.1.5
R/W	0x21	33	Crystal Trim	Crystal trim	0000_0000	X	6.10.1.1
R/W	0x22	34	LNA Trim	LNA input and output matching trim	0000_0000	X	6.10.1.2
R/W	0x23	35	Quick Start Trim	Quick Start oscillator trim	0000_0000	X	6.10.1.3

Table 118: Register List (Continued)

R/W	Address		Register Name	Description	POR State	EE	Section
	Hex	Dec					
R/W	0x24	36	10k Osc Trim	10kHz oscillator trim	0000_0000	X	6.10.1.4
	0x25	37	Analog Trim	Bandgap and temp sensor trim	0000_0000	X	6.10.1.5
	0x26	38	Analog Trim 2	Capacitance trim	0010_0100	X	6.10.1.6
	0x27	39	RF PLL Trim	PLL calibration storage register	0100_0100	X	6.10.1.7
	0x28	40	RF PLL Options	RF PLL options register	0000_0000	X	6.4.1.7
	0x29	41	Data Rate 1	User defined data rate upper bits	0000_0000	X	7.1.7
	0x2A	42	Data Rate 0	User defined data rate lower bits	0000_0000	X	7.1.8
	0x2B	43	PLL Loop Co	User defined PLL detector bandwidth	0000_0000	X	6.5.1.4
	0x2C	44	CDR Loop Co	User defined clock recovery loop	0000_0000	X	6.5.1.5
	0x2D	45	User Data	Transmitted on normal interval burst	0000_0000	X	6.7.3.2
	0x2E	46	User Data	Transmitted on interrupt triggered Burst		X	6.7.3.3
	0x2F	47	TargNumWakeUps	Target number of wake ups for		X	6.7.2.4
	0x30	48	CRCPoly	CRC polynomial register		X	7.1.9
	0x31	49	DefaultLOP	Default LOP register		X	7.1.10
	0x32	50	Checksum	EEPROM checksum		X	6.9.1
	0x33	51					
	0x34	52	Temp ADC	Storage register for the temp sensor reading	0000_0000		6.13.1.1
	0x35	53	Battery ADC	Storage register for the battery reading	0000_0000		6.13.1.2
	0x36	54	RSSI ADC	Storage register for the RSSI reading	0000_0000		6.13.1.3
	0x37	55	EXT1 ADC	Storage register for the EXT1 input	0000_0000		6.13.1.4
	0x38	56	EXT2 ADC	Storage register for the EXT2 input	0000_0000		6.13.1.5
	0x39	57	Loop Filter				6.4.1.8
	0x3A	58	Global Chip ID1				7.1.11
	0x3B	59	Global Chip ID0				7.1.12
	0x3C	60	Software State				6.4.5.3
	0x3D	61					
	0x3E	62					
	0x3F	63					
	0x40	64	Unlock Reg		1010_0101		9.1
	0x41	65	AMIS ID Code		0011_0001		8.4.1
	0x42	66	IF Amp Trim A				9.2.1
	0x43	67	IF Amp Trim B				9.2.2
	0x44	68	Manual PLL Trim				9.2.3
	0x45	69	PLL Test Mode				9.2.4
	0x46	70	PDtestRF				9.2.5
	0x47	71	Analog Test Mode				9.2.6
	0x48	72	RFTM				9.2.7
	0x49	73	Analog Test Mux				9.2.8
	0x4A	74	RF Test Mux				9.2.9
	0x4B	75	Digital Test Mux A		0000_0000		9.2.10
	0x4C	76	Digital Test Mux B		0000_0000		9.2.11
	0x4D	77	Digital Test Mux C		0000_0000		9.2.12
	0x4E	78	DTM A		0000_0000		9.2.13
	0x4F	79	DTM B		0000_0000		9.2.14
	0x50	80	DTM C		0000_0000		9.2.15
	0x51	81	DTM D				9.2.16
	0x52	82	MTM Address				9.2.17
	0x53	83	MTM Data				9.2.18
	0x54	84	PLLCalTarget	PLL calibration target value	0000_0000		6.10.1.8

11.0 Applications

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12.0 Ordering Information

Table 119: Ordering Information

Ordering Code	Product Name	Package Type	Operating Temperature Range	Industry Application	Differentiating Feature	Shipping Configuration
19608-001-XTP (or –XTD)	AMIS-53000-I/A	32 LQFP	-40C to 85C	Industrial, Automotive, Other	Extra Low Power	Tape & Reel (-XTP); Tubes (-XTD)
19608-002-XTP (or –XTD)	AMIS-53000-I/A	32 LQFP	-40C to 85C	Industrial, Automotive, Other	SPI Interface; Ganged Transceivers	Tape & Reel (-XTP); Tubes (-XTD)
19637-001-XTP (or –XTD)	AMIS-53000-M	32 LQFP	-40C to 85C	Medical	Extra Low Power	Tape & Reel (-XTP); Tubes (-XTD)
19637-002-XTP (or –XTD)	AMIS-53000-M	32 LQFP	-40C to 85C	Medical	SPI Interface; Ganged Transceivers	Tape & Reel (-XTP); Tubes (-XTD)

13.0 Company or Product Inquiries

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