Contents

1. AP2011 Specification

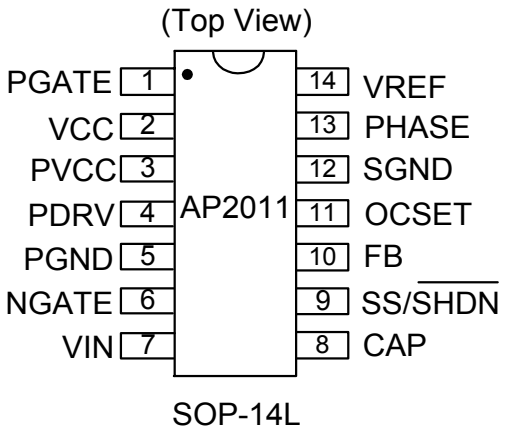
1.1 Features

- Single 10V to 40V Supply Application
- 1.25V ± 2.0% Voltage Reference.
- Virtual Frequency Control™.
- Fast transient response.
- Synchronous operation for high efficiency
- Current limit function.
- Small size with minimum external components
- Soft Start and Shutdown functions
- Industrial temperature range
- Under Voltage Lockout function
- SOP-14L **Pb-Free** package

1.2 General Description

The AP2011 integrates Pulse-width-Modulation (PWM) control circuit into a single chip, mainly designs for power-supply regulator. All the functions included an on-chip 1.25V reference voltage, a smart auto modulated oscillator, UVLO, SCP, circuitry, and synchronous PWM controller circuit. Recommend the output CE transistors as pre-driver for Driving externally. Switching frequency can be adjustable by Virtual Frequency Control™. During low VCC situation, the UVLO makes sure that the outputs are off until the internal circuit is operational normally.

1.3 Pin Assignments

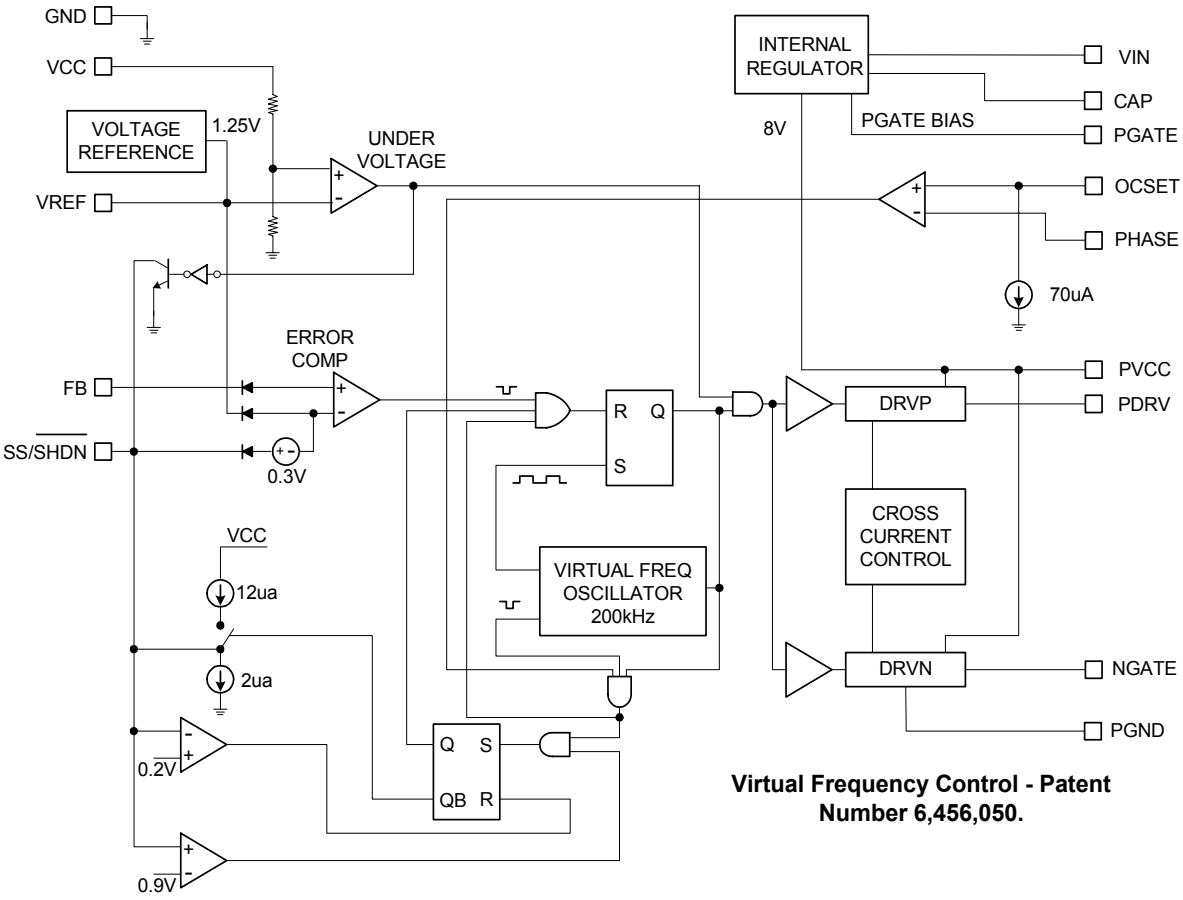


SOP-14L

1.4 Pin Descriptions

Pin Name	No.	Description
PGATE	1	Level shift-gate driver
VCC	2	Internal regulator voltage
PVCC	3	Power VCC
PDRV	4	PMOS Gat driver
PGND	5	Power Ground
NGATE	6	Low side driver output (N MOSFET)
VIN	7	Chip supply voltage
CAP	8	Charge pump pin
SS/$\overline{\text{SHDN}}$	9	Soft start, a capacitor to ground sets the slow start time/set low for shutdown function.
FB	10	Feedback input
OCSET	11	Sets the converter over-current trip point
SGND	12	Signal Ground
PHASE	13	Input from the phase node between the MOSFETs
VREF	14	Reference voltage

1.5 Block Diagram



AP2011 FUNCTIONAL BLOCK DIAGRAM

1.6 Absolute Maximum Ratings

Symbol	Parameter	Range.	Unit
V_{IN}	VCC to GND	0 to 42	V
V_{PHASE}	PHASE to GND	0 to 42	V
Θ_{JC}	Thermal Resistance Junction to Case	60	°C/W
Θ_{JA}	Thermal Resistance Junction to Ambient	150	°C/W
T_{OP}	Operating Temperature Range	-40 to +85	°C
T_{ST}	Storage Temperature Range	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering) 10 Sec.	300	°C

2. Hardware

2.1 Introduction

AP2011 is a high efficiency and high performance synchronous PWM controller. With using one P-channel MOSFET and one N-channel MOSFET to be the synchronous switch, AP2011 can make the system operating in more than 92% efficiency situation. There are a lots of function built inside in AP2011 like programmable current limit, UVLO, soft-start, shutdown, reference voltage, voltage clamping for high input voltage, and the most important function is the Virtual Frequency Control™, which make the frequency modulated automatically by the input and output voltage of the system. The functions' description will show in each section to let user know how to define the outside circuit.

2.2 Description of the built-in function

- **Programmable Current Limit Control**

The programmable current limit control circuit is designed for engineer who needs to control the limit current to avoid too large system current. The current limit set pin (OCSET) just needs to add an outside resistor between VCC and OCSET pin, which resistor can make a voltage drop to VCC with the internal current source (70uA). This voltage drop will compare with the voltage drop of PWM waveform (Phase pin waveform) because the voltage drop of PWM is made by output current and P-channel MOSFET RDSON, so we can limit the output current by this formula:

$$I_{LOAD} \times R_{DS(on)-PMOS} = I_{OCSET} \times R_{OCSET}$$

If the comparator detected the PWM high voltage level is under the OCSET pin voltage level, it will sent turn off signal to shutdown the PWM control and SS pin will discharge the outside capacitor with a 2uA current. After SS pin voltage lower than 0.2V, AP2011 will reset to make PWM and start to charge SS pin. If SS pin charges to 0.9V but PWM still lower than OCSET voltage, then the comparator will send the signal to shutdown PWM again.

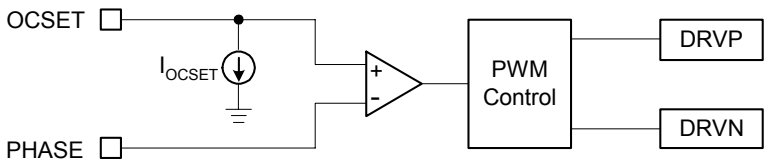


Figure 1. Programmable Current Limit Control Circuit

Under Voltage Lock Out (UVLO)

The circuit shown in Figure 2 is a simple explanation of UVLO function. VCC voltage will make that two resistors get a compared voltage with VREF. AP2011 is designed for UVLO voltage is 6.5V, and recovery voltage is 6.8V (that 0.3V voltage is depend on the offset voltage of the comparator). If VCC voltage is lower than 6.5V, the separate voltage of those two resistors is under 1.25V, than that comparator will send low level signal to SS pin to shutdown AP2011. And if VCC is higher than 6.8V, that comparator will send high level signal to SS and AP2011 will start to enter normal operation mode.

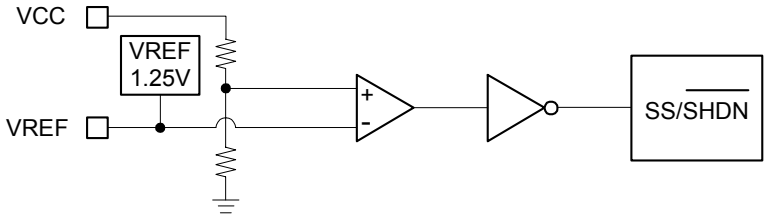


Figure 2. Under Voltage Lock-Out circuit

Soft-Start and Shutdown (SS/$\overline{\text{SHDN}}$)

The circuit shown in Figure 3 is about soft-start and shutdown function. If outside system force SS pin always under 0.2V, AP2011 will turn into shutdown mode and turn off the PWM. When SS pin higher than 0.2V, PWM will turn on to drive outside MOSFET, but now PWM duty is depend on the comparison of SS and FB. According to SS pin raising curve, FB will follow this curve until SS reaches to VREF + 0.3V, and then PWM duty will turn to depend on the comparison of VREF and FB.

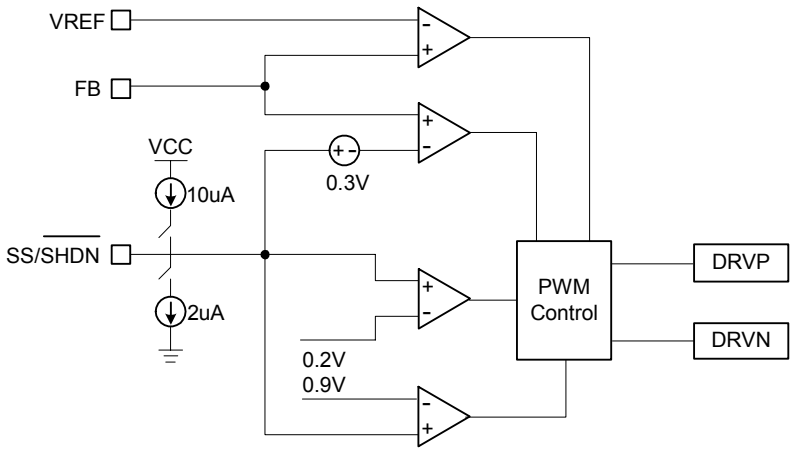


Figure 3. Soft-start and Shutdown circuit

Voltage Clamping for High Input Voltage

Normally the MOSFETs AP2011 used can be bought easily, but always the easy-buying parts have 25V V_{GS} maximum rating. If we use AP2011 in more than 25V input voltage system, we need a voltage clamping function for protecting the MOSFETs. AP2011 is built-in a 8V voltage drop circuit to clamp the voltage between V_{IN} to PGATE, and NGATE to GND. This 8V voltage will show in PVCC pin to GND and make P_{DRV} to PGATE always keep a V_{IN}-8V voltage. In this function's operation, first we add a capacitor outside in CAP pin (Figure. 4), AP2011 will make a current to charge the outside capacitor by the resistor. And if that charging current is large enough to make the voltage of that resistor larger than V_{BE} of the PNP, the PNP will turn on and have I_{CE} passing through. This current will be mirrored to make charging current of C_{BOOST}. We need choose a suitable capacitor for CAP pin to make sure that charging current is enough for C_{BOOST}. If Ccap value is not enough, the P channel MOSFET may conduct a large short-through current during supply transition.

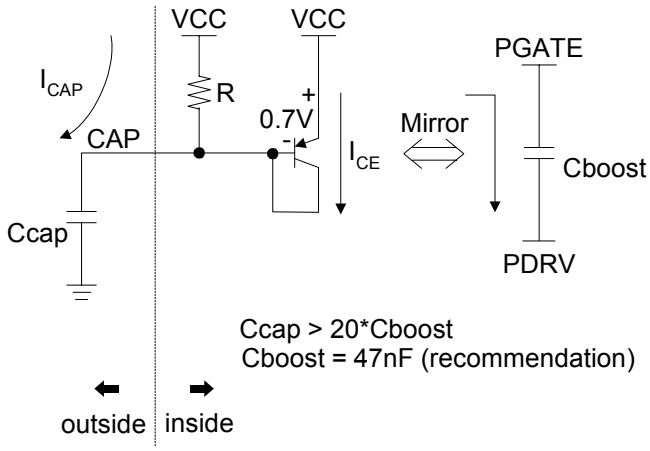
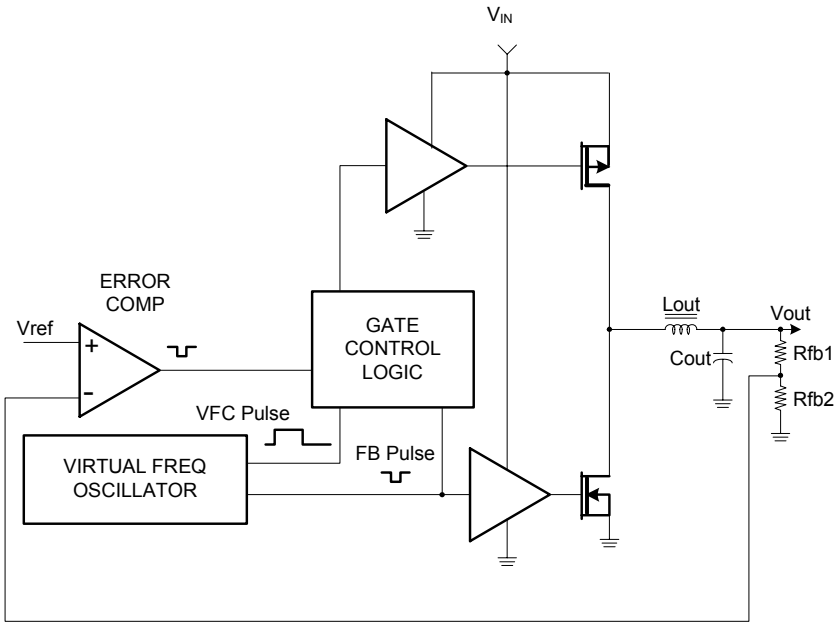


Figure 4. Voltage Clamping Function Circuit

Virtual Frequency Control

Virtual Frequency Control™ combines the advantages of constant frequency and constant off-time control in a single mode of operation. This allows fix frequency, precision switching voltage regulator control with fast transient response and the smallest solution size. Switch duty cycle can be adjusted from 0% to 100% on a pulse by pulse basis when responding to transient conditions. Both 0% and 100% duty cycle operation can be maintained for extended periods of time in response to load or line transients. Figure 5 depicts a simplified operation of the Virtual Frequency Control technique: The VFC oscillator generates a pulse of a known duration (VFC_Pulse). The regulator loop responds by returning a complementary feedback pulse (FB_Pulse). The FB_Pulse duration is a result of external conditions such as inductor size, the voltage

across the inductor and the duration of the VFC_Pulse. A VFC control loop is then formed whereby the duration of the VFC_Pulse is modified as a result of the FB_Pulse duration. The VFC loop arrives at a state of equilibrium, where the operating frequency remains inherently constant.



$$D_{ON} > 0.1,\ 240\text{-}50 \times (1\text{-}\ \frac{V_{OUT}}{V_{IN}})\ \text{-}\ V_{IN}$$

$$D_{ON} < 0.1,\ \frac{10000 \times\ V_{OUT}/\ V_{IN}}{5.9\ \text{-}\ 0.01V_{IN}}$$

Figure 5: Virtual Frequency Control Loop-

Synchronous single supply application.

Virtual frequency control is a technique that provides stable, constant frequency of operation for pulse controlled architectures such as constant off-time/on-time. This is all done internal to the IC with minimal number of components and without the need for connections to external terminals such as input and/or output. No external compensation is required, thus providing a low cost, high performance fix frequency solution for switching voltage regulators.

Virtual Frequency Control is a trademark of PWRTEK, LLC.

2.3 Schematic

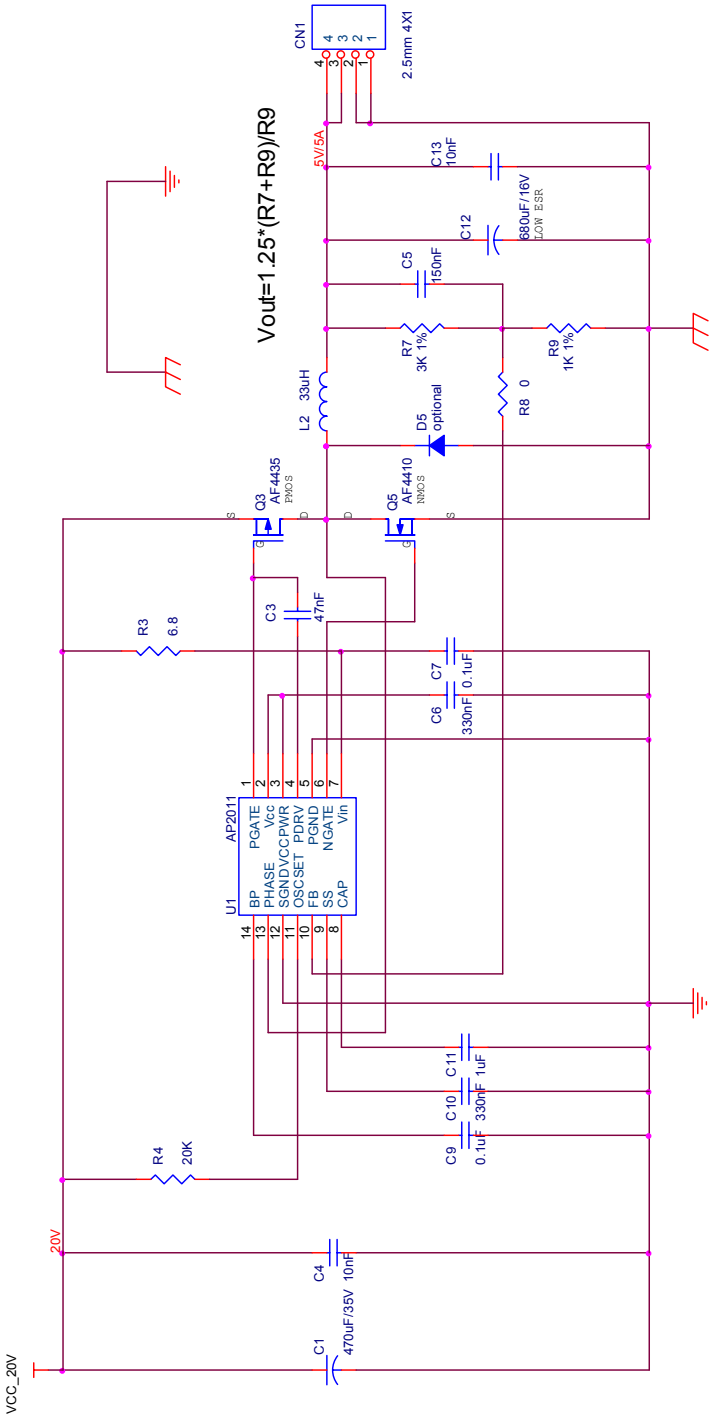


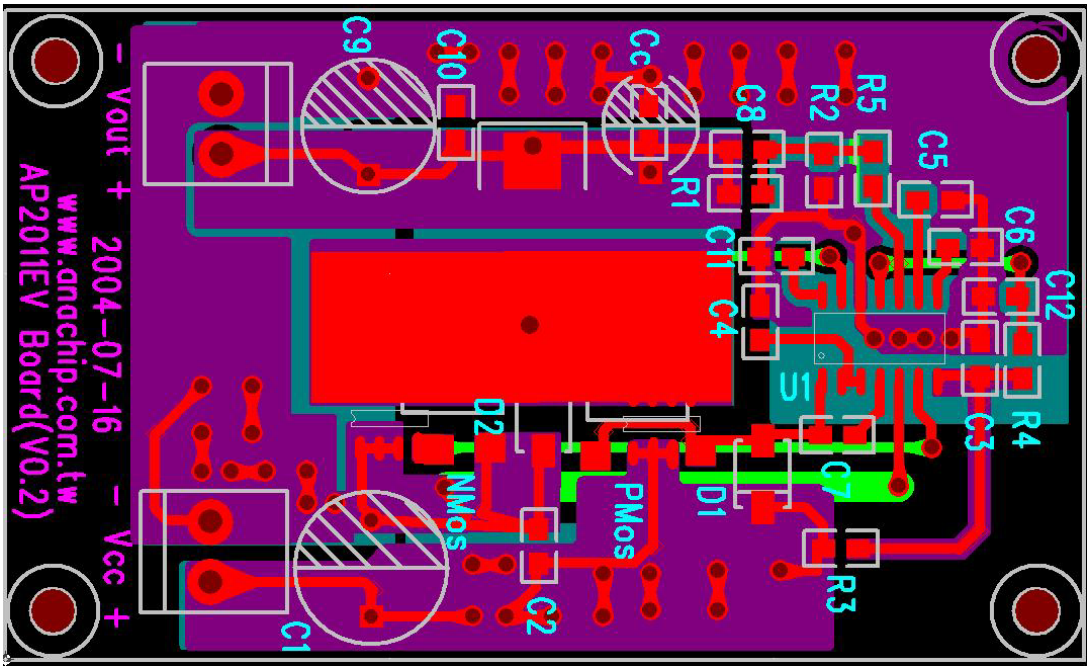
Figure 5. AP2011 Application Circuit

2.4 Board of Materials

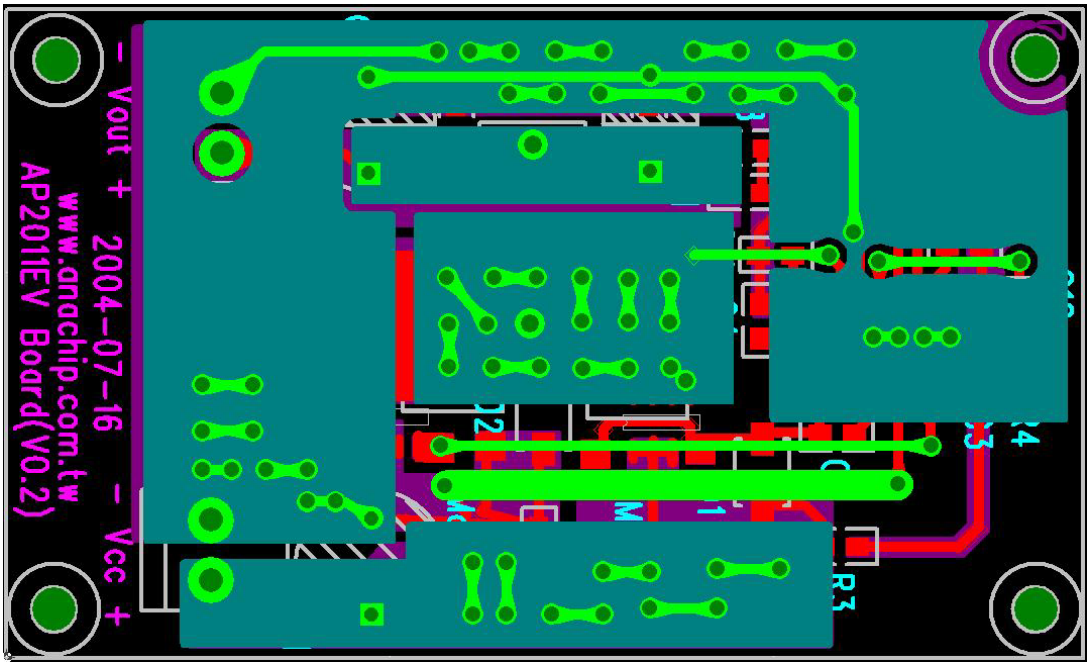
No.	Value	Q'ty	Part Reference	Description	Manufacturers	Part Number
1	AP2011	1	U1	AP2011	Anachip	AP2011
2	470uF/35V	1	C1	Low ESR	OST	
3	47nF/50V	1	C3	0805 ceramic SMD capacitor	Viking Tech	
4	10nF/50V	2	C4, C13	0805 ceramic SMD capacitor	Viking Tech	
5	150nF/50V	1	C5	0805 ceramic SMD capacitor	Viking Tech	
6	330nF/50V	2	C6, C10	0805 ceramic SMD capacitor	Viking Tech	
7	0.1uF/50V	2	C7, C9	0805 ceramic SMD capacitor	Viking Tech	
8	1uF/50V	1	C11	0805 ceramic SMD capacitor	Viking Tech	
9	680uF/16V	1	C12	Low ESR	OST	
10	6.8	1	R3	1% 0805 SMD resistor	Viking Tech	
11	3K	2	R4, R7	1% 0805 SMD resistor	Viking Tech	
12	1K	1	R9	1% 0805 SMD resistor	Viking Tech	
13	0	1	R8	1% 0805 SMD resistor	Viking Tech	
14	SB340	1	D5	optional		
15	33uH	1	L2	ring core inductor 5A	Viking Tech	
16	AF4435	1	Q3	30V 10A P-MOSFET	Anachip	
17	AF4410	1	Q5	30V 10A N-MOSFET	Anachip	
18	Connecter		CN1			

2.5 Board Layout

Top Side



Bottom Side



3. Design Procedure

3.1 Introduction

The AP2011 integrated circuit is a synchronous PWM controller, it operates over a wide input voltage range. Being low cost, it is a very popular choice of PWM controller. This section will describe the AP2011 design procedure. The operation and the design of this application will also be discussed in detail.

3.2 Operating Specifications

Specification	Min	Typ	Max	Units
Input Voltage	18	20	22	V
Output Voltage	4.9	5	5.1	V
Operating Frequency	160	180	200	KHz
Output power	0	25	30	W

Table 1. Operating Specifications

3.3 Design Procedures

This section describes the steps to design synchronous buck converter, and explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop.

- **Synchronous buck converter**

Example calculations accompany the design equations. Since this is a buck output system, this example calculations apply to the converter with output power is 60W and input voltage set to 25V, unless specified otherwise. The first quantity to be determined is the converter the duty cycle value.

$$\text{Duty ratio} \quad D = \frac{V_o + V_{DS(sat),N}}{V_{IN} - V_{DS(sat),P} + V_{DS(sat),N}} = \frac{T_{on}}{T_s} \quad , \quad 0 \leqq D \leqq 1$$

Assuming the low-side N-channel MOSFET switch-on voltage $V_{DS(sat),N}$ = 0.1 V, the high-side P-channel MOSFET switch on voltage $V_{DS(sat),P}$ = 0.1V and V_o = 5V. In this case the duty cycle for V_{IN} = 20V is 0.255 for 5V/5A output system.

Inductor Selection

The inductor plays a central role in the proper operation of the buck circuit. To find the inductor value it is necessary to consider the inductor ripple current. Choose an inductor to maintain continuous-mode operation down to 10 percent ($I_{o(min)}$) of the rated output load:

$\Delta I_L = 2 \times 10\% \times I_o = 2 \times 0.1 \times 5 = 1A$

The inductor "L_B" value for this system is connected to be:

$$L_B \geqq \frac{(V_{in} - V_{ds(sat)} - V_o) \times D_{min}}{\Delta I_L \times f_s} = \frac{(25 - 0.1 - 12) \times 0.484}{1 \times (180 \times 10\text{^}3)} = 21\mu H$$

So we choose buck inductor value to be 33uH for this case, and if the core loss is a problem, increasing the inductance of L will be helpful.

Output Capacitor Selection

A. The output capacitor is required to filter the output and provide regulator loop stability. When selecting an output capacitor, the important capacitor parameters are; the 100KHz Equivalent Series Resistance (ESR), the RMS ripples current rating, voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter. The ESR can be calculated from the following formula.

$$ESR = \left(\frac{V_{RIPPLE}}{2 \times I_{LOAD(\min)}} \right)$$

An aluminum electrolytic capacitor's ESR value is related to the capacitance and its voltage rating. In most case, higher voltage electrolytic capacitors have lower ESR values. Most of the time, capacitors with much higher voltage ratings may be needed to provide the low ESR values required for low output ripple voltage. If the selected capacitor's ESR is extremely low, resulting in an oscillation at the output. It is recommended to replace this low ESR capacitor by using two general standard capacitors in parallel.

B. The capacitor voltage rating should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements needed for low output ripple voltage.

Output P-channel MOSFET and N-channel MOSFET Selection

A. The current ability of the output P-channel and N-channel MOSFETs must be at least larger than the peak switch current IPK. The voltage rating V_{DS} of the P-channel and N-channel MOSFETs should be at least 1.25 times the maximum input voltage.

B. The MOSFETs must be fast (switch time) and must be located close to the AP2011 using short leads and short printed circuit traces. In case of a large output current, we must layout a copper to reduce the temperature of these two MOSFETs.

Because of their fast switching speed and low $DS_{(ON)}$ resistor ($R_{DS(ON)}$), the Anachip AF44XX series provide the best performance and efficiency, and should be the first choice, especially in low output voltage applications.

Input Capacitor Selection

A. The RMS current rating of the input capacitor can be calculated from the following formula table. The capacitor manufactured by data sheet must be checked to assure that this current rating is not exceeded.

Calculation	Step-down (buck) regulator
δ	***Ton/(Ton+Toff)***
I_{PK}	$I_{LOAD(\max)} - I_{LOAD(\min)}$
I_m	$I_{LOAD(\max)} + I_{LOAD(\min)}$
ΔI_L	$2 \times I_{LOAD(\min)}$
$I_{IN(rms)}$	$\sqrt{\delta \times \left[\left(I_{PK} \times I_m \right) + \frac{1}{3} \left(\Delta I_L \right)^2 \right]}$

B. This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage.

4. Design Example

4.1 Summary of Target Specifications

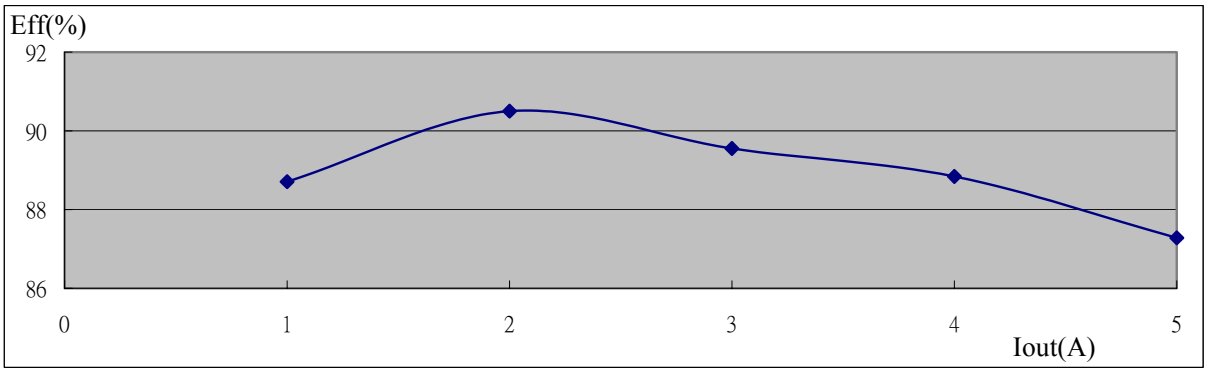
Input Power	$V_{IN(\max)}$ = +20V; $V_{IN(\min)}$ = +20V
Regulated Output Power	V_{OUT} = + 5V; $I_{LOAD(\max)}$ = 5A; $I_{LOAD(\min)}$ = 0.5A
Output Ripple Voltage	$V_{RIPPLE} \leq$ 50 mV peak-to-peak
Output Voltage Load Regulation	1% (0.2A to 5A)
Efficiency	87% minimum at full load.
Switching Frequency	F = Virtual Control (180KHz ± 10 %)

4.2 Calculating and Components Selection

Calculation Formula	Select Condition	Component spec.
$V_{OUT}=V_{FB}$ x $((R7/R9) + 1)$	$560\Omega \leq R9 \leq 5K\Omega$	R9=1kΩ; R7=3kΩ
$L_{(\min)} \geq \frac{[V_{IN(\min)} - V_{SAT} - V_{OUT}] \times T_{ON(\max)}}{2 \times I_{LOAD(\min)}}$ $I_{PK} = I_{LOAD(\max)} - I_{LOAD(\min)}$	$L_{(\min)} \geq 21uH$ $I_{rms} \geq I_{PK} = 4.5A$	Select L2=33uH
$ESR = \left(\frac{V_{RIPPLE}}{2 \times I_{LOAD(\min)}} \right)$ $V_{WVDC} \geq 1.5 \times V_{OUT}$	$ESR \leq 50m\Omega$ $V_{WVDC} \geq 7.5V$	Select C12 680uF/16V*1pcs
$I_{IN(rms)} = \sqrt{\delta \times \left[(I_{PK} \times I_m) + \frac{1}{3}(\Delta I_L)^2 \right]}$ $V_{WVDC} \geq 1.5 \times V_{IN(\max)}$	$I_{ripple} \geq I_{IN(rms)}$ =2.5A $V_{WVDC} \geq 30V$	Select C1 470uF/35V*1pcs

4.3 Efficiency Calculation

Vin(V)	Iin(A)	Vout(V)	Iout(A)	Eff(%)
20.09	0.28	4.99	1	88.70796
20.01	0.55	4.98	2	90.5002
20.1	0.83	4.98	3	89.55224
20.02	1.12	4.98	4	88.83973
20.05	1.42	4.97	5	87.2818



AP2011 Temperature VS Efficiency								
Parameter	Temperature(℃)							
	-40	-25	0	25	50	75	100	125
Vin(V)	20.04	20.02	20.01	20.03	20.06	20.10	20.06	20.03
Iin(A)	0.29	0.28	0.28	0.28	0.28	0.28	0.28	0.28
Vout(V)	4.85	4.94	4.94	4.92	4.89	4.87	4.84	4.78
Iout(A)	1	1	1	1	1	1	1	1
Efficiency (%)	83.453	88.162	88.170	87.725	87.060	86.531	86.170	88.385

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