



## Peak Reducing EMI Solution

### Features

- Generates an EMI optimized clocking signal at the output.
- Selectable output frequency range.
- Single 1.25% or 2.4% down spread output.
- Integrated loop filter components.
- Operates with a 3.3V supply.
- Low-power CMOS design.
- Available in 8-pin SOIC and 8-pin TSSOP packages.

### Product Description

The ASM3P2180A is a versatile Spread Spectrum frequency modulator designed specifically for a wide range of clock frequencies. The ASM3P2180A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The ASM3P2180A allows significant system cost savings by reducing the number of circuit board layers and shielding that are traditionally required to pass EMI regulations.

The ASM3P2180A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the

typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal’s bandwidth is called spread spectrum clock generation.

The ASM3P2180A uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all-digital method.

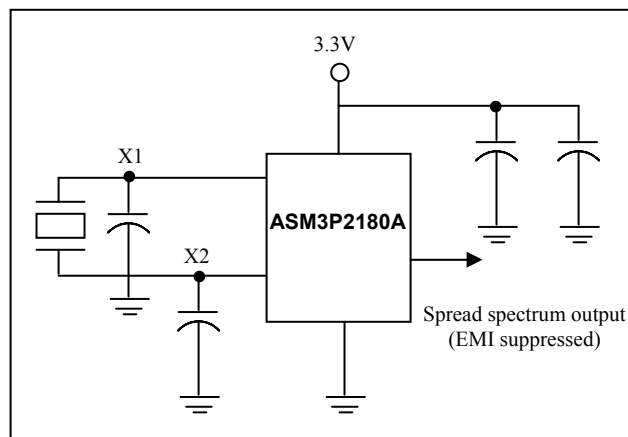
### Applications

The ASM3P2180A is targeted towards notebook LCD displays, other displays using an LVDS interface, PC peripheral devices and embedded systems.

### Key Specifications

Description		Specification
Supply voltages		$V_{DD} = 3.3V \pm 5\%$
Frequency range	FS1=0	$6 \text{ MHz} \leq F_{in} \leq 10 \text{ MHz}$
	FS1=1	$18 \text{ MHz} \leq F_{in} \leq 30 \text{ MHz}$
Cycle-to-cycle jitter		325 pS (max)
Selectable spread percentage		-1.25% or -2.4%
Output duty cycle		45/55% (worst case)
Output rise and fall time		5ns (maximum)

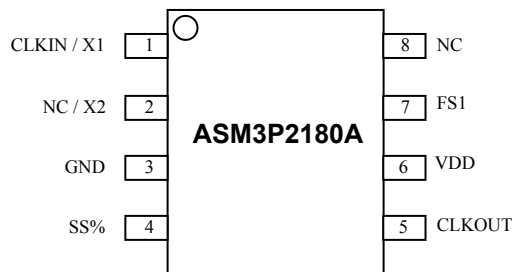
### Simplified Block Diagram





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## Pin Diagram



## Modulation Width Selection

SS%	Output
0	$FIN \geq FOUT \geq FIN - 1.25\%$
1	$FIN \geq FOUT \geq FIN - 2.4\%$

## Frequency Range Selection

FS1	Modulation Rate
0	$6 \leq FIN \leq 10$
1	$18 \leq FIN \leq 30$

## Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN / X1	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected to either an external crystal or an external reference clock.
2	NC / X2	O	Crystal connection. Connection for an external crystal. If using an external reference, this pin must be left unconnected.
3	GND	P	Ground to entire chip.
4	SS%	I	Modulation width selection. When spread spectrum feature is turned on, this pin is used to select the amount of variation and peak EMI reduction that is desired on the output signal. Internal pull-up resistor.
5	CLKOUT	O	Output modulated frequency. Copy of the un-modulated input clock.
6	VDD	P	Power supply for the entire chip (3.3V).
7	FS1	I	Frequency selection bit 1. This pin selects the frequency range of operation. ( <i>Refer to the Frequency Range Selection Table</i> ). This pin has an internal pull-up resistor.
8	NC	-	No connect.



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**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Unit
$V_{DD}, V_{IN}$	Voltage on any pin with respect to GND	-0.5 to + 7.0	V
$T_{STG}$	Storage temperature	-65 to +125	°C
$T_A$	Operating temperature	0 to 70	°C

Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
$V_{IL}$	Input low voltage	GND – 0.3	-	0.8	V
$V_{IH}$	Input high voltage	2.0	-	$V_{DD} + 0.3$	V
$I_{IL}$	Input low current (pull-up resistors on inputs SS%, FS1)	-	-	-27	μA
$I_{IH}$	Input high current	-	-	18	μA
$I_{XOL}$	$X_{OUT}$ output low current (@ 0.4V, $V_{DD} = 3.3V$ )	-	3	-	mA
$I_{XOH}$	$X_{OUT}$ output high current (@2.5V, $V_{DD} = 3.3V$ )	-	4	-	mA
$V_{OL}$	Output low voltage ( $V_{DD} = 3.3V$ , $I_{OL} = 4mA$ )	-	-	0.4	V
$V_{OH}$	Output high voltage ( $V_{DD} = 3.3V$ , $I_{OH} = 4mA$ )	2.5	-	-	V
$I_{CC}$	Dynamic supply current normal mode (3.3V and 10pF loading)	8	21	35	mA
$I_{DD}$	Static supply current standby mode	-	0.8	-	μA
$V_{DD}$	Operating voltage	2.8	3.3	3.7	V
$t_{ON}$	Power up time (first locked clock cycle after power up)	-	0.18	-	mS
$Z_{OUT}$	Clock output impedance	-	50	-	Ω

**AC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input frequency	6	-	30	MHz
CLKOUT	Output frequency	6	-	30	MHz
$t_{LH}^*$	Output rise time (measured at 0.8V to 2.0V)	1.2	1.3	1.4	nS
$t_{HL}^*$	Output fall time (measured at 2.0V to 0.8V)	0.8	0.9	1.0	nS
$t_{JC}$	Jitter (cycle to cycle)	-	-	325	pS
$t_D$	Output duty cycle	45	50	55	%

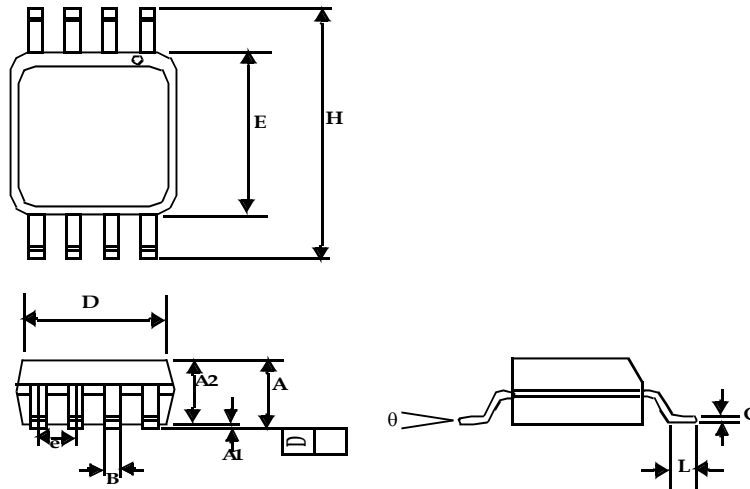
\* $t_{LH}$  and  $t_{HL}$  are measured into a capacitive load of 15pF



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Package Information:

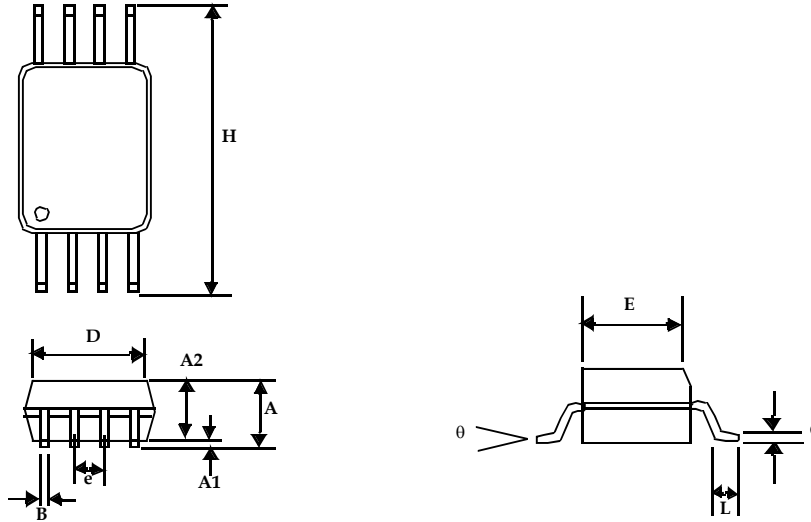
## 8-Pin SOIC Package



Symbol	Dimensions in inches		Dimensions in millimeters	
	Min	Max	Min	Max
A	0.057	0.071	1.45	1.80
A1	0.004	0.010	0.10	0.25
A2	0.053	0.069	1.35	1.75
B	0.012	0.020	0.31	0.51
C	0.004	0.01	0.10	0.25
D	0.186	0.202	4.72	5.12
E	0.148	0.164	3.75	4.15
e	0.050 BSC		1.27 BSC	
H	0.224	0.248	5.70	6.30
L	0.012	0.028	0.30	0.70
□	0°	8°	0°	8°



## 8-Pin TSSOP Package



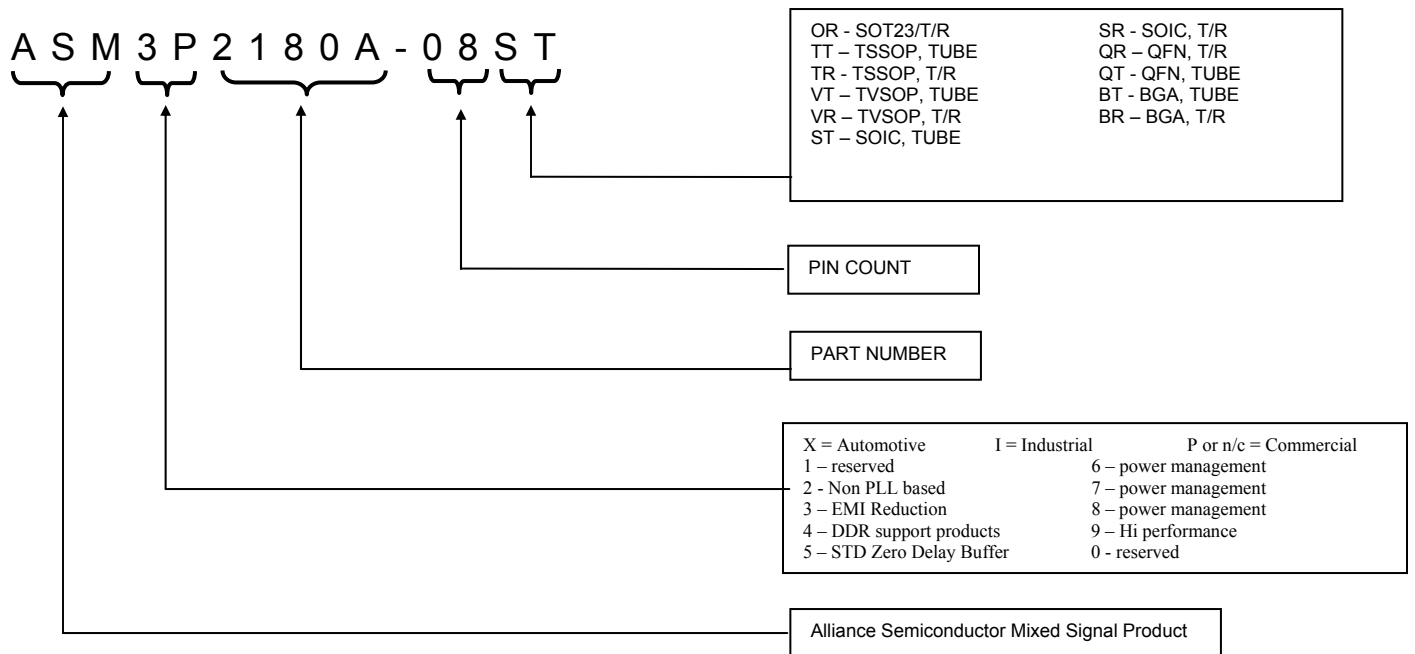
Symbol	Dimensions in inches		Dimensions in millimeters	
	Min	Max	Min	Max
A	0.047			1.10
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.244	0.260	6.20	6.60
L	0.018	0.030	0.45	0.75
$\theta$	0°	8°	0°	8°



Ordering Codes

Ordering Number	Marking	Package Type	Quantity per reel	Temperature
ASM3P2180A-08ST	ASM3P2180A	8-pin SOIC, tube		0° C to 70°C
ASM3P2180A-08SR	ASM3P2180A	8-pin SOIC, tape and reel	2500	0° C to 70°C
ASM3P2180A-08TT	ASM3P2180A	8-pin TSSOP, tube		0° C to 70°C
ASM3P2180A-08TR	ASM3P2180A	8-pin TSSOP, tape and reel	2500	0° C to 70°C

Ordering Information



Licensed under US patent Nos 5,488,627 and 5,631,920.



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003

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