
Features

General

- High-performance, Low-power AVR™ Enhanced RISC Architecture
 - 120 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low Power Idle and Power-down Modes
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to $\pm 6000V$
- Operating Ranges: 1.62 to 5.5V
- Compliant with GSM, 3GPP and EMV 2000 Specifications; PC Industry Compatible
- Available in Wafers, Modules, and Industry-standard Packages

Memory

- 48K Bytes of ROM Program Memory
- 18K Bytes of EEPROM, Including 128 OTP Bytes and 384-byte Bit-addressable Area
 - 1 to 128-byte Program / Erase
 - 1 ms Program / 1 ms Erase
 - Typically More than 500,000 Write/Erase Cycles at a Temperature of 25°C
 - 10 Years Data Retention
- 1.5K Bytes of RAM

Peripherals

- One I/O Port
 - Configurable to Support Communication Protocol Including ISO7816-3
- 16-bit Timer
- Random Number Generator (RNG)
- 2-level, 8-vector Interrupt Controller

Security

- Advanced Protection Against Physical Attack
- Environmental Protection Systems
- Voltage Monitor
- Secure Memory Management/Access Protection (Supervisor Mode)
- SPA/DPA Counter Measure

Development Tools

- Voyager Emulation Platform (ATV2 Standard) to Support Software Development
- IAR Systems EWAVR® V3.10 Debugger or Atmel's AVR Studio® Version 4.07 or Above
- Software Libraries and Application Notes



Secure Microcontroller for Smart Cards

AT90SC 4818RT Summary

6506AS-SMIC-30Mar04



Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.

Description

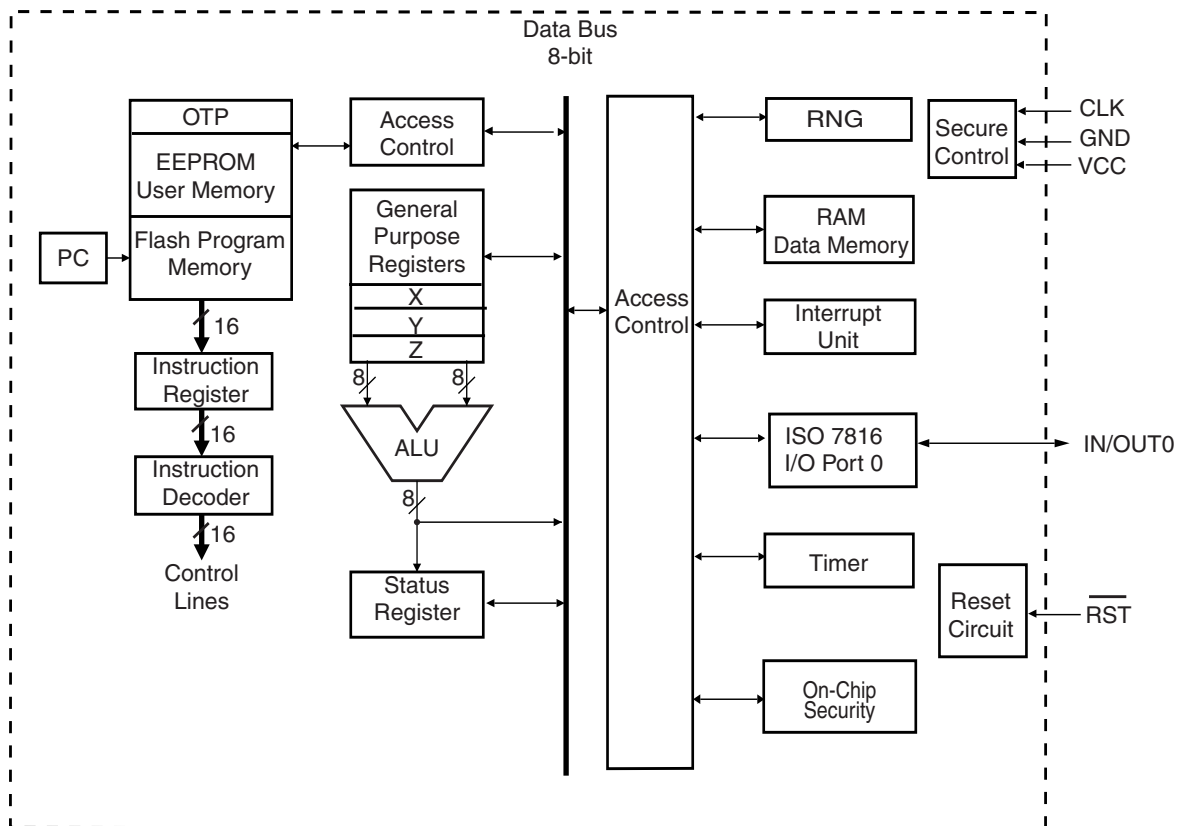
The AT90SC4818RT is a low power, high performance, 8/16-bit microcontroller based on the AVR™ enhanced RISC architecture, with flexible ROM program memory and EEPROM data memory. By executing powerful instructions in a single clock cycle, the AT90SC4818RT achieves throughputs close to 1 MIPS per Mhz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system. This technology combined with the versatile 8/16-bit CPU on a monolithic chip provides a highly flexible and cost-effective solution to many smartcard applications.

The AT90SC4818RT can also be configured to offer compatibility with the AT90SC4818R and the AT90SC4816R.

Figure 1 shows the AT90SC4818RT block diagram.

Figure 1. AT90SC4818RT secureAVR Enhanced RISC Architecture





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