



# ATA06212AD1C

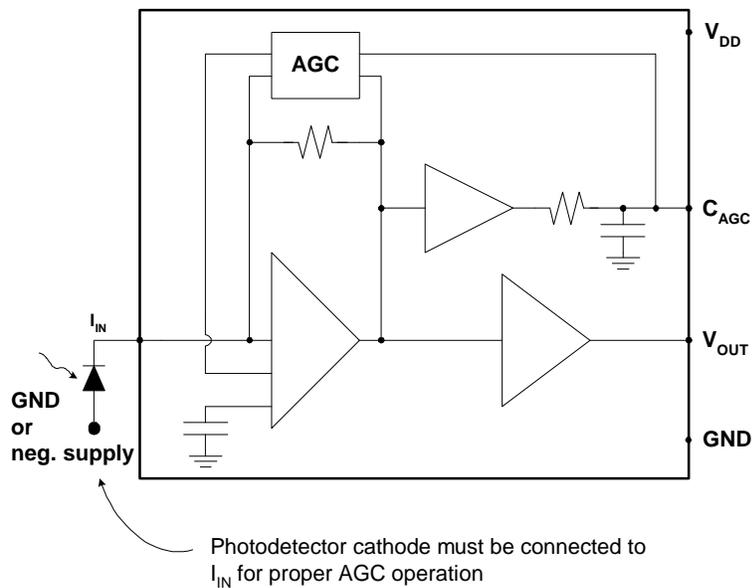
## Absolute Maximum Ratings

$V_{DD1}$	7.0 V
$V_{DD2}$	7.0 V
$I_{IN}$	5 mA
$T_A$	Operating Temp. -40 °C to 125 °C
$T_S$	Storage Temp. -65 °C to 150 °C

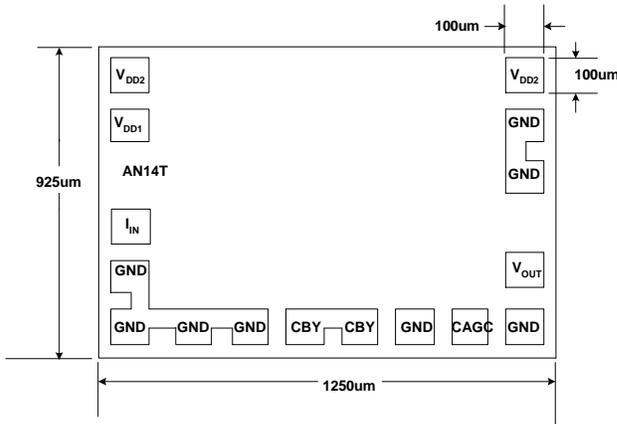
## ATA06212AD1C Pad Description

PAD	Description	Comment
$V_{DD1}$	VDD1	Positive supply for input gain stage
$V_{DD2}$	VDD2	Positive supply for second gain stage
$I_{IN}$	TIA Input Current	Connect to detector cathode for proper operation
$V_{OUT}$	TIA Output Voltage	Requires external DC block
$C_{AGC}$	External AGC Capacitor	$70k\Omega \times (4.5pF + C_{AGC}) = \text{AGC time constant}$
$C_{BY}$	Input gain stage bypass capacitor	>56 pF

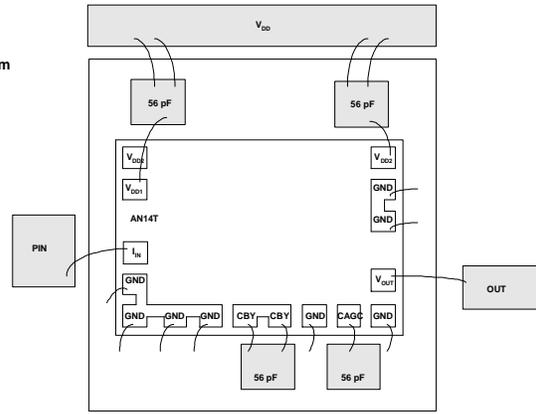
## ATA06212AD1C Equivalent Circuit



**Bonding Pads**



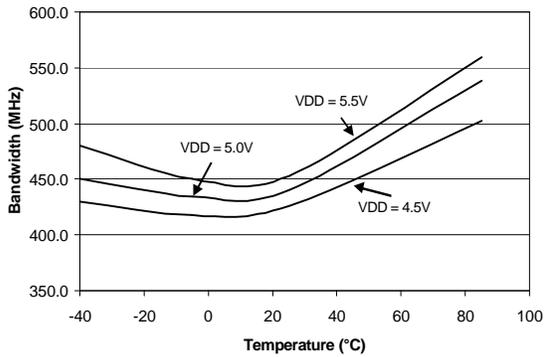
**Typical Bonding Diagram**



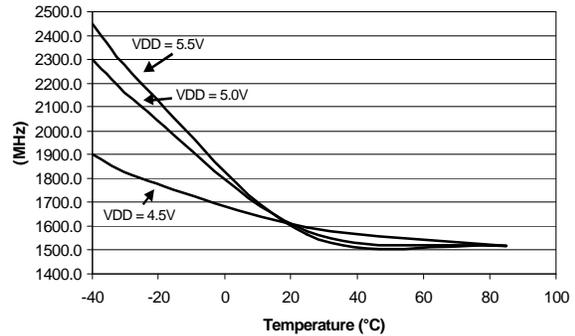
Note: Bond to either  $V_{DD2}$  Bond Pad

**TYPICAL CHARACTERISTICS ( $V_{DD} = +5V$ ,  $T_A = +25^\circ C$ , UNLESS OTHERWISE NOTED)**

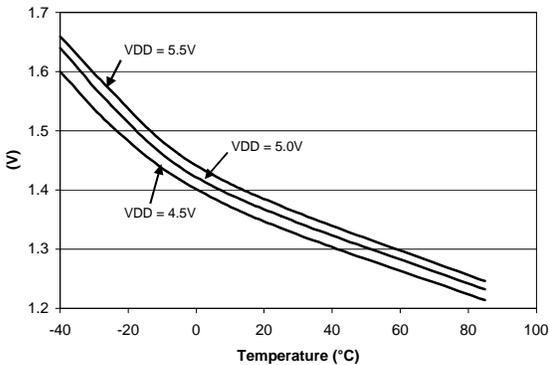
**3dB Bandwidth vs. Temperature**  
 $C_T = 0.6 \text{ pF}$



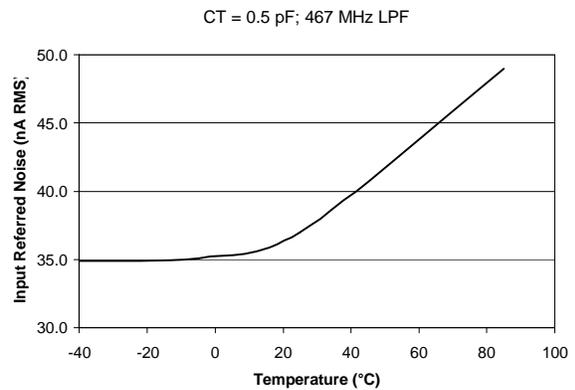
**AGC Bandwidth vs. Temperature**  
 $C_T = 0.6 \text{ pF}$ ;  $I_{IN} = 1.5 \text{ mA}$  (Average)



**Input Offset Voltage vs. Temperature**



**Input Referred Noise vs. Temperature**



## ATA06212AD1C

### POWER SUPPLIES AND GENERAL LAYOUT CONSIDERATIONS

The ATA06212AD1C may be operated from a positive supply as low as + 4.5 V and as high as + 6.0 V. Below + 4.5 V, bandwidth, overload and sensitivity will degrade, while at + 6.0 V, bandwidth, overload and sensitivity improve (see “Bandwidth vs. Temperature” curves). Use of surface mount (preferably MIM type capacitors), low inductance power supply bypass capacitors ( $\geq 56\text{pF}$ ) are essential for good high frequency and low noise performance. The power supply bypass capacitors should be mounted on or connected to a good low inductance ground plane.

### GENERAL LAYOUT CONSIDERATIONS

Since the gain stages of the transimpedance amplifier have an open loop bandwidth in excess of 1.0 GHz, it is essential to maintain good high frequency layout practices. To prevent oscillations, a low inductance RF ground plane should be made available for power supply bypassing. Traces that can be made short should be made short, and the utmost care should be taken to maintain very low capacitance at the photodiode-TIA interface ( $I_{IN}$ ); excess capacitance at this node will cause a degradation in bandwidth and sensitivity.

### $I_{IN}$ CONNECTION

Bonding the detector cathode to  $I_{IN}$  (and thus drawing current from the ATA06212AD1C) improves the dynamic range. Although the detector may be used in the reverse direction for input currents not exceeding  $25\ \mu\text{A}$ , the specifications for optical overload will not be met (refer to the equivalent circuit diagram).

### $V_{OUT}$ CONNECTION

The output pad should be connected via a coupling capacitor to the next stage of the receiver channel (filter or decision circuits), as the output buffers are not designed to drive a DC coupled 50 Ohm load (this would require an output bias current of approximately 36 mA to maintain a quiescent 1.8 Volts across the output load). If  $V_{OUT}$  is connected to a high input impedance decision circuit ( $>500\ \text{Ohms}$ ), then a coupling capacitor may not be required, although caution should be exercised since DC offsets of the photo detector/TIA combination may cause clipping of subsequent gain or decision circuits.

### SENSITIVITY AND BANDWIDTH

In order to guarantee sensitivity, the TIA is subjected to a comprehensive series of tests at the die sort level (100% testing at  $25\ ^\circ\text{C}$ ) to verify the DC and AC parametric performance (transimpedance and bandwidth).

## INDIRECT MEASUREMENT OF OPTICAL OVERLOAD

Optical overload can be defined as the maximum optical power above which the BER (bit error rate) increases beyond 1 error in  $10^{10}$  bits. The ATA06212AD1C is 100% tested at die sort by an AC measurement which has excellent correlation with a PRBS optical overload measurement.

## INPUT REFERRED NOISE CURRENT

The “Input Noise Current” is directly related to sensitivity . It can be defined as the output noise voltage ( $V_{OUT}$ ) with no input signal, (including a 400 MHz lowpass filter at the output of the TIA) divided by the AC transresistance.

## AGC CAPACITOR

It is important to select an external AGC capacitor of high quality and appropriate size. The ATA06212AD1C has an on-chip 70 k $\Omega$  resistor with a shunt 4.5 pF capacitor to ground. Without external capacitance the chip will provide an AGC time constant of 315 ns. For the best performance in a typical 622Mb/s SONET receiver, a minimum AGC capacitor of 56pF is recommended. This will provide the minimum amount of protection against pattern sensitivity and pulse width distortion on repetitive data sequences during high average optical power conditions. The AGC function can be disabled by bonding  $C_{AGC}$  to ground. Conservative design practices should be followed when selecting an AGC capacitor, since unit to unit variability of the internal time constant and various data conditions can lead to data errors if the chosen value is too small.

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NOTES

**NOTES**



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