

Structure : Silicon Monolithic Integrated Circuit
 Product Name : BTL Driver For CD-ROM

Device Name : **BA5983FM**

- Features :
- Driver exclusively for the 4-ch BTL
 - HSOP-M28 PIN power package
 - A wide dynamic range [PreVcc=8V, PowVcc=5V, 4V(Typ.) when RL=8Ω]
 - A built-in thermal shutdown circuit installed.
 - The power supplies such as PreVcc, PowVcc of CH1 and CH2, and PowVcc of CH3 and CH4 are supplied independently to achieve an efficient drive.
 - The standby mode can be controlled independently in CH1 to 3 and CH4.
 - Setting all of CH1-4 to the standby mode leads the entire circuit to the standby mode.
 - The driver pre-stage OP-amp features GND-sense and output rail-to-rail to make this IC suitable for a low voltage DSP.

○ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

| Parameter | Symbol | Limits | Unit |
|-----------------------------|---------------|------------|------|
| Power Supply Voltage | PREVcc,POWVcc | 13.5 | V |
| Power Dissipation | Pd | 2.2 *1 | W |
| Output current | IOMAX | 1 *2 | A |
| Operating Temperature Range | Topr | -35 to 85 | °C |
| Storage Temperature Range | Tstg | -55 to 150 | °C |

*1 When mounted on the glass/epoxy board with the size: 70 mm×70 mm, the thickness: 1.6 mm, and the rate of copper foil occupancy area: 3% or less.

Over Ta=25°C, derating at the rate of 17.6mW/°C.

*2 The power dissipation should be specified within the ASO range.

○ OPERATING POWER SUPPLY VOLTAGE RANGE

(To determine a power supply voltage, the power dissipation must be taken into consideration.)

| | |
|--------|-------------------|
| PREVcc | 4.5 to 13.2(V) |
| POWVcc | 4.5 to PREVcc (V) |

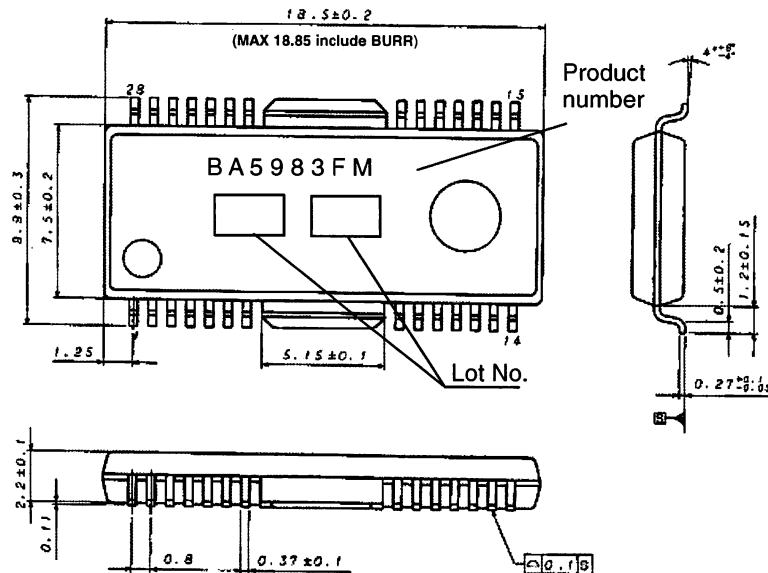
This product has not been checked for the strategic materials (or service) defined in the Foreign Exchange and Foreign Trade Control Law of Japan so that a verification work is required before exporting it.

Not designed for radiation resistance.

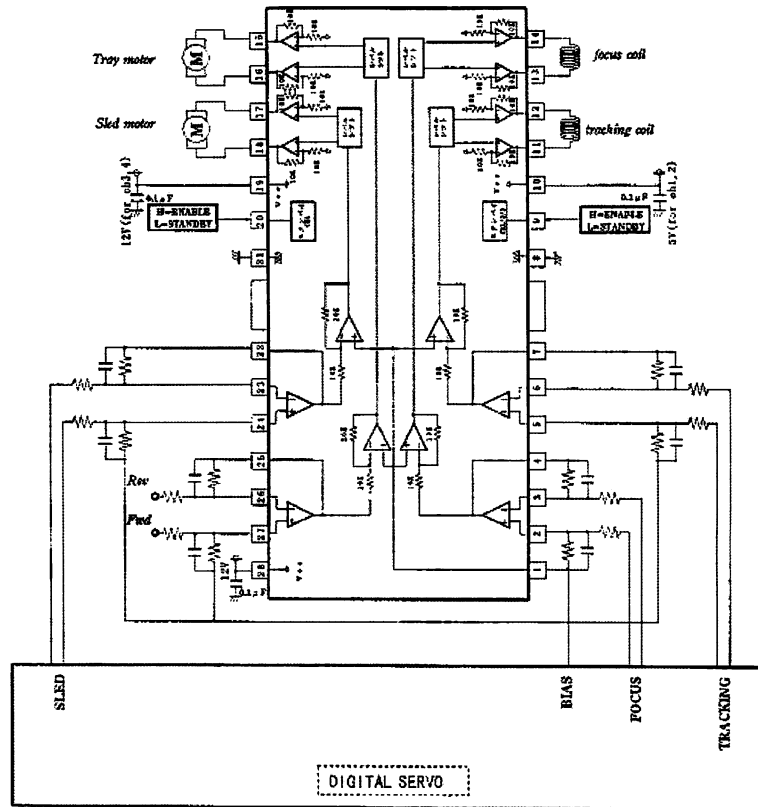
○ ELECTRIC CHARACTERISTICS (Ta=25°C, Vcc=12V, PVcc1=PVcc2=5V, BIAS=2.5V, RL=8Ω, Rd=0.5Ω, C=100pF, unless otherwise noted.)

| Parameter | Symbol | MIN. | TYP | MAX. | Unit | Condition |
|--|--------|------|-----|------|------|--|
| Quiescent Consumption Current | IQ | - | 20 | 30 | mA | No load applied |
| CH1, 2, 3 Standby IQST | IQST1 | - | 6.2 | 13 | mA | No load applied (IQ of Pre only) |
| CH4 Standby IQST | IQST2 | - | 16 | 26 | mA | No load applied (IQ of Pre only) |
| All CHs Standby IQST | IQST3 | - | - | 1 | mA | No load applied (IQ of Pre only) |
| <Driver> | | | | | | |
| Output Offset Voltage | VOOF | -70 | 0 | 70 | mV | |
| Maximum Output Amplitude 1 | VOM1 | 3.6 | 4.0 | - | V | CH1,2 VIN=VBIAS ± 1.65V |
| Maximum Output Amplitude 2 | VOM2 | 7.5 | 9 | - | V | CH3,4 VIN=VBIAS ± 1.65V * |
| Voltage Gain 1 | GVC1 | 10 | 12 | 14 | dB | CH1,2 VIN=VBIAS ± 0.5V |
| Voltage Gain 2 | GVC2 | 16 | 18 | 20 | dB | CH3,4 VIN=VBIAS ± 0.5V * |
| Slew Rate | SRDRV | - | 2 | - | V/μs | Input square wave, 100kHz, 2V _{P-P} |
| Standby ON Voltage | VSTON | - | - | 0.5 | V | |
| Standby OFF Voltage | VSTOFF | 2.0 | - | - | V | |
| Bias Drop Mute ON Voltage | VBMON | - | - | 0.7 | V | |
| Bias Drop Mute OFF Voltage | VBMOFF | 1.3 | - | - | V | |
| <Pre-stage Operational Amplifier> | | | | | | |
| Input Range (buffer in use) | VICM | 0 | - | 9 | V | |
| Input Offset Voltage | VOFOP | -6 | 0 | 6 | mV | |
| Input Bias Current | VBOP | - | - | 300 | nA | |
| High-level Output Voltage | VOHOP | 9 | 11 | - | V | VBIAS=6V |
| Low-level Output Voltage | VOLOP | - | - | 0.3 | V | VBIAS=6V |
| Output Driving Current Sink | ISI | 1 | - | - | mA | VBIAS=6V VCC with 50Ω attached |
| Output Driving Current Source | ISO | 300 | 500 | - | μA | VBIAS=6V GND with 50Ω |
| Slew Rate | SROP | - | 2 | - | V/μs | Input square wave, 100kHz, 2V _{P-P} |

○ OUTLINE DIMENSIONS, SYMBOLS



○ APPLICATION CIRCUIT DIAGRAM



Resistance unit: [Ω]

○ PIN NUMBERS, PIN NAMES

| No. | Pin Name | Description | No. | Pin Name | Description |
|-----|----------|---|-----|----------|---|
| 1 | BIASIN | Bias amp input terminal | 15 | VO4(+) | Driver CH4 positive output |
| 2 | OPIN1(+) | CH1 pre-stage amp non-inverted input terminal | 16 | VO4(-) | Driver CH4 negative output |
| 3 | OPIN1(-) | CH1 pre-stage amp inverted input terminal | 17 | VO3(+) | Driver CH3 positive output |
| 4 | OPOUT1 | CH1 pre-stage amp output terminal | 18 | VO3(-) | Driver CH3 negative output |
| 5 | OPIN2(+) | CH2 pre-stage amp non-inverted input terminal | 19 | PowVcc2 | PowVcc (CH3, 4) |
| 6 | OPIN2(-) | CH2 pre-stage amp inverted input terminal | 20 | STBY2 | CH4 standby control terminal |
| 7 | OPOUT2 | CH2 pre-stage amp output terminal | 21 | GND | GND |
| 8 | GND | GND | 22 | OPOUT3 | CH3 pre-stage amp output terminal |
| 9 | STBY1 | CH1 to 3 standby control terminal | 23 | OPIN3(-) | CH3 pre-stage amp inverted input terminal |
| 10 | PowVcc1 | PowVcc (CH1,2) | 24 | OPIN3(+) | CH3 pre-stage amp non-inverted input terminal |
| 11 | VO2(-) | Driver CH2 negative output | 25 | OPOUT4 | CH4 pre-stage amp output terminal |
| 12 | VO2(+) | Driver CH2 positive output | 26 | OPIN4(-) | CH4 pre-stage amp inverted input terminal |
| 13 | VO1(-) | Driver CH1 negative output | 27 | OPIN4(+) | CH4 pre-stage amp non-inverted input terminal |
| 14 | VO1(+) | Driver CH1 positive output | 28 | PreVcc | PreVcc |

Note) The positive or negative polarity of driver outputs is determined by the input polarity. (For example, when the pre-stage OPAMP is used as a buffer, the pin 14 shows a same polarity output while the pin 13 an opposite polarity output.)

○ CAUTIONS ON USE

- (1) When the voltage applied on the Bias terminal (pin 1) has dropped to 0.7V (Typ.) or less, the mute function will be activated. Under conditions of normal use, it should be set to 1.3V or above.
- (2) When the power supply voltage drops to 3.8V (Typ.) or less, the internal circuit will be OFF and, when recovering to 4.0V (Typ.) or above, the circuit will startup again.
- (3) Thermal shutdown (TSD), bias terminal voltage drop or power supply voltage drop will activate the mute functions for the circuits in all channels, where the output terminals will show the value of the internal bias voltage ($V_{cc}/2$).
- (4) Setting the Standby terminal to open or 0.5V or less leads all the circuits in the channel to the standby mode. Under conditions of normal use, the Standby terminal should be pulled-up to 2V or above.
- (5) Setting both two Standby terminals to open or 0.5V or less allows the circuit current to be in the standby mode. The switched threshold voltage is approximately 1.4V.
- (6) Vcc of the pre part must be provided with the same voltage as Vcc of the power part or higher.
- (7) The source current of the pre-stage OP-amp is a constant current and the input resistance of the next-stage driver: 10kΩ is also internally connected as a load.
Careful consideration must be given when determining the external load resistance value of the OP-amp.
- (8) Even though a radiating fin is connected to the GND inside of the package, it must be connected to the external GND.
- (9) About absolute maximum ratings
Exceeding the absolute maximum ratings, such as the applied voltage or the operating temperature range, may cause permanent device damage. As these cases cannot be limited to the broken short mode or the open mode, if a special mode where the absolute maximum ratings may be exceeded is assumed, it is recommended to take mechanical safety measures such as attaching fuses.
- (10) About power supply lines
As a measure against the back current regenerated by a counter electromotive force of the motor, a capacitor to be used as a regenerated-current path can be installed between the power supply and GND and its capacitance value should be determined after careful check that any problems, for example, a leak capacitance of the electrolytic capacitor at low temperature, are not found in various characteristics.
- (11) About GND potential
The electric potential of the GND terminal must be kept lowest in the circuitry at any operation states.
- (12) About thermal design
With consideration of the power dissipation (Pd) under conditions of actual use, a thermal design provided with an enough margin should be done.
- (13) About operations in a strong electric field
When used in a strong electric field, note that a malfunction may occur.
- (14) ASO
When using this IC, the output Tr must be set not to exceed the values specified in the absolute maximum ratings and ASO.
- (15) Thermal shutdown circuit
This IC incorporates a thermal shutdown circuit (TSD circuit). When the chip temperature reaches the value shown below, the coil output to the motor will be set to open.
The thermal shutdown circuit is designed only to shut off the IC from a thermal runaway and not intended to protect or guarantee the entire IC functions.
Therefore, users cannot assume that the TSD circuit once activated can be used continuously in the subsequent operations.

| TSD ON Temperature [°C] (typ.) | Hysteresis Temperature [°C] (typ.) |
|-----------------------------------|---------------------------------------|
| 175 | 25 |

- (16) About earth wiring patterns
When a small signal GND and a large current GND are provided, it is recommended that the large current GND pattern and the small signal GND pattern should be separated and grounded at a single point of the reference point of the set in order to prevent the voltage of the small signal GND from being affected by a voltage change caused by the resistance of the pattern wiring and the large current. Make sure that the GND wiring patterns of the external components will not change, too.

- (17) This IC is a monolithic IC which has a P⁺ isolations and P substrate to isolate elements each other. This P layer and an N layer in each element form a PN junction to construct various parasitic elements. Due to the IC structure, the parasitic elements are inevitably created by the potential relationship. Activation of the parasitic elements can cause interference between circuits and may result in a malfunction or, consequently, a fatal damage. Therefore, make sure that the IC must not be used under conditions that may activate the parasitic elements, for example, applying the lower voltage than the ground level (GND, P substrate) to the input terminals. In addition, do not apply the voltage to input terminals without applying the power supply voltage to the IC. Also while applying the power supply voltage, the voltage of each input terminal must not be over the power supply voltage, or within the guaranteed values in the electric characteristics.

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