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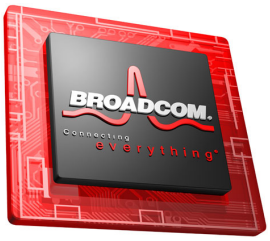
BCM8152 PRODUCT Brief



10 GBPS TRANSCEIVER WITH 10G CLOCK, BUS SKEW, AND LIMITING AMPLIFIER

FEATURES

- 10-Gigabit MSA (Multi-Source Agreement) compatible
- Fully integrated multi-rate CDR, DEMUX, CMU, and MUX
- 16-bit LVDS interface
- 10-gigabit serial transmitter clock output
- Limiting amplifier
- On-chip PLL-based clock generator
- Line and system loopback modes
- Receiver and transmitter serial data polarity invert
- Bit order reversal
- Analog loss-of-signal output (ALOSB) and input (LOSIB)
- Tx and Rx lock detect
- 10-word FIFO with overflow alarm absorbs system clock jitter
- Reference clock: 1/16 or 1/64 of the selectable data rate
- Selectable Rx clock and Rx data squelch upon ALOSB
- Selectable loop timing mode
- Internal phase detector and charge pump for cleanup PLL, external VCXO required
- Power supplies: core, LVPECL, LVDS output, and CML at 1.8V, LVDS input and CMOS I/O at 1.8 or 3.3V
- Power dissipation: 1.2W typical

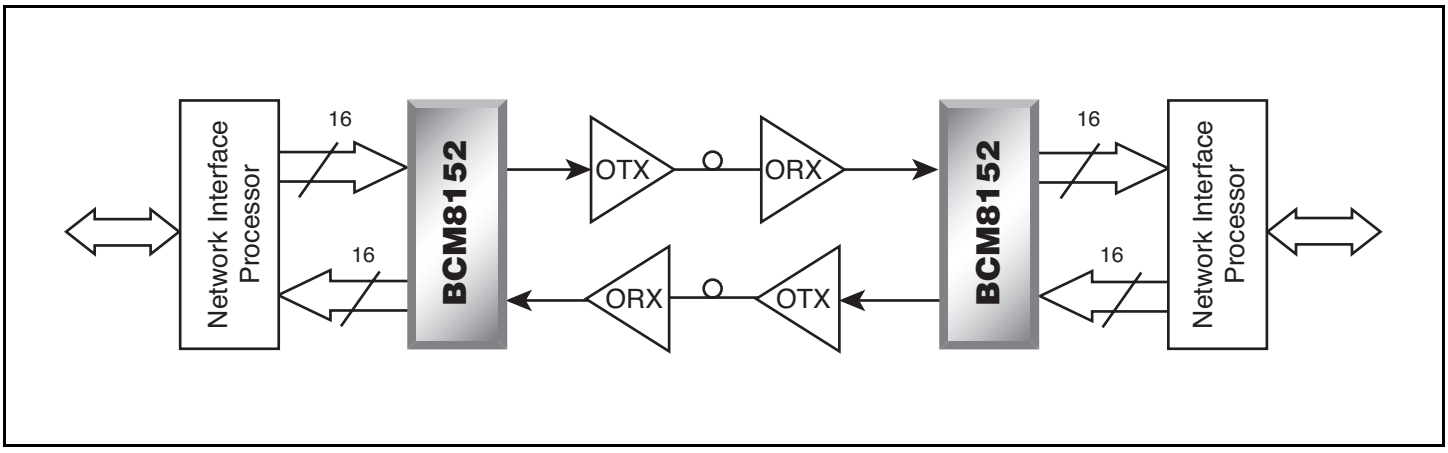
SUMMARY OF BENEFITS

- Provides compliance Optical Internetworking Forum (OIF), Telcordia, ITU-T, and IEEE 802.3ae standards.
- Reduces design cycle and time to market.
- High level of integration allows for higher port density solutions.
- Uses the most effective silicon economy of scale for CMOS-based devices.
- Standard CMOS fabrication process.

APPLICATIONS

- OC-192/STM-64/10 GE/FEC transmission equipment
- SONET/SDH/10 GE/FEC optical modules
- ADD/DROP multiplexers
- Digital cross-connects
- ATM switch backbone
- SONET/SDH/10 GE/FEC test equipment
- Terabit and edge routers

BCM8152 Functional Block Diagram



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